Virtex™-II Electrical Characteristics

Virtex-II devices are provided in -4, -5, and -6 speed grades, with -6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -4 speed grade industrial device are the same as for a -4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal Supply voltage relative to GND	–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.0	V
V_{REF}	Input Reference Voltage	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (user and dedicated I/Os)	–0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.5 to 4.0	V
V_{CCINT}	Longest Supply Voltage Rise Time from 0 V - 1.425 V	50	ms
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temp.	+220	°C
T_J	Operating junction temperature	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Power supplies might turn on in any order.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
	Internal Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	3.0	3.6	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.6	V
V_{BATT}	Battery voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. If V_{CCAUX} and V_{CCO} are both at 3.3 V, they must use a common supply voltage.
2. If battery is not used, do not connect V_{BATT}.
3. For LVDS operation, V_{CCAUX} min is 3.13 V and max is 3.47 V.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)	All	1.2		V
V_{DRI}	Data Retention V_{CCAUX} Voltage (below which configuration data might be lost)	All	2.5		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current[1]	Device Dependent			
I_{CCOQ}	Quiescent V_{CCO} supply current[1]	Device Dependent			
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current[1]	Device Dependent			
I_{REF}	V_{REF} current per bank	All			µA
I_L	Input or output leakage current	All			µA
C_{IN}	Input capacitance (sample tested)	All			pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note 2		mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)	All	Note 2		mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Data are retained even if V_{CCO} drops to 0 V.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms).

Table 4: **Supply Current Requirements**

Product	Description[2]	Current Requirement[3]
Virtex-II Family, Commercial Grade	Minimum required current supply	500 mA
Virtex-II Family, Industrial Grade	Minimum required current supply	500 mA

Notes:
1. Ramp rate used for this specification is from 0 to 1.5 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents may result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 5: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	V_{CCO} – 0.45	16	– 16
LVCMOS15	– 0.5	20% V_{CCO}	70% V_{CCO}	1.65	0.4	V_{CCO} – 0.45	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	48	– 8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	– 8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	– 16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	2.7	V_{REF} – 0.65	V_{REF} + 0.65	7.6	– 7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	2.7	V_{REF} – 0.80	V_{REF} + 0.80	15.2	– 15.2
AGP–2X	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.

LDT DC Specifications (LDT_25)

Table 6: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	530	600	740	mV
Change in V_{OD} Magnitude	ΔV_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals			30	mV
Output Common Mode Voltage	V_{OS}	R_T = 100 ohm across Q and $\overline{Q}$ signals	550	600	680	mV
Change in V_{OS} Magnitude	ΔV_{OS}				30	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 7: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.475	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 8: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.70	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V				mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV				V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 9 summarizes the DC output specifications of LVPECL.

Table 9: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as **Virtex-II Switching Characteristics**, page 7 (speed files).

Table 10 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 10: **Pin-to-Pin Performance**

Description	Pin-to-Pin (w/ I/O delays)	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder	6.7	XC2V1000 -5
32-bit Address Decoder	8.0	XC2V1000 -5
64-bit Address Decoder	9.6	XC2V1000 -5
4:1 MUX	6.0	XC2V1000 -5
8:1 MUX	6.8	XC2V1000 -5
16:1 MUX	6.8	XC2V1000 -5
32:1 MUX	8.9	XC2V1000 -5
Combinatorial (pad to LUT to pad)	5.4	XC2V1000 -5
Memory		
Block RAM		
Pad to setup	N/A	
Clock to Pad	N/A	
Distributed RAM		
Pad to setup	2.9	XC2V1000 -5
Clock to Pad	5.3 (no clk skew)	XC2V1000 -5

Table 11 shows internal (register-to-register) performance. Values are reported in MHz.

Table 11: **Register-to-Register Performance**

Description	Register-to-Register Performance	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder	460	XC2V1000 -5
32-bit Address Decoder	312.5	XC2V1000 -5
64-bit Address Decoder	264.6	XC2V1000 -5
4:1 MUX	554	XC2V1000 -5
8:1 MUX	516.5	XC2V1000 -5
16:1 MUX	428	XC2V1000 -5
32:1 MUX	371.2	XC2V1000 -5
Register to LUT to Register	715.3	XC2V1000 -5
8-bit Adder	315.2	XC2V1000 -5
16-bit Adder	284.8	XC2V1000 -5
64-bit Adder	171.2	XC2V1000 -5
64-bit Counter	186.2	XC2V1000 -5
64-bit Accumulator	116.9	XC2V1000 -5
Multiplier 18x18 (with Block RAM inputs)	103.8	XC2V1000 -5
Multiplier 18x18 (with Register inputs)	147.3	XC2V1000 -5
Memory		
Block RAM		
Single-Port 4096 x 4 bits	N/A	
Single-Port 2048 x 9 bits	N/A	
Single-Port 1024 x 18 bits	N/A	
Single-Port 512 x 36 bits	N/A	
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits	N/A	
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits	N/A	
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits	N/A	
Distributed RAM		
Single-Port 32 x 8-bit	481.0	XC2V1000 -5
Single-Port 64 x 8-bit	405.8	XC2V1000 -5
Single-Port 128 x 8-bit	343.4	XC2V1000 -5
Dual-Port 16 x 8	264.9	XC2V1000 -5
Dual-Port 32 x 8	414.3	XC2V1000 -5
Dual-Port 64 x 8	363.4	XC2V1000 -5
Dual-Port 128 x 8	318.7	XC2V1000 -5
Shift Registers		
128-bit SRL	N/A	
256-bit SRL	N/A	

Table 11: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register Performance	Device Used & Speed Grade
FIFOs (Async. in Block RAM)		
1024 x 18-bit	N/A	
1024 x 18-bit	N/A	
FIFOs (Sync. in SRL)		
128 x 8-bit	N/A	
128 x 16-bit	N/A	
CAMs in Block RAM		
32 x 9-bit	N/A	
64 x 9-bit	N/A	
128 x 9-bit	N/A	
256 x 9-bit	N/A	
CAMs in SRL		
32 x 16-bit	N/A	
64 x 32-bit	N/A	
128 x 40-bit	N/A	
256 x 48-bit	N/A	
1024 x 16-bit	N/A	
1024 x 72-bit	N/A	

Virtex-II Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Final. Note that **Virtex-II Performance Characteristics**, page 5 are subject to these guidelines, as well. The status of each designation is defined as follows:

Advance:These speed files are based on additional simulation and testing of some family members. Although speed grades with this designation are considered relatively stable, some under-reporting might still occur. All family members do not necessarily transition to “Advance” at the same time. Typically, the slowest speed grades transition to “Advance” before faster speed grades.

Preliminary:Preliminary speed files are based on full device characterization. Devices and speed grades with this designation are considered safe for use in production designs. There are no under-reported delays.

Final:Final speed files are released once the family has enough production history and full correlation between the speeds files and devices is established over numerous production lots.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.

Table 12: **IOB Input Switching Characteristics**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All		0.61	0.70	ns, max
Pad to I output, with delay	T_{IOPID}			2.61	3.00	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All		0.82	0.94	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}			2.82	3.24	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.66	0.76	ns, max
Setup and Hold Times With Respect to Clock at IOB **Input Register**						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All		0.69 / 0.00	0.79 / 0.00	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$			2.69 / 0.00	3.09 / 0.00	ns, min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21 / 0.00	0.24 / 0.00	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All		0.19	0.21	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All		0.32	0.36	ns, max
GSR to output IQ	T_{GSRQ}	All		7.66	8.81	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 17.

IOB Input Switching Characteristics Standard Adjustments

Table 13: **IOB Input Switching Characteristics Standard Adjustments**

Description	Symbol	Standard	Speed Grade			Units
			–6	–5	–4	
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL		0.00	0.00	ns
	$T_{ILVCMOS33}$	LVCMOS33		0.00	0.00	ns
	$T_{ILVCMOS25}$	LVCMOS25		0.11	0.12	ns
	$T_{ILVCMOS18}$	LVCMOS18		0.43	0.49	ns
	$T_{ILVCMOS15}$	LVCMOS15		1.00	1.14	ns
	T_{ILVDS_25}	LVDS_25		0.60	0.69	ns
	T_{ILVDS_33}	LVDS_33		0.60	0.69	ns
	$T_{ILVPECL\_33}$	LVPECL		0.60	0.69	ns

Table 13: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V		0.00	0.00	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V		0.00	0.00	ns
	T_{IPCIX}	PCI–X, 133 MHz, 3.3 V		0.00	0.00	ns
	T_{IGTL}	GTL		0.42	0.48	ns
	$T_{IGTLPLUS}$	GTLP		0.42	0.48	ns
	T_{IHSTL_I}	HSTL I		0.42	0.48	ns
	T_{IHSTL_II}	HSTL II		0.42	0.48	ns
	T_{IHSTL_III}	HSTL III		0.42	0.48	ns
	T_{IHSTL_IV}	HSTL IV		0.42	0.48	ns
	T_{ISSTL2_I}	SSTL2 I		0.42	0.48	ns
	T_{ISSTL2_II}	SSTL2 II		0.42	0.48	ns
	T_{ISSTL3_I}	SSTL3 I		0.35	0.40	ns
	T_{ISSTL3_II}	SSTL3 II		0.35	0.40	ns
	T_{IAGP}	AGP–2X		0.35	0.40	ns
	$T_{ILVDCI33}$	LVDCI_33		0.00	0.00	ns
	$T_{ILVDCI25}$	LVDCI_25		0.11	0.12	ns
	$T_{ILVDCI18}$	LVDCI_18		0.43	0.49	ns
	$T_{ILVDCI15}$	LVDCI_15		1.00	1.14	ns
	$T_{ILVDCI\_DV2\_33}$	LVDCI_DV2_33		0.00	0.00	ns
	$T_{ILVDCI\_DV2\_25}$	LVDCI_DV2_25		0.11	0.12	ns
	$T_{ILVDCI\_DV2\_18}$	LVDCI_DV2_18		0.43	0.49	ns
	$T_{ILVDCI\_DV2\_15}$	LVDCI_DV2_15		1.00	1.14	ns
	T_{IGTL_DCI}	GTL_DCI		0.42	0.48	ns
	T_{IGTLP_DCI}	GTLP_DCI		0.42	0.48	ns
	$T_{IHSTL\_I\_DCI}$	HSTL_I_DCI		0.42	0.48	ns
	$T_{IHSTL\_II\_DCI}$	HSTL_II_DCI		0.42	0.48	ns
	$T_{IHSTL\_III\_DCI}$	HSTL_III_DCI		0.42	0.48	ns
	$T_{IHSTL\_IV\_DCI}$	HSTL_IV_DCI		0.42	0.48	ns
	$T_{ISSTL2\_I\_DCI}$	SSTL2_I_DCI		0.42	0.48	ns
	$T_{ISSTL2\_II\_DCI}$	SSTL2_II_DCI		0.42	0.48	ns
	$T_{ISSTL3\_I\_DCI}$	SSTL3_I_DCI		0.35	0.40	ns
	$T_{ISSTL3\_II\_DCI}$	SSTL3_II_DCI		0.35	0.40	ns
	T_{ILDT_25}	LDT_25		0.49	0.56	ns
	T_{IULVDS_25}	ULVDS_25		0.49	0.56	ns

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 17.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 11.

Table 14: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–6**	**–5**	**–4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}		2.88	3.31	ns, max
O input to Pad via transparent latch	T_{IOOLP}		3.09	3.55	ns, max
3-State Delays					
T input to Pad high-impedance (Note 2)	T_{IOTHZ}		2.37	2.73	ns, max
T input to valid data on Pad	T_{IOTON}		2.37	2.73	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$		2.58	2.97	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$		2.58	2.97	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}		6.89	7.92	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}		3.24	3.73	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}		2.88	3.32	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}		2.88	3.32	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}		0.19/0.00	0.21/0.00	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$		0.21/0.00	0.24/0.00	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$		0.19/0.00	0.21/0.00	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}		0.22/0.00	0.26/0.00	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$		0.21/0.00	0.24/0.00	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$		0.19/0.00	0.21/0.00	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}		3.08	3.55	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}		2.54	2.92	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}		2.54	2.92	ns, max
GSR to Pad	T_{IOGSRQ}		5.98	6.88	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 15: **IOB Output Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA		11.13	12.80	ns
	T_{OLVTTL_S4}	4 mA		6.87	7.90	ns
	T_{OLVTTL_S6}	6 mA		4.79	5.50	ns
	T_{OLVTTL_S8}	8 mA		3.40	3.91	ns
	T_{OLVTTL_S12}	12 mA		2.61	3.00	ns
	T_{OLVTTL_S16}	16 mA		1.83	2.10	ns
	T_{OLVTTL_S24}	24 mA		1.22	1.40	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA		7.66	8.80	ns
	T_{OLVTTL_F4}	4 mA		3.05	3.50	ns
	T_{OLVTTL_F6}	6 mA		1.83	2.10	ns
	T_{OLVTTL_F8}	8 mA		0.27	0.30	ns
	T_{OLVTTL_F12}	12 mA		0.00	0.00	ns
	T_{OLVTTL_F16}	16 mA		–0.44	–0.50	ns
	T_{OLVTTL_F24}	24 mA		–0.52	–0.60	ns
	T_{OLVDS_25}	LVDS		–1.12	–1.29	ns
	T_{OLVDS_33}	LVDS		–1.18	–1.36	ns
	$T_{OLVDSEXT\_25}$	LVDS		–1.03	–1.19	ns
	$T_{OLVDSEXT\_33}$	LVDS		–1.05	–1.21	ns
	T_{OLDT_25}	LDT		–1.11	–1.28	ns
	T_{OBLVDS_25}	BLVDS				ns
	T_{OULVDS_25}	ULVDS		–1.11	–1.28	ns
	$T_{OLVPECL\_33}$	LVPECL		0.81	0.93	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V		2.79	3.20	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V		0.27	0.30	ns
	T_{OPCIX}	PCI–X, 133 MHz, 3.3 V		0.27	0.30	ns
	T_{OGTL}	GTL		0.00	0.00	ns
	T_{OGTLP}	GTLP		0.00	0.00	ns
	T_{OHSTL_I}	HSTL I		0.18	0.20	ns
	T_{OHSTL_II}	HSTL II		–0.17	–0.20	ns
	T_{OHSTL_IIII}	HSTL III		–0.34	–0.40	ns
	T_{OHSTL_IV}	HSTL IV		–0.52	–0.60	ns
	T_{OSSTL2_I}	SSTL2 I		–0.09	–0.10	ns
	T_{OSSTL2_II}	SSTL2 II		–0.34	–0.40	ns

Table 15: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{OSSTL3_I}	SSTL3 I		0.00	0.00	ns
	T_{OSSTL3_II}	SSTL3 II		–0.17	–0.20	ns
	T_{OAGP}	AGP–2X		–0.26	–0.30	ns
	$T_{OLVCMOS33\_S2}$	LVCMOS33, Slow, 2 mA		9.66	11.10	ns
	$T_{OLVCMOS33\_S4}$	4 mA		5.51	6.33	ns
	$T_{OLVCMOS33\_S6}$	6 mA		4.00	4.60	ns
	$T_{OLVCMOS33\_S8}$	8 mA		2.70	3.10	ns
	$T_{OLVCMOS33\_S12}$	12 mA		2.27	2.60	ns
	$T_{OLVCMOS33\_S16}$	16 mA		1.40	1.60	ns
	$T_{OLVCMOS33\_S24}$	24 mA		1.31	1.50	ns
	$T_{OLVCMOS33\_F2}$	LVCMOS33, Fast, 2 mA		7.22	8.30	ns
	$T_{OLVCMOS33\_F4}$	4 mA		3.13	3.60	ns
	$T_{OLVCMOS33\_F6}$	6 mA		1.40	1.60	ns
	$T_{OLVCMOS33\_F8}$	8 mA		0.27	0.30	ns
	$T_{OLVCMOS33\_F12}$	12 mA		0.00	0.00	ns
	$T_{OLVCMOS33\_F16}$	16 mA		–0.34	–0.40	ns
	$T_{OLVCMOS33\_F24}$	24 mA		–0.52	–0.60	ns
	$T_{OLVCMOS25\_S2}$	LVCMOS25, Slow, 2 mA		11.22	12.90	ns
	$T_{OLVCMOS25\_S4}$	4 mA		6.44	7.40	ns
	$T_{OLVCMOS25\_S6}$	6 mA		5.83	6.70	ns
	$T_{OLVCMOS25\_S8}$	8 mA		5.05	5.80	ns
	$T_{OLVCMOS25\_S12}$	12 mA		3.66	4.20	ns
	$T_{OLVCMOS25\_S16}$	16 mA		2.96	3.40	ns
	$T_{OLVCMOS25\_S24}$	24 mA		2.61	3.00	ns
	$T_{OLVCMOS25\_F2}$	LVCMOS25, Fast, 2 mA		5.57	6.40	ns
	$T_{OLVCMOS25\_F4}$	4 mA		1.74	2.00	ns
	$T_{OLVCMOS25\_F6}$	6 mA		1.05	1.20	ns
	$T_{OLVCMOS25\_F8}$	8 mA		0.70	0.80	ns
	$T_{OLVCMOS25\_F12}$	12 mA		0.18	0.20	ns
	$T_{OLVCMOS25\_F16}$	16 mA		0.00	0.00	ns
	$T_{OLVCMOS25\_F24}$	24 mA		–0.17	–0.20	ns
	$T_{OLVCMOS18\_S2}$	LVCMOS18, Slow, 2 mA		20.18	23.20	ns
	$T_{OLVCMOS18\_S4}$	4 mA		13.74	15.80	ns
	$T_{OLVCMOS18\_S6}$	6 mA		10.35	11.90	ns
	$T_{OLVCMOS18\_S8}$	8 mA		9.57	11.00	ns
	$T_{OLVCMOS18\_S12}$	12 mA		8.18	9.40	ns
	$T_{OLVCMOS18\_S16}$	16 mA		7.74	8.90	ns

Table 15: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	$T_{OLVCMOS18\_F2}$	LVCMOS18, Fast, 2 mA		7.66	8.80	ns
	$T_{OLVCMOS18\_F4}$	4 mA		3.48	4.00	ns
	$T_{OLVCMOS18\_F6}$	6 mA		1.57	1.80	ns
	$T_{OLVCMOS18\_F8}$	8 mA		1.40	1.60	ns
	$T_{OLVCMOS18\_F12}$	12 mA		0.70	0.80	ns
	$T_{OLVCMOS18\_F16}$	16 mA		0.61	0.70	ns
	$T_{OLVCMOS15\_S2}$	LVCMOS15, Slow, 2 mA		25.57	29.40	ns
	$T_{OLVCMOS15\_S4}$	4 mA		18.09	20.80	ns
	$T_{OLVCMOS15\_S6}$	6 mA		16.79	19.30	ns
	$T_{OLVCMOS15\_S8}$	8 mA		14.53	16.70	ns
	$T_{OLVCMOS15\_S12}$	12 mA		13.31	15.30	ns
	$T_{OLVCMOS15\_S16}$	16 mA		12.53	14.40	ns
	$T_{OLVCMOS15\_F2}$	LVCMOS15, Fast, 2 mA		7.48	8.60	ns
	$T_{OLVCMOS15\_F4}$	4 mA		3.83	4.40	ns
	$T_{OLVCMOS15\_F6}$	6 mA		2.79	3.20	ns
	$T_{OLVCMOS15\_F8}$	8 mA		1.74	2.00	ns
	$T_{OLVCMOS15\_F12}$	12 mA		1.40	1.60	ns
	$T_{OLVCMOS15\_F16}$	16 mA		1.40	1.60	ns
	$T_{OLVDCI33}$	LVDCI_33		0.09	0.10	ns
	$T_{OLVDCI25}$	LVDCI_25		0.18	0.20	ns
	$T_{OLVDCI18}$	LVDCI_18		0.44	0.50	ns
	$T_{OLVDCI15}$	LVDCI_15		0.53	0.60	ns
	$T_{OLVDCI\_DV2\_33}$	LVDCI_DV2_33		–0.87	–1.00	ns
	$T_{OLVDCI\_DV2\_25}$	LVDCI_DV2_25		–0.69	–0.80	ns
	$T_{OLVDCI\_DV2\_18}$	LVDCI_DV2_18		–0.60	–0.70	ns
	$T_{OLVDCI\_DV2\_15}$	LVDCI_DV2_15		–0.43	–0.50	ns
	T_{OGTL_DCI}	GTL_DCI		0.35	0.40	ns
	T_{OGTLP_DCI}	GTLP_DCI		0.27	0.30	ns
	$T_{OHSTL\_I\_DCI}$	HSTL_I_DCI		0.18	0.20	ns
	$T_{OHSTL\_II\_DCI}$	HSTL_II_DCI		–0.17	–0.20	ns
	$T_{OHSTL\_III\_DCI}$	HSTL_III_DCI		–0.34	–0.40	ns
	$T_{OHSTL\_IV\_DCI}$	HSTL_IV_DCI		–0.52	–0.60	ns
	$T_{OSSTL2\_I\_DCI}$	SSTL2_I_DCI		–0.09	–0.10	ns
	$T_{OSSTL2\_II\_DCI}$	SSTL2_II_DCI		–0.34	–0.40	ns
	$T_{OSSTL3\_I\_DCI}$	SSTL3_I_DCI		0.00	0.00	ns
	$T_{OSSTL3\_II\_DCI}$	SSTL3_II_DCI		–0.17	–0.20	ns

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard, as listed in Table 16.

Table 16: **Constants for Use in Calculation of T_{IOOP}**

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	
LVTTL Fast Slew Rate, 4mA drive	35	
LVTTL Fast Slew Rate, 6mA drive	35	
LVTTL Fast Slew Rate, 8mA drive	35	
LVTTL Fast Slew Rate, 12mA drive	35	
LVTTL Fast Slew Rate, 16mA drive	35	
LVTTL Fast Slew Rate, 24mA drive	35	
LVTTL Slow Slew Rate, 2mA drive	35	
LVTTL Slow Slew Rate, 4mA drive	35	
LVTTL Slow Slew Rate, 6mA drive	35	
LVTTL Slow Slew Rate, 8mA drive	35	
LVTTL Slow Slew Rate, 12mA drive	35	
LVTTL Slow Slew Rate, 16mA drive	35	
LVTTL Slow Slew Rate, 24mA drive	35	
LVCMOS33	35	
LVCMOS25	35	
LVCMOS18	35	
LVCMOS15	35	
PCI 33MHZ 3.3 V	10	
PCI 66 MHz 3.3 V	10	
PCI–X 133 MHz 3.3 V	10	
GTL	0	
GTLP	0	
HSTL Class I	20	
HSTL Class II	20	
HSTL Class III	20	
HSTL Class IV	20	
SSTL2 Class I	30	
SSTL2 Class II	30	
SSTL3 Class I	30	
SSTL3 Class II	30	
AGP–2X	10	

Notes:
1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding T_{IOOP}.

$$T_{IOOP} = T_{IOOP} + T_{OPADJUST} + (C_{LOAD} - C_{SL}) * fl$$

Where:

$T_{OPADJUST}$ is reported above in the Output Delay Adjustment section.

C_{LOAD} is the capacitive load for the design.

Table 17: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	–
LVCMOS33	0	3.3	1.65	–
LVCMOS25	0	2.5	1.25	–
LVCMOS18	0	1.8	0.9	–
LVCMOS15	0	1.5	0.75	–
PCI33_3	Per PCI Specification			–
PCI66_3	Per PCI Specification			–
PCIX33_3	Per PCI–X Specification			–
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
AGP–2X	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL	1.6 –0.3	1.6 + 0.3	1.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in Table 16.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
5. Use of IBIS models results in a more accurate prediction of the propagation delay:
   a. Model the output in an IBIS simulation into the standard capacitive load.
   b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
   c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
   d. Record the results from the new simulation.
   e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

Clock Distribution Switching Characteristics

Table 18: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
GCLK IOB **and Buffer**					
Global Clock PAD to output.	T_{GPIO}		0.36	0.41	ns, max
Global Clock Buffer I input to O output	T_{GIO}		0.23	0.26	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 14). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 19: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}		0.39	0.45	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}		0.58	0.67	ns, max
5-input function: F/G inputs to X output	T_{IF5X}		0.77	0.88	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}		0.33	0.38	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}		0.25	0.28	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}		0.25	0.28	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}		0.49	0.56	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}		0.33	0.37	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}		0.42	0.48	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}		0.61	0.70	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}		0.28/0.00	0.32/0.00	ns, min
DY inputs	T_{DYCK}/T_{CKDY}		0.19/0.00	0.22/0.00	ns, min
DX inputs	T_{DXCK}/T_{CKDX}		0.19/0.00	0.22/0.00	ns, min
CE input	T_{CECK}/T_{CKCE}		0.21/0.00	0.24/0.00	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}		0.19/ 0.00	0.22/0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}		0.57	0.66	ns, min
Minimum Pulse Width, Low	T_{CL}		0.57	0.66	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}		0.57	0.66	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}		0.25	0.29	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}		880	765	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Table 20: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$		1.78	2.04	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$		2.09	2.41	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$		1.89	2.17	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		0.67/0.00	0.77/0.00	ns, min
F/G address inputs	T_{AS}/T_{AH}		0.44/0.00	0.50/0.00	ns, min
CE input (WE)	T_{WES}/T_{WEH}		0.46/0.00	0.53/0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}		0.63	0.72	ns, min
Minimum Pulse Width, Low	T_{WPL}		0.63	0.72	ns, min
Minimum clock period to meet address write cycle time	T_{WC}		1.25	1.44	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 21: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}		2.53	2.91	ns, max
Clock CLK to X/Y outputs	T_{REG32}		2.84	3.27	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}		2.45	2.82	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}		2.39	2.75	ns, max
Clock CLK to Shiftout	T_{CKSH}		2.17	2.49	ns, max
Clock CLK to F5 output	T_{REGF5}		2.64	3.04	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}		0.28/0.00	0.32/0.00	ns, min
CE input (WS)	T_{WSS}/T_{WSH}		0.21/0.00	0.24/0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}		0.63	0.72	ns, min
Minimum Pulse Width, Low	T_{SRPL}		0.63	0.72	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Multiplier Switching Characteristics

Table 22: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT}		4.34	4.98	ns, max
Input to Pin34	T_{MULT}		4.22	4.85	ns, max
Input to Pin33	T_{MULT}		4.11	4.72	ns, max
Input to Pin32	T_{MULT}		3.99	4.59	ns, max
Input to Pin31	T_{MULT}		3.88	4.46	ns, max
Input to Pin30	T_{MULT}		3.77	4.33	ns, max
Input to Pin29	T_{MULT}		3.65	4.20	ns, max
Input to Pin28	T_{MULT}		3.54	4.07	ns, max
Input to Pin27	T_{MULT}		3.42	3.93	ns, max
Input to Pin26	T_{MULT}		3.31	3.80	ns, max
Input to Pin25	T_{MULT}		3.20	3.67	ns, max
Input to Pin24	T_{MULT}		3.08	3.54	ns, max
Input to Pin23	T_{MULT}		2.97	3.41	ns, max
Input to Pin22	T_{MULT}		2.85	3.28	ns, max
Input to Pin21	T_{MULT}		2.74	3.15	ns, max
Input to Pin20	T_{MULT}		2.63	3.02	ns, max
Input to Pin19	T_{MULT}		2.51	2.89	ns, max
Input to Pin18	T_{MULT}		2.40	2.76	ns, max
Input to Pin17	T_{MULT}		2.28	2.62	ns, max
Input to Pin16	T_{MULT}		2.17	2.49	ns, max
Input to Pin15	T_{MULT}		2.06	2.36	ns, max
Input to Pin14	T_{MULT}		1.94	2.23	ns, max
Input to Pin13	T_{MULT}		1.83	2.10	ns, max
Input to Pin12	T_{MULT}		1.71	1.97	ns, max
Input to Pin11	T_{MULT}		1.60	1.84	ns, max
Input to Pin10	T_{MULT}		1.49	1.71	ns, max
Input to Pin9	T_{MULT}		1.37	1.58	ns, max
Input to Pin8	T_{MULT}		1.26	1.45	ns, max
Input to Pin7	T_{MULT}		1.14	1.31	ns, max
Input to Pin6	T_{MULT}		1.03	1.18	ns, max
Input to Pin5	T_{MULT}		0.92	1.05	ns, max
Input to Pin4	T_{MULT}		0.80	0.92	ns, max
Input to Pin3	T_{MULT}		0.69	0.79	ns, max
Input to Pin2	T_{MULT}		0.57	0.66	ns, max
Input to Pin1	T_{MULT}		0.46	0.53	ns, max
Input to Pin0	T_{MULT}		0.35	0.40	ns, max

Block SelectRAM Switching Characteristics

Table 23: **Block SelectRAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}		3.01	3.46	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}		0.32/ 0.00	0.36/ 0.00	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}		0.32/ 0.00	0.36/ 0.00	ns, min
EN input	T_{BECK}/T_{BCKE}		1.04/ 0.00	1.20/ 0.00	ns, min
RST input	T_{BRCK}/T_{BCKR}		1.44/ 0.00	1.65/ 0.00	ns, min
WEN input	T_{BWCK}/T_{BCKW}		0.63/ 0.30	0.72/ 0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}		1.51	1.74	ns, min
Minimum Pulse Width, Low	T_{BPWL}		1.51	1.74	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 24: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
IN input to OUT output	T_{IO}		0.25	0.29	ns, max
TRI input to OUT output high-impedance	T_{OFF}		0.48	0.55	ns, max
TRI input to valid data on OUT output	T_{ON}		0.48	0.55	ns, max

JTAG Test Access Port Switching Characteristics

Table 25: **JTAG Test Access Port Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
TMS and TDI Setup times before TCK	T_{TAPTK}				ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}				ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}				ns, max
Maximum TCK clock frequency	F_{TCK}				MHz, max

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM

Table 26: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 11.	$T_{ICKOFDCM}$					ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 16 and Table 17.
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 27: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 11.	T_{ICKOF}	2V1000		5.20	5.98	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 16 and Table 17.
3. DCM output jitter is already included in the timing calculation.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *With* DCM

Table 28: **Global Clock Set-Up and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.						
No Delay Global Clock and IFF	T_{PSDCM}/T_{PHDCM}					ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *Without* DCM

Table 29: **Global Clock Set-Up and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.						
Full Delay Global Clock and IFF	T_{PSFD}/T_{PHFD}	2V1000		1.8/0.0	2.1/0.0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DCM Timing Parameters

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605; all devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 30: **Operating Frequency Ranges**

Description	Symbol	Constraints	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Output Clocks (Low Frequency Mode)									
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF				24	210	24	180	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF				48	420	48	360	MHz
CLKDV	CLKOUT_FREQ_DV_LF				1.5	140	1.5	120	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF				24	240	24	200	MHz
Input Clocks (Low Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_FREQ_DLL_LF				24	210	24	180	MHz
CLKIN (using CLKFX outputs)	CLKIN_FREQ_FX_LF				12	240	12	200	MHz
PSCLK	PSCLK_FREQ_LF				0.01	210	0.01	180	MHz
Output Clocks (High Frequency Mode)									
CLK0, CLK180	CLKOUT_FREQ_1X_HF				48	420	48	360	MHz
CLKDV	CLKOUT_FREQ_DV_HF				3	280	3	240	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF				160	320	160	270	MHz
Input Clocks (High Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_FREQ_DLL_HF				48	420	48	360	MHz
CLKIN (using CLKFX outputs)	CLKIN_FREQ_FX_HF				32	320	32	270	MHz
PSCLK	PSCLK_FREQ_HF				0.01	420	0.01	365	MHz

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Input Clock Tolerances

Table 31: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/high Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz			25.00		25.00		ns
CLKIN[2]	CLKIN_PULSE	1 - 10 MHz			25.00		25.00		ns
		10 - 25 MHz			10.00		10.00		ns
		25 - 50 MHz			5.00		5.00		ns
		50 - 100 MHz			3.00		3.00		ns
		100 - 150 MHz			2.40		2.40		ns
		150 - 200 MHz			2.00		2.00		ns
		200 - 250 MHz			1.80		1.80		ns
		250 - 300 MHz			1.50		1.50		ns
		300 - 350 MHz			1.30		1.30		ns
		350 - 400 MHz			1.15		1.15		ns
		> 400 MHz			1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_CYC_JITT_DLL_LF					±300		±300	ps
CLKIN (using CLKFX outputs)	CLKIN_CYC_JITT_FX_LF					±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_CYC_JITT_DLL_HF					±150		±150	ps
CLKIN (using CLKFX outputs)	CLKIN_CYC_JITT_FX_HF					±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_PER_JITT_DLL_LF					±1.00		±1.00	ns
CLKIN (using CLKFX outputs)	CLKIN_PER_JITT_FX_LF					±1.00		±1.00	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_PER_JITT_DLL_HF					±1.00		±1.00	ns
CLKIN (using CLKFX outputs)	CLKIN_PER_JITT_FX_HF					±1.00		±1.00	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT					±1.00		±1.00	ns

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Output Clock Jitter

Table 32: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Clock Synthesis Period Jitter									
CLK0	CLKOUT_PER_JITT_0					±100		±100	ps
CLK90	CLKOUT_PER_JITT_90					±150		±150	ps
CLK180	CLKOUT_PER_JITT_180					±150		±150	ps
CLK270	CLKOUT_PER_JITT_270					±150		±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X					±200		±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1					±150		±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2					±300		±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX								ps

Output Clock Phase Alignment

Table 33: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Phase Offset Between CLKIN and CLKFB									
CLKIN/CLKFB	CLKIN_CLKFB_PHASE					±100		±100	ps
Phase Offset Between Any DCM Outputs									
All CLK* outputs	CLKOUT_PHASE					±140		±140	ps
Duty Cycle Precision									
DLL outputs[1]	CLKOUT_DUTY_CYCLE_DLL					±150		±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX					±100		±100	ps

Miscellaneous Timing Parameters

Table 34: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Time Required to Achieve LOCK									
Using DLL outputs[1]	LOCK_DLL								
		> 60MHz				20		20	us
		50 - 60 MHz				25		25	us
		40 - 50 MHz				50		50	us
		30 - 40 MHz				90		90	us
		24 - 30 MHz				120		120	us
Using CLKFX outputs	LOCK_FX				10 us	10	10 us	10	ms
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT					50		50	us
Fine Phase Shifting									
Absolute shifting range	FINE_SHIFT_RANGE					10		10	ns
Delay Lines									
Tap delay resolution	DCM_TAP				40	50	40	50	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Parameter Cross-Reference

Table 35: **Parameter Cross-Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). Values were added and revised in tables in the following sections: • **Virtex-II Performance Characteristics** • **Virtex-II Switching Characteristics** • **DCM Timing Parameters** • Table 17, “Delay Measurement Methodology,” on page 15
04/23/01	1.5	• Updated values in the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections. • Added T_{REG32} symbol to Table 21. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- DS031-1, Virtex-II 1.5V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS031-2, Virtex-II 1.5V FPGAs: **Functional Description (Module 2)**
- DS031-3, Virtex-II 1.5V FPGAs: DC and Switching Characteristics (Module 3)
- DS031-4, Virtex-II 1.5V FPGAs: **Pinout Tables (Module 4)**

Virtex-II 1.5V Field-Programmable Gate Arrays

DS031-1 (v1.5) April 2, 2001

Advance Product Specification

Summary of Virtex®-II Features

- Industry First Platform FPGA Solution
- IP-Immersion™ Architecture
  - Densities from 40K to 10M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3.5 Mb of True Dual-Port™ RAM in 18-Kbit block SelectRAM resources
  - Up to 1.9 Mb of distributed SelectRAM resources
  - High-performance interfaces to external memory
    - 400 Mb/s DDR-SDRAM interface (Advance Data)
    - 400 Mb/s FCRAM interface (Advance Data)
    - 333 Mb/s QDR™-SRAM interface (Advance Data)
    - 600 Mb/s Sigma RAM interface (Advance Data)
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 122,880 internal registers / latches with Clock Enable
  - Up to 122,880 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
    - EMI reduction
  - 16 global clock multiplexer buffers
- Active Interconnect™ Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectI/O-Ultra™ Technology
  - Up to 1,108 user I/Os
  - 19 single-ended standards and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - XCITE™ Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X @ 133 MHz, PCI @ 66 MHz and 33 MHz compliance
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR Input and Output registers
  - Proprietary high-performance SelectLink™ Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance™ Series Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE1532 support
  - Partial reconfiguration
  - Unlimited re-programmability
  - Readback capability
- Power-Down Mode
- 0.15 µm 8-Layer Metal process with 0.12 µm high-speed transistors
- 1.5 V (V_{CCINT}) core power supply, dedicated 3.3 V V_{CCAUX} auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 compatible boundary-scan logic support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) packages in three standard fine pitches (0.80mm, 1.00mm, and 1.27mm)
- 100% factory tested

Table 1: **Virtex-II Field-Programmable Gate Array Family Members**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18-Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108
XC2V10000	10M	128 x 120	61,440	1,920	192	192	3,456	12	1,108

Notes:
1. See details in Table 2, “Maximum Number of User I/O Pads”.

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15µm / 0.12µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 12 members, ranging from 40K to 10M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80mm, 1.00mm, and 1.27mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-Chip construction offers the combination of high pin count with high thermal capacity.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: **Maximum Number of User I/O Pads**

Device	Wire-Bond	Flip-Chip
XC2V40	88	
XC2V80	120	
XC2V250	200	
XC2V500	264	
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	456	624
XC2V3000	516	720
XC2V4000		912
XC2V6000		1,104
XC2V8000		1,108
XC2V10000		1,108

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

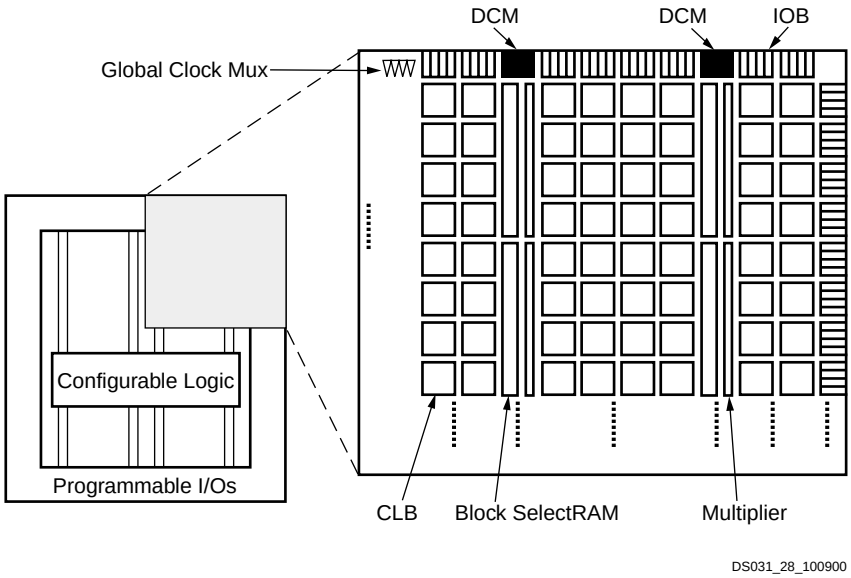


Figure 1: **Virtex-II Architecture Overview**

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18-Kbit storage elements of True Dual-Port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse and fine-grained clock phase shifting, and electromagnetic interference (EMI) reduction.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bi-directional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3 V, 2.5 V, 1.8 V, and 1.5 V)
- PCI-X at 133 MHz, PCI (3.3 V at 33 MHz and 66 MHz)
- GTL and GTLP

- HSTL (Class I, II, III, and IV)
- SSTL (3.3 V and 2.5 V, Class I and II)
- AGP-2X

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bits, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 3.

Table 3: **Dual-Port And Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

Up to 12 DCM blocks are available. To generate de-skewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to any M/D ratio of the input clock frequency, where M and D are two integers. For the exact timing parameters, see **Virtex™-II Electrical Characteristics**.

Virtex-II devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each global clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM block is able to drive up to four of the 16 global clock MUX buffers.

Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column as well as massive secondary and local routing resources provide fast interconnect. Virtex-II buffered interconnects are relatively unaffected by net fanout and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II devices that complies with IEEE standards 1149.1 - 1993 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II devices are configured by loading data into internal configuration memory, using the following five modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops/latches, distributed SelectRAM, and block SelectRAM memory resources can be read back. This capability is useful for real-time debugging.

The Integrated Logic Analyzer (ILA) core and software provides a complete solution for accessing and verifying Virtex-II devices.

Power-Down Mode

Activated by the power-down input, this mode reduces supply current and retains the Virtex-II device configuration.

Virtex-II Device/Package Combinations and Maximum I/O

Wire-bond and flip-chip packages are available. Table 4 and Table 5 show the maximum possible number of user I/Os in wire-bond and flip-chip packages, respectively. Table 6 shows the number of available user I/Os for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD) and VBATT.

Table 4: **Wire-Bond Packages Information**

Package	CS144	FG256	FG456	FG676	BG575	BG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Table 5: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 6: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)**

Package	Available I/Os											
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000	XC2V 10000
CS144	88	92	92									
FG256	88	120	172	172	172							
FG456			200	264	324							
FG676						392	456	484				
FF896					432	528	624					
FF1152								720	824	824	824	824
FF1517									912	1,104	1,108	1,108
BG575					328	392	408					
BG728							456	516				
BF957							624	684	684	684	684	684

Notes:
1. All devices in a particular package are pin-out (footprint) compatible. In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages.

Virtex-II Ordering Information

Virtex-II ordering information is shown in Figure 2

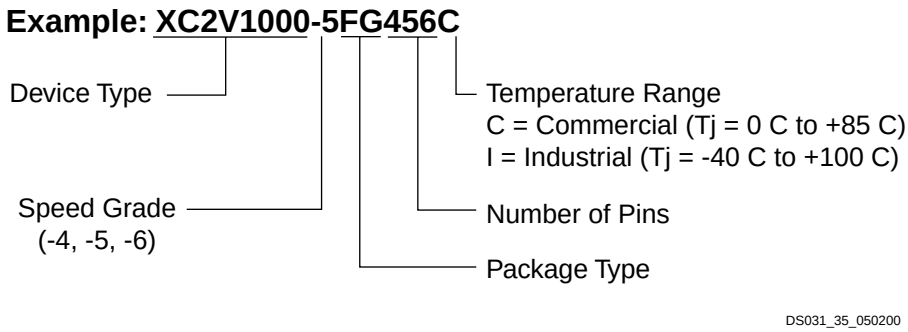


Figure 2: **Virtex-II Ordering Information**

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- DS031-1, Virtex-II 1.5V FPGAs: Introduction and Ordering Information (Module 1)
- DS031-2, Virtex-II 1.5V FPGAs: **Functional Description (Module 2)**
- DS031-3, Virtex-II 1.5V FPGAs: **DC and Switching Characteristics (Module 3)**
- DS031-4, Virtex-II 1.5V FPGAs: **Pinout Tables (Module 4)**

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 1.

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.

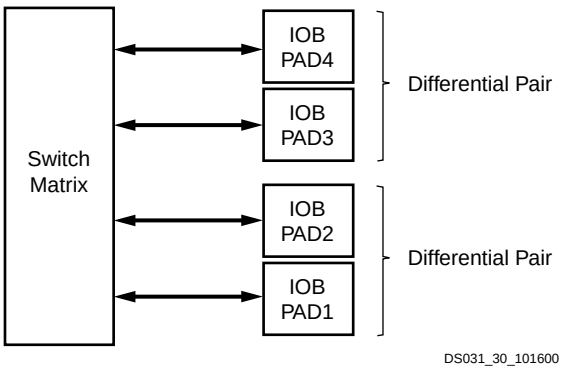


Figure 1: **Virtex-II Input/Output Tile**

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (V_{CCINT} = 1.5V), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see Table 1). An auxiliary supply voltage (V_{CCAUX} = 3.3 V) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see **DC Input and Output Levels**.

Table 1: **Supported Single-Ended I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
LVCMOS15	1.5	1.5	N/A	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
PCI-X	3.3	3.3	N/A	N/A
GTL	Note 1	Note 1	0.8	1.2
GTLP	Note 1	Note 1	1.0	1.5
HSTL_I	1.5	N/A	0.75	0.75
HSTL_II	1.5	N/A	0.75	0.75
HSTL_III	1.5	N/A	0.9	1.5
HSTL_IV	1.5	N/A	0.9	1.5
SSTL2_I	2.5	N/A	1.25	1.25
SSTL2_II	2.5	N/A	1.25	1.25
SSTL3_I	3.3	N/A	1.5	1.5
SSTL3_II	3.3	N/A	1.5	1.5
AGP-2X/AGP	3.3	N/A	1.32	N/A

Notes:
1. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad.

Table 2: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LVPECL_33	3.3	N/A	N/A	V_{CCO} – 1.025 to V_{CCO} – 1.64
LDT_25	2.5	N/A	N/A	0.430 - 0.670
LVDS_33	3.3	N/A	N/A	0.250 - 0.400
LVDS_25	2.5	N/A	N/A	0.250 - 0.400
LVDSEXT_33	3.3	N/A	N/A	0.330 - 0.700
LVDSEXT_25	2.5	N/A	N/A	0.330 - 0.700
BLVDS_25	2.5	N/A	N/A	0.250 - 0.450
ULVDS_25	2.5	N/A	N/A	0.430 - 0.670

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. The IOBs are not compatible or compliant with 5 V I/O standards (not 5 V tolerant).

Table 3 lists supported I/O standards with Digitally Controlled Impedance. See **Digitally Controlled Impedance (DCI)**, page 6.

Table 3: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/A	Series
LVDCI_DV2_33(1)	3.3	3.3	N/A	Series
LVDCI_25(1)	2.5	2.5	N/A	Series
LVDCI_DV2_25(1)	2.5	2.5	N/A	Series
LVDCI_18(1)	1.8	1.8	N/A	Series
LVDCI_DV2_18(1)	1.8	1.8	N/A	Series
LVDCI_15(1)	1.5	1.5	N/A	Series
LVDCI_DV2_15(1)	1.5	1.5	N/A	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL3_I_DCI(2)	3.3	3.3	1.5	Split
SSTL3_II_DCI(2)	3.3	3.3	1.5	Split

Notes:
1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.

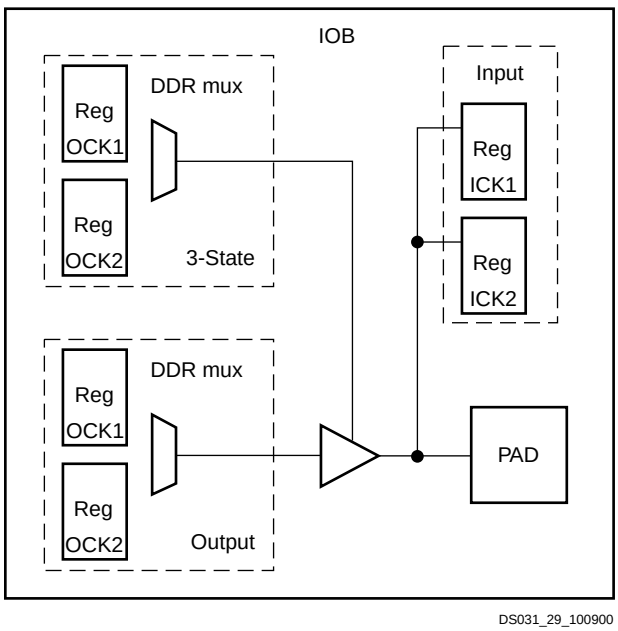


Figure 2: **Virtex-II IOB Block**

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 3. There are two input, output, and 3-state data signals, each being alternately clocked out.

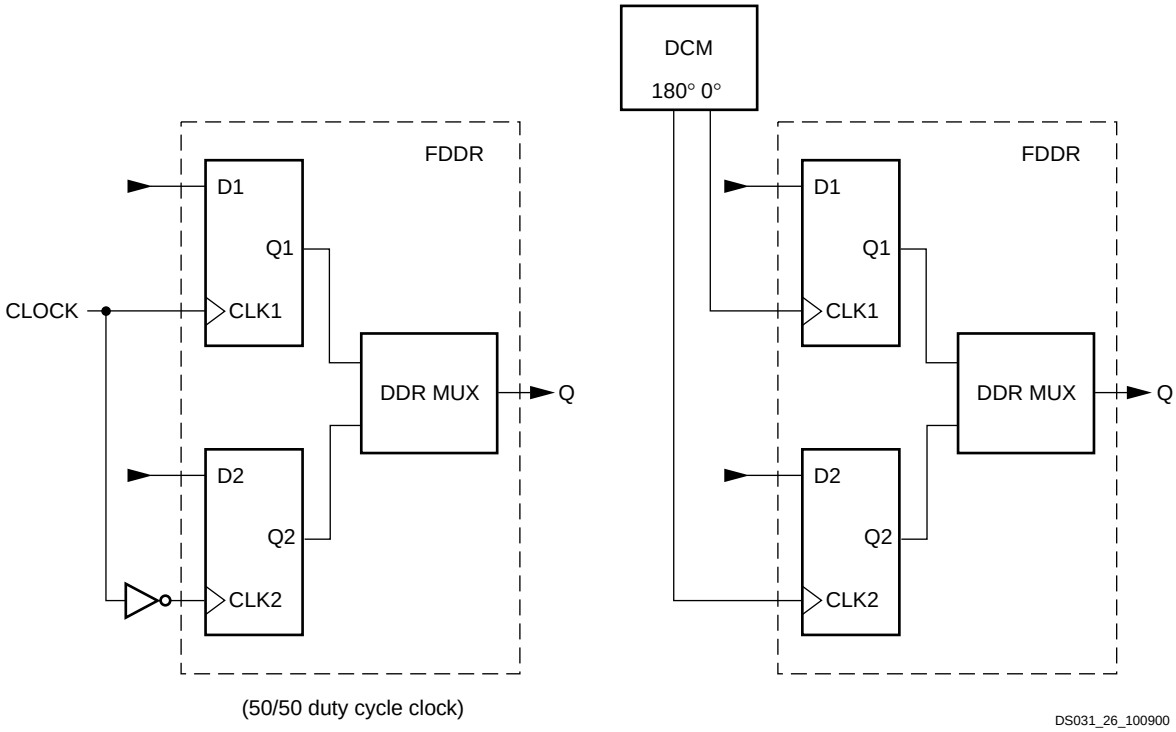


Figure 3: **Double Data Rate Registers**

This DDR mechanism can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

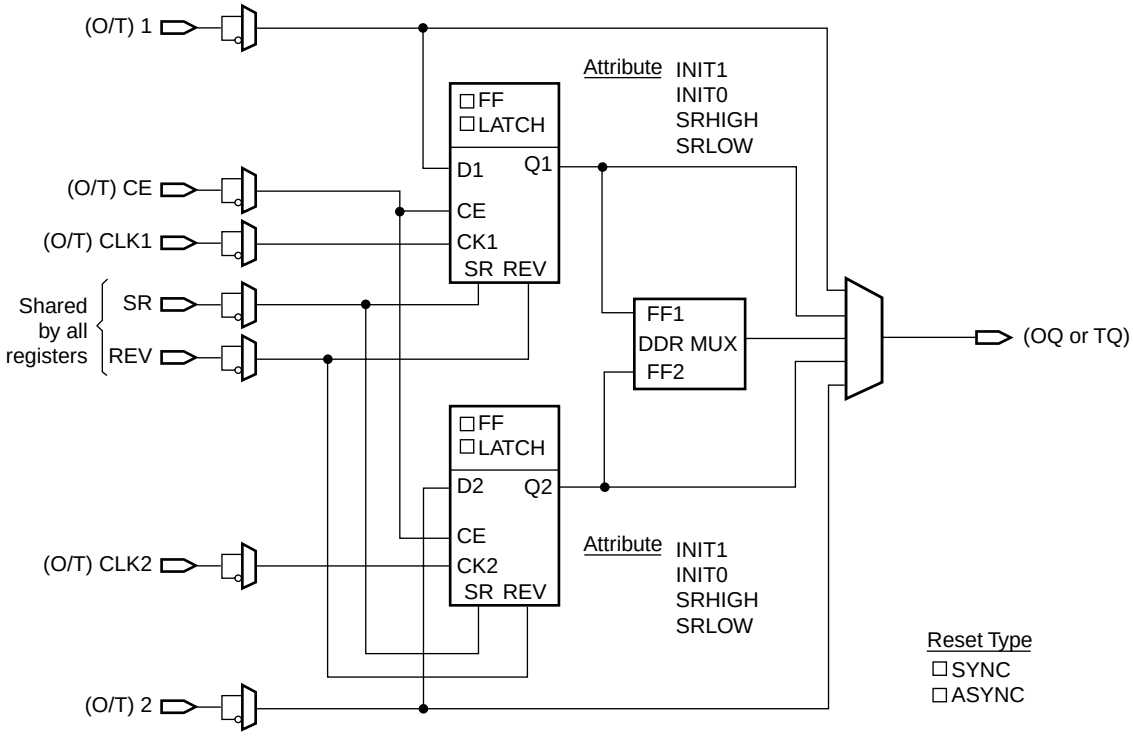


Figure 4: **Register / Latch Configuration in an IOB Block**

Input/Output Individual Options

Each device pad has optional pull-up, pull-down, and weak-keeper in LVTTL and LVCMOS SelectI/O configurations, as illustrated in Figure 5. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 KΩ, which is the specification for V_{CCO} when operating at 3.3 V (from 3.0 to 3.6 V only).

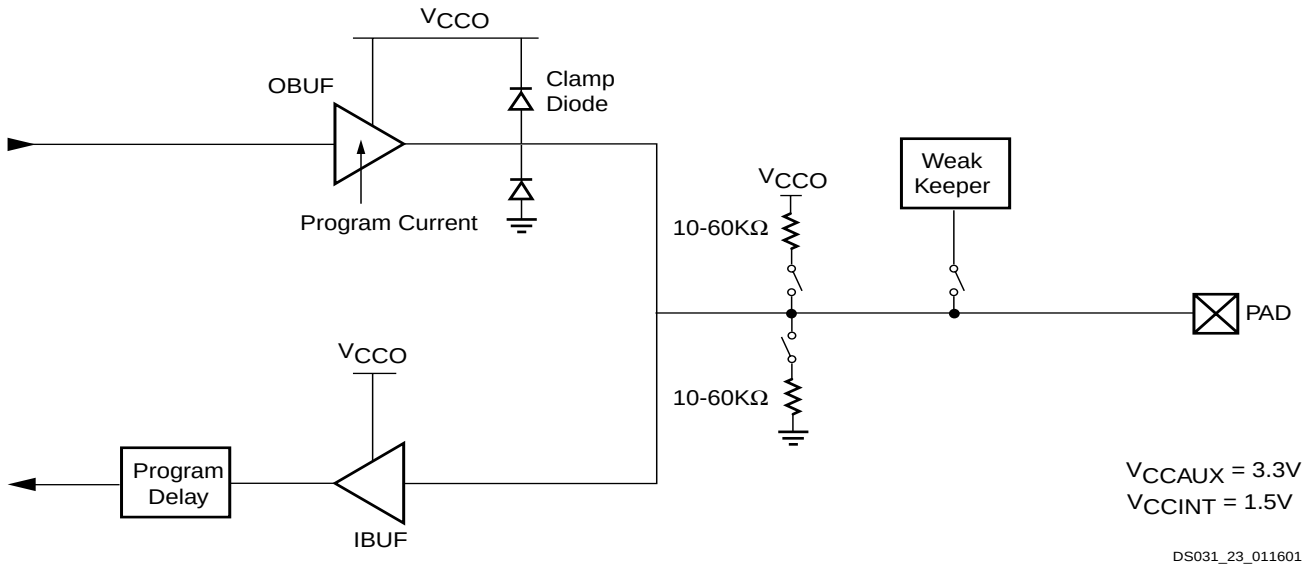


Figure 5: **LVTTL, LVCMOS or PCI SelectI/O Standards**

The optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintain-

ing a valid logic level in this way eliminates bus chatter; pull-up or pull-down override the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVCMOS SelectI/O standards (see Table 4). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

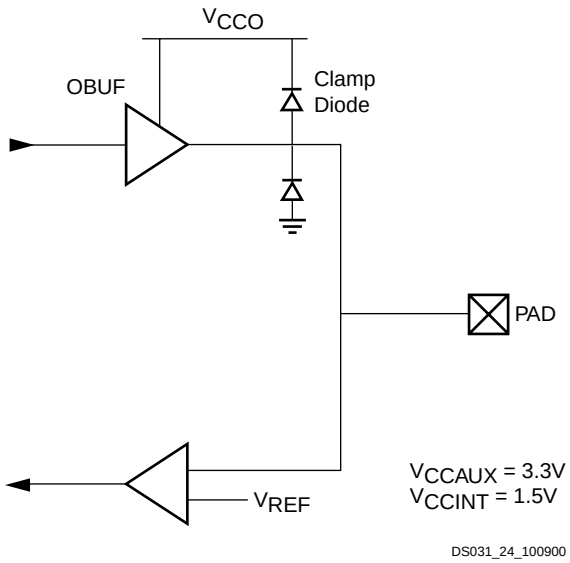


Figure 6: **SSTL or HSTL SelectI/O Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible boundary scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be con-

nected to the same voltage. This voltage is determined by the output standards in use.

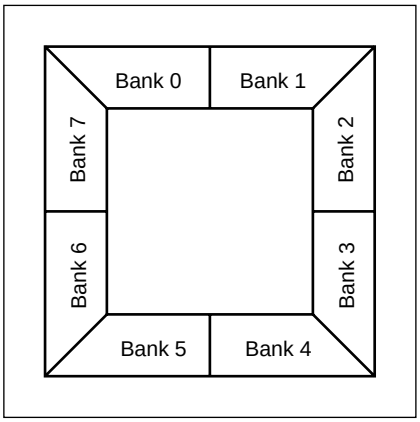


Figure 7: **Virtex-II I/O Banks: Top View for Wire-Bond Packages (CS, FG, & BG)**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 5. GTL and GTLP appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

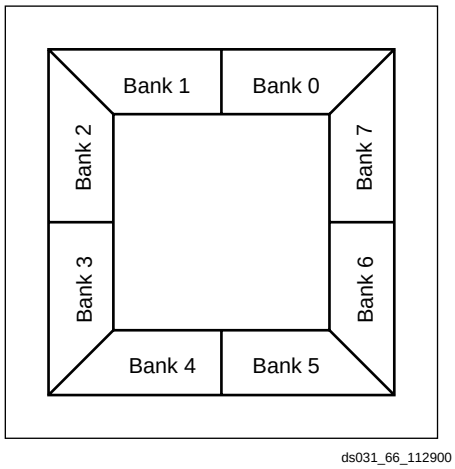


Figure 8: **Virtex-II I/O Banks: Top View for Flip-Chip Packages (FF & BF)**

V_{REF} pins within a bank are interconnected internally, and consequently only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

Table 5: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 (I & II), AGP-2X, LVDS_33, LVDSEXT_33, LVCMOS33, LVDCI_33, LVDCI_DV2_33, SSTL3_DCI (I & II), BLVDS, LVPECL, GTL, GTLP
2.5 V	SSTL2 (I & II), LVCMOS25, GTL, GTLP, LVDS_25, LVDSEXT_25, LVDCI_25, LVDCI_DV2_25, SSTL2_DCI (I & II), LDT, ULVDS, BLVDS
1.8 V	LVCMOS18, GTL, GTLP, LVDCI_18, LVDCI_DV2_18
1.5 V	HSTL (I, II, III, & IV), LVCMOS15, GTL, GTLP, LVDCI_15, LVDCI_DV2_15, GTLP_DCI, HSTL_DCI (I,II, III & IV)
1.2V	GTL_DCI

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to the V_{CCO} voltage to permit migration to a larger device.

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II DCI provides controlled impedance drivers and on-chip termination for single-ended I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins

on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

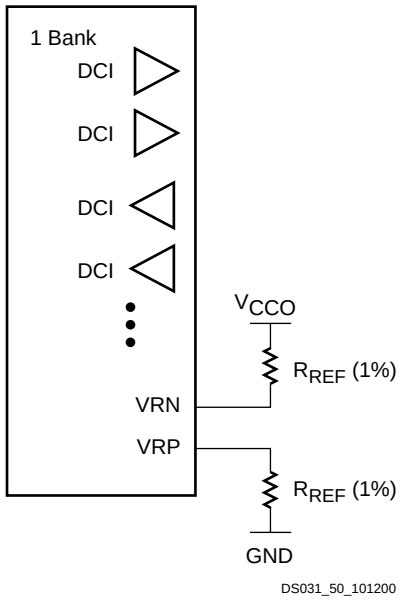


Figure 9: **DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of the resistor is specified by the standard (typically 50 Ω). When used with a controlled impedance driver, the resistor sets the output impedance of the driver within the specified range (25 Ω to 150 Ω). The resistors connected to VRN and VRP do not need to be the same value. 1% resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistor, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

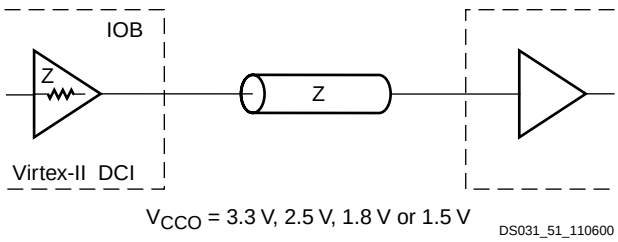


Figure 10: **Internal Series Termination**

Table 6: **SelectI/O Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel Termination)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 lists the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 3. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 7: **SelectI/O Buffers With On-Chip Parallel Termination**

I/O Standard	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI(1)
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI(1)
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI(1)
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI(1)
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:
1. SSTL Compatible

For further details, see the *Virtex-II User Guide.*

Figure 11 provides examples illustrating the use of the HSTL_IV_DCI, HSTL_II_DCI, and SSTL2_DCI I/O standards.

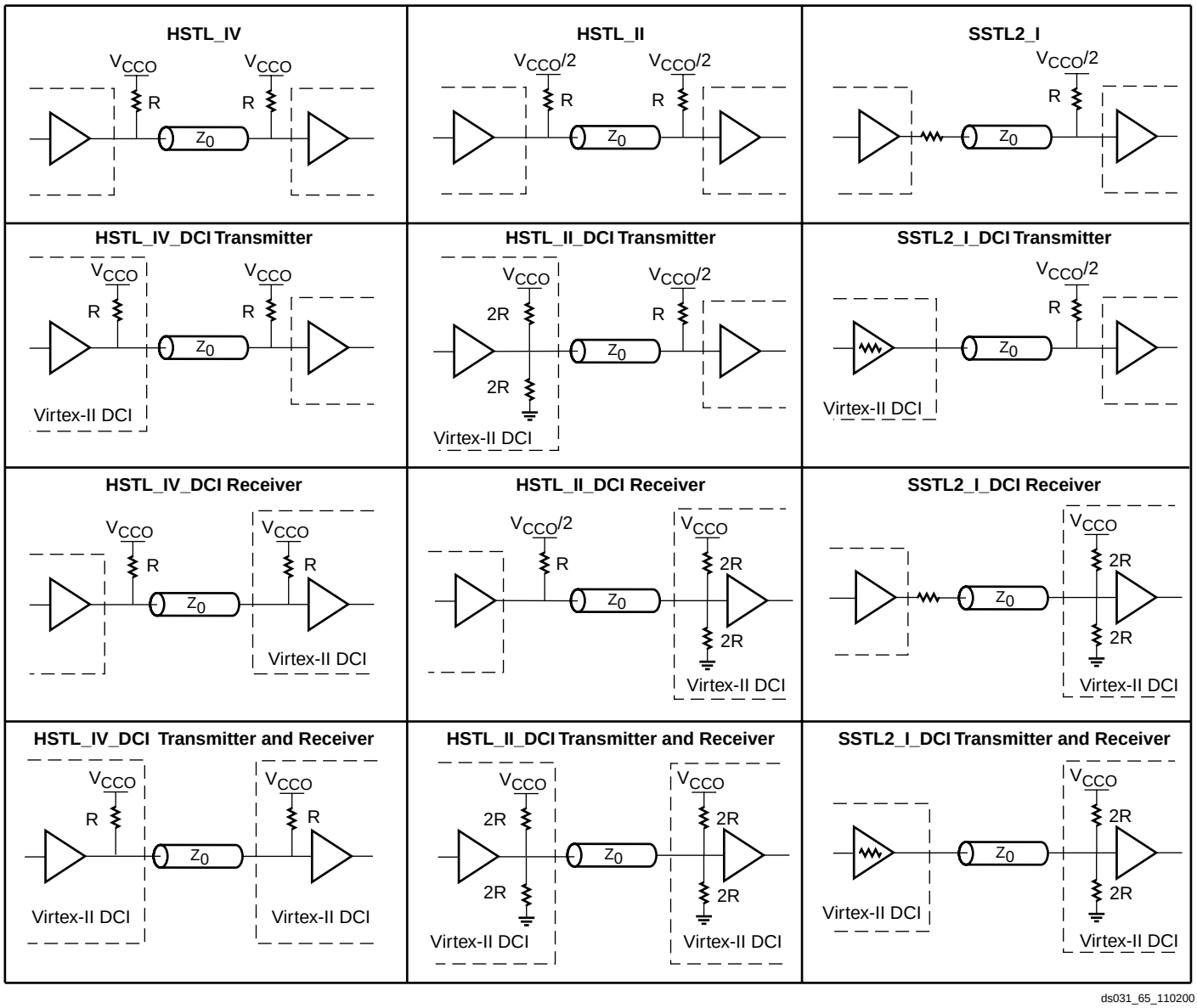


Figure 11: **DCI Usage Examples**

Configurable Logic Blocks (CLBs)

The Virtex-II configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 12. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

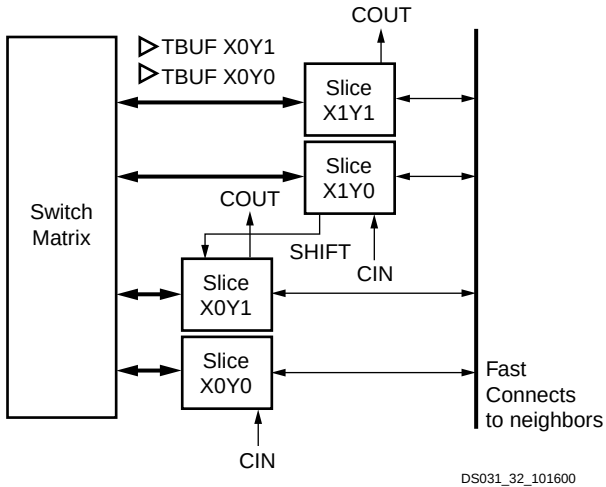


Figure 12: **Virtex-II CLB Element**

Slice Description

Introduction

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 13, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM memory, or a 16-bit variable-tap shift register element.

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 14 shows a more detailed view of a single slice.

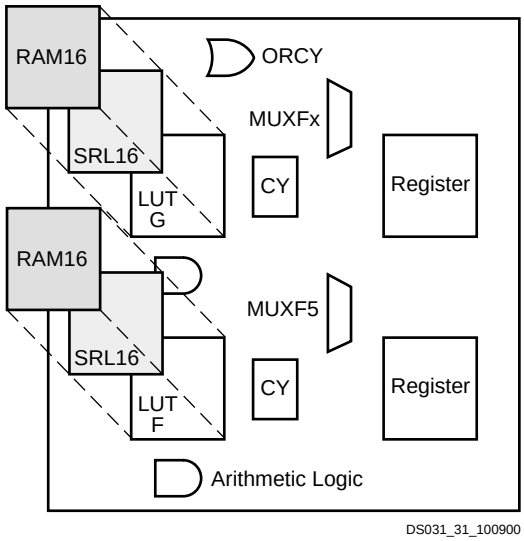


Figure 13: **Virtex-II Slice Configuration**

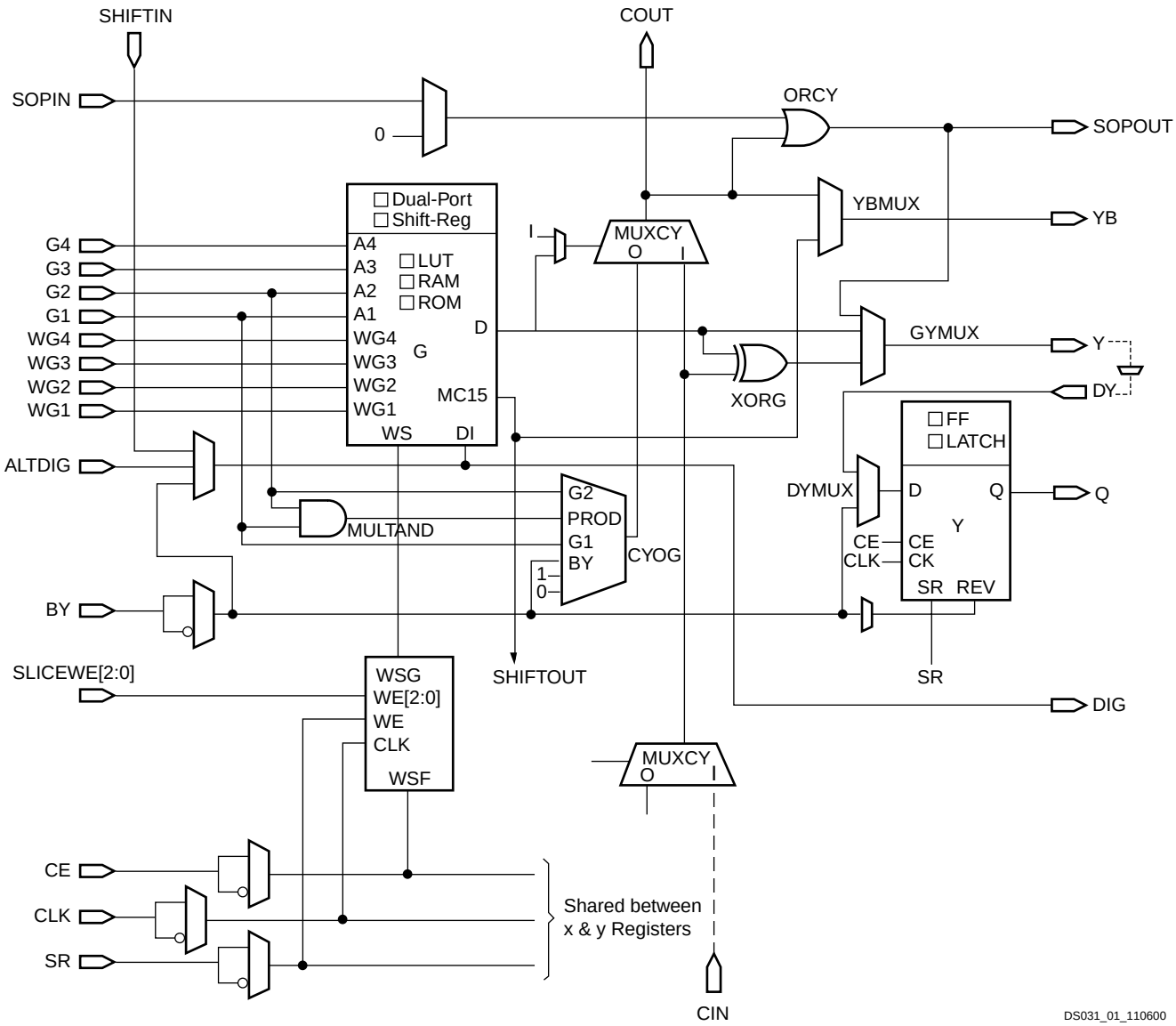


Figure 14: **Virtex-II Slice (Top Half)**

Configurations

Look-Up Table

Virtex-II function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 14).

In addition to the basic LUTs, the Virtex-II slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX are either MUXF6, MUXF7 or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexers to map any functions of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a Virtex-II slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic “1” when SR is asserted. SRLOW forces a logic “0”. When SR is used, a second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition. (See Figure 15.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

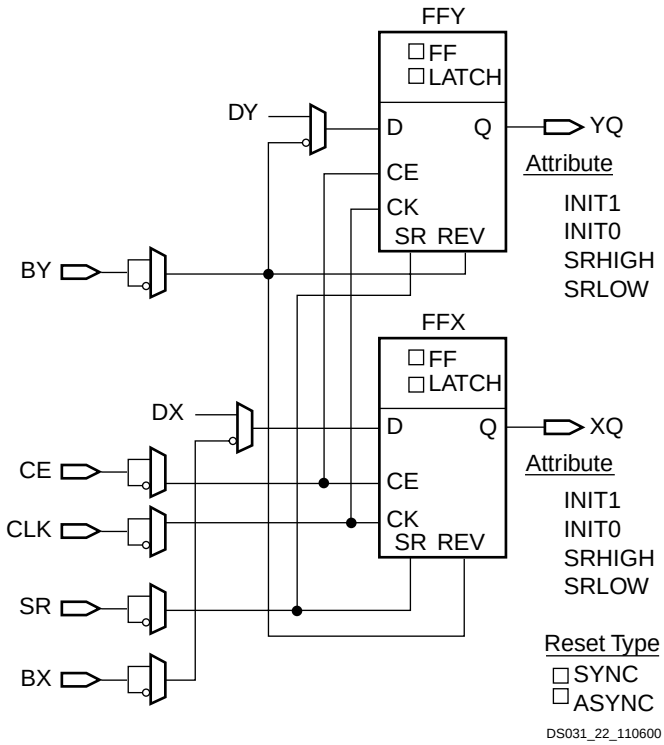


Figure 15: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies

high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 8 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 8: **Distributed SelectRAM Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Figure 16, Figure 17, and Figure 18 illustrate various example configurations.

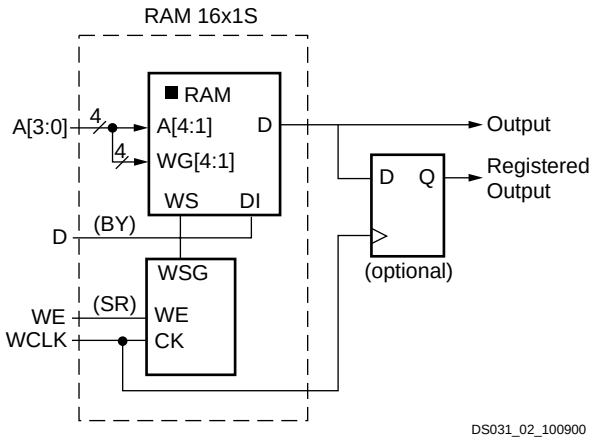


Figure 16: **Distributed SelectRAM (RAM16x1S)**

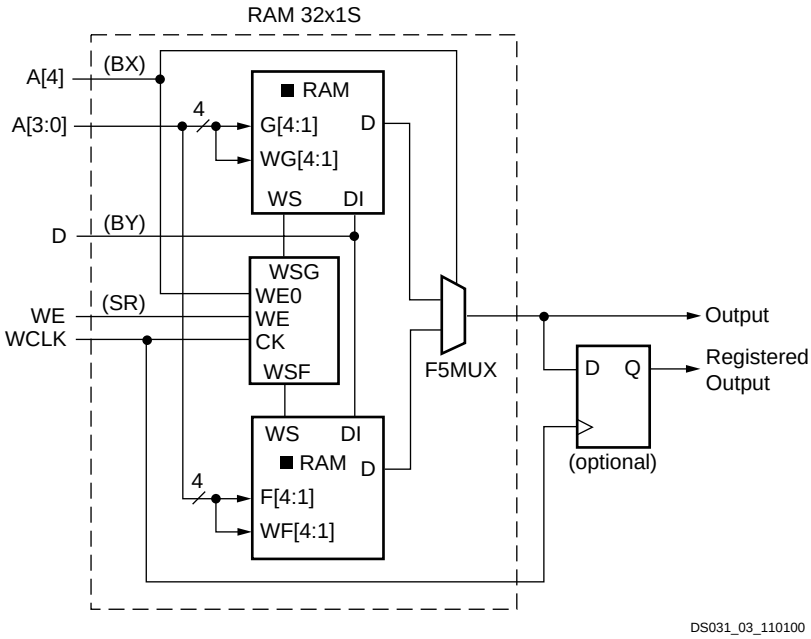


Figure 17: **Single-Port Distributed SelectRAM (RAM32x1S)**

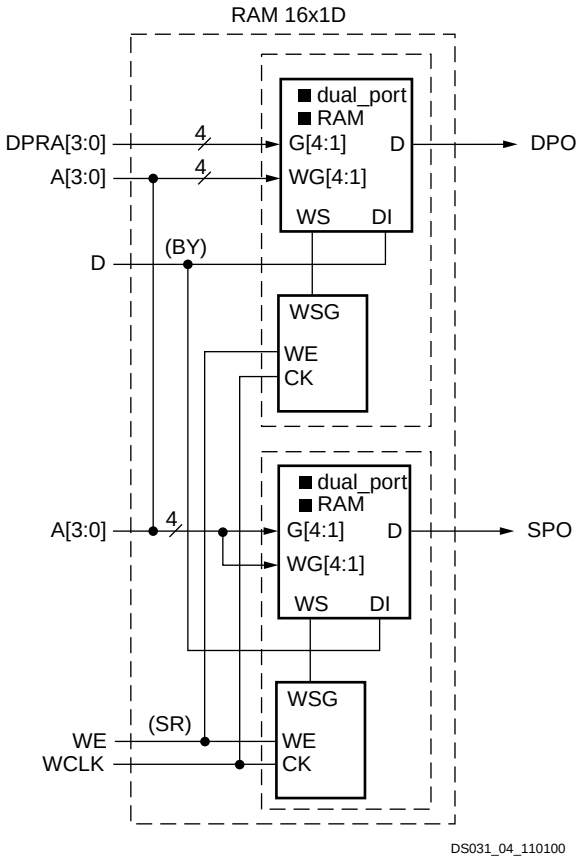


Figure 18: **Dual-Port Distributed SelectRAM (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 9 shows the number of LUTs occupied by each configuration.

Table 9: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 19. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

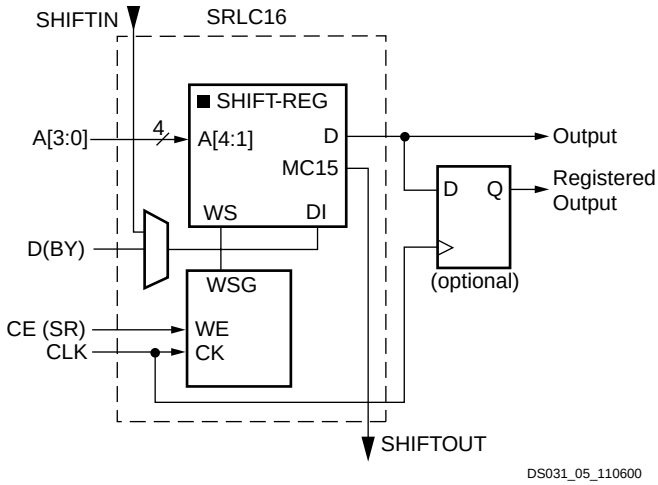


Figure 19: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 20.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

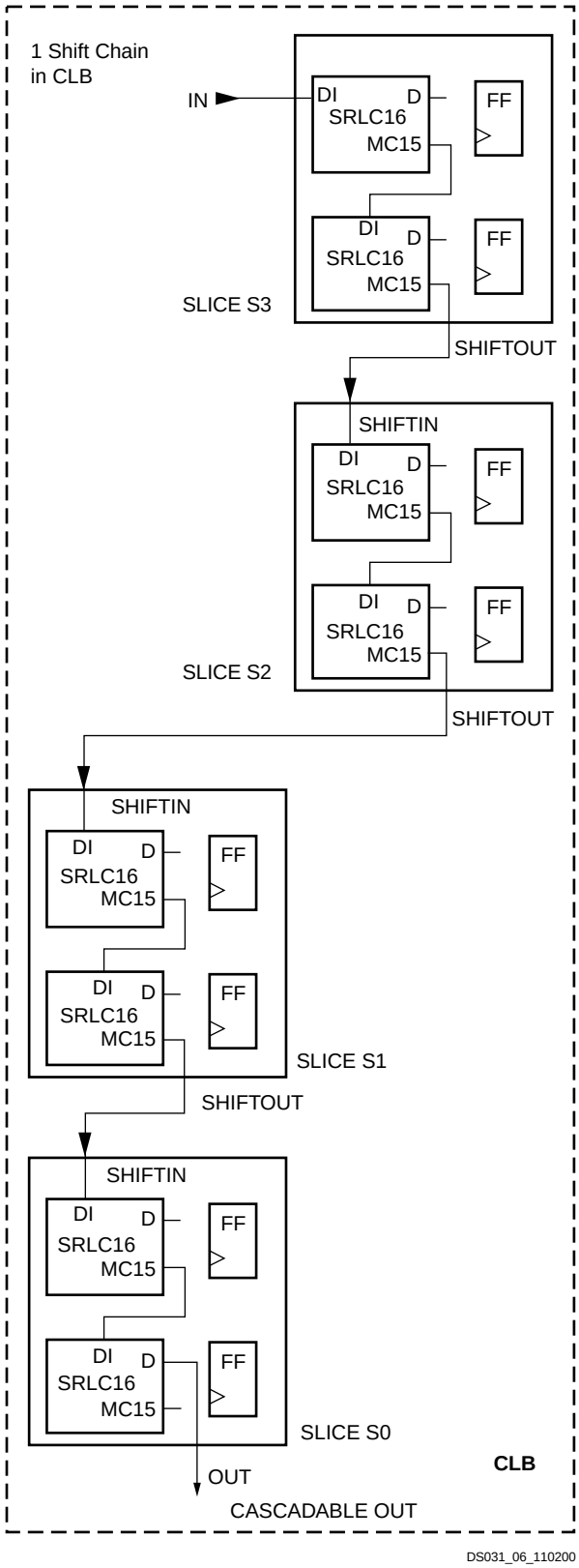


Figure 20: **Cascadable Shift Register**

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 21. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the Virtex-II *User Guide*. Any LUT can implement a 2:1 multiplexer.

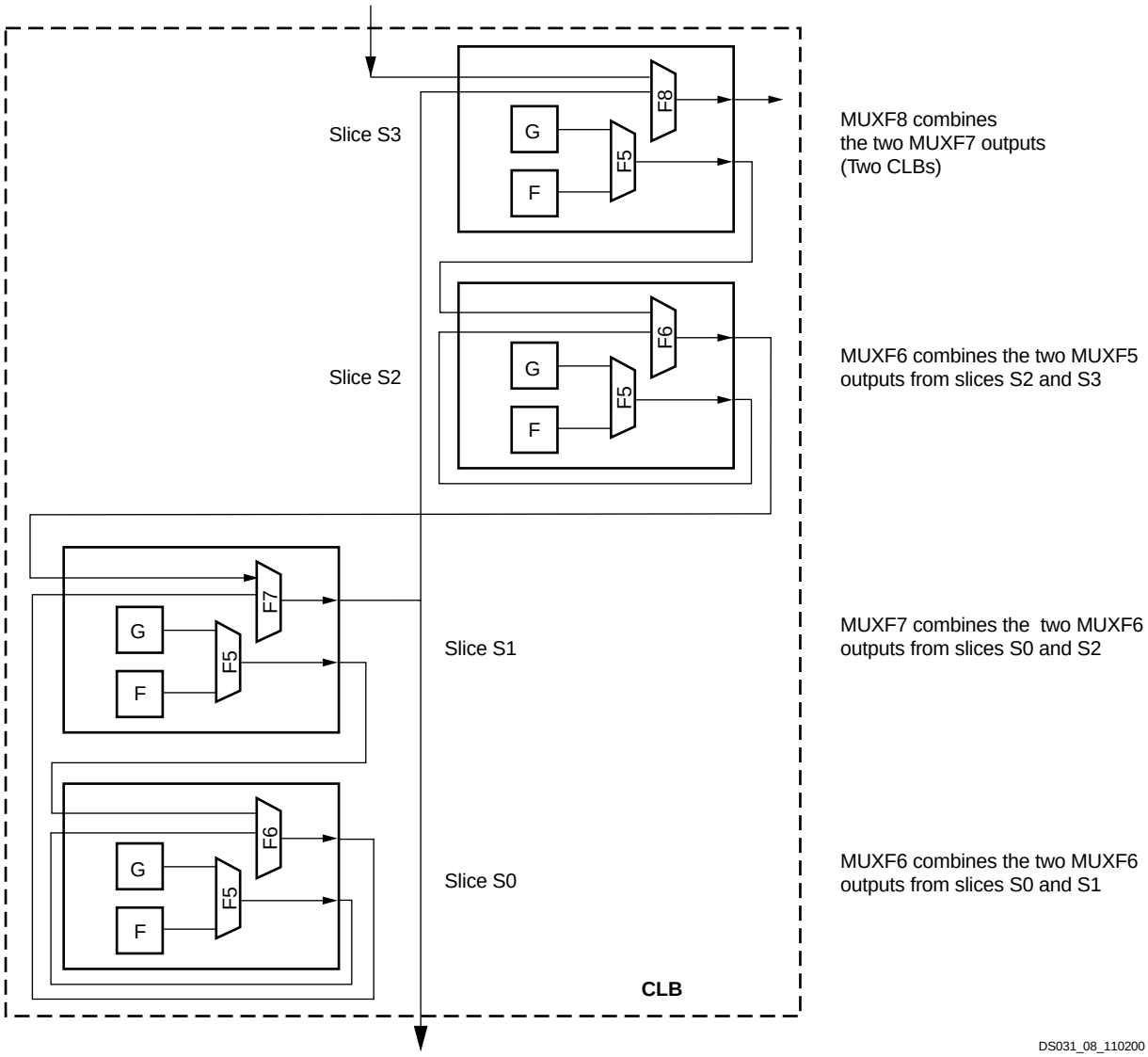


Figure 21: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 22.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

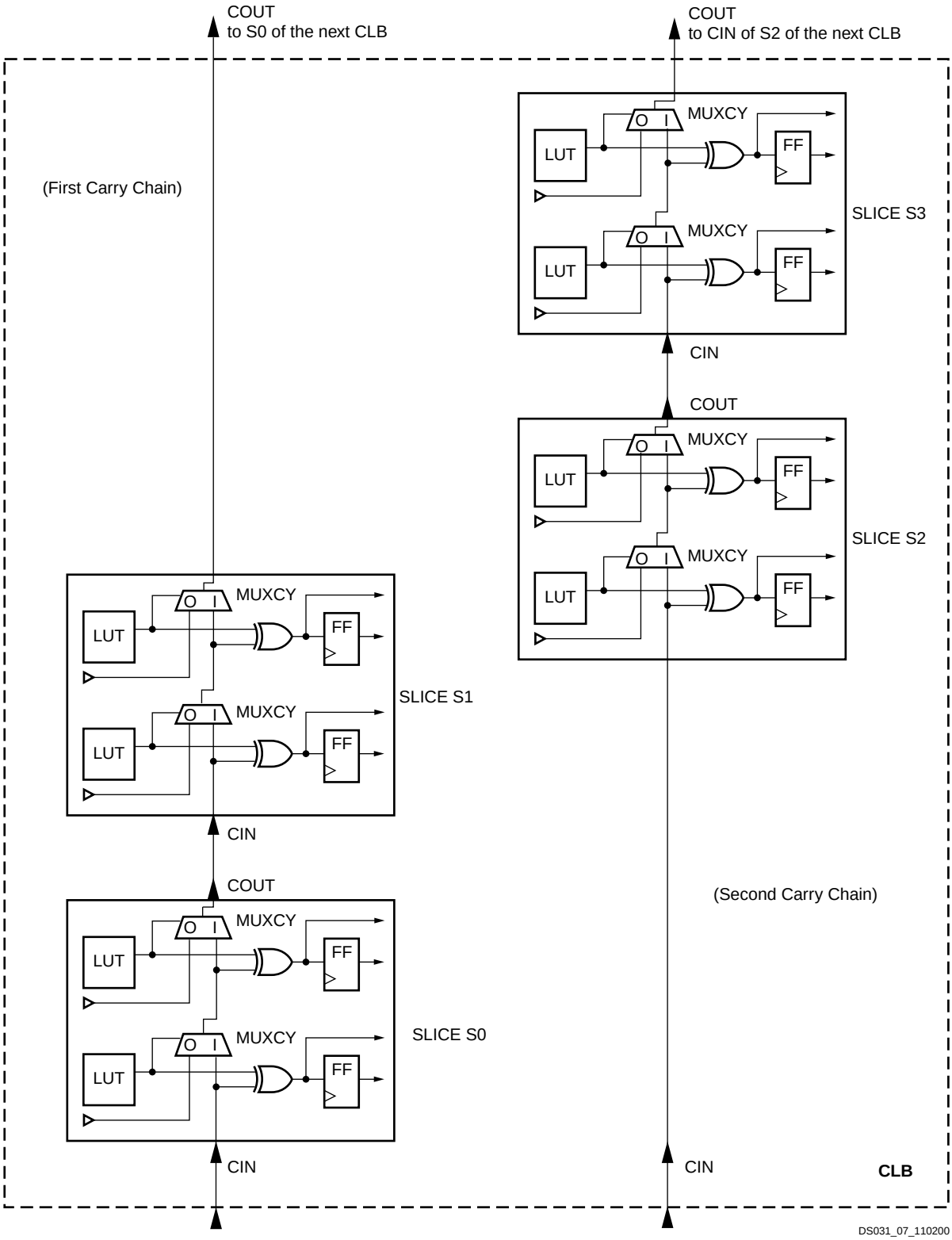


Figure 22: **Fast Carry Logic Path**

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 14) improves the efficiency of multiplier implementation.

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 23.

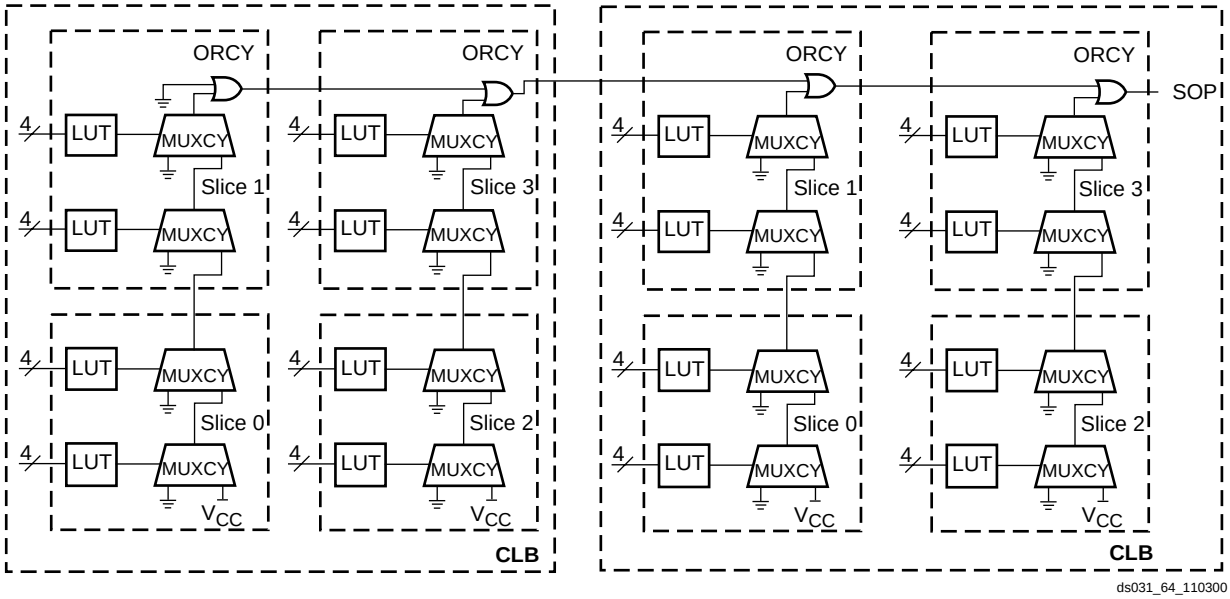


Figure 23: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 24 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

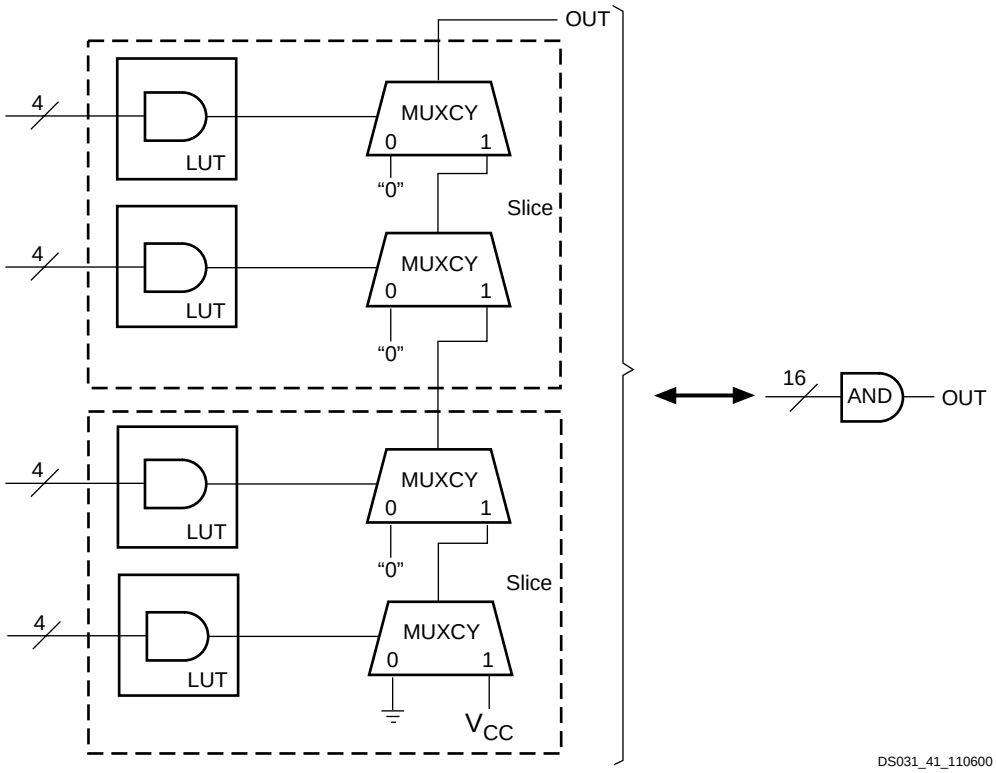


Figure 24: **Wide-Input AND Gate (12 Inputs)**

3-State Buffers

Introduction

Each Virtex-II CLB contains two 3-state drivers (TBUFs) that can drive on-chip busses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 25. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state busses.

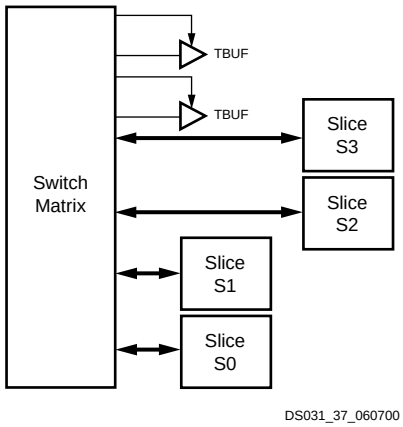


Figure 25: **Virtex-II 3-State Buffers**

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependant especially with larger devices.

Locations / Organization

Four horizontal routing resources per CLB are provided for on-chip 3-state busses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 26. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.

Number of 3-State Buffers

Table 10 shows the number of 3-state buffers available in each Virtex-II device. The number of 3-state buffers is twice the number of CLB elements.

Table 10: **Virtex-II 3-State Buffers**

Device	3-State Buffers per Row	Total Number of 3-State Buffers
XC2V40	16	128
XC2V80	16	256
XC2V250	32	768
XC2V500	48	1,536
XC2V1000	64	2,560
XC2V1500	80	3,840
XC2V2000	96	5,376
XC2V3000	112	7,168
XC2V4000	144	11,520
XC2V6000	176	16,896
XC2V8000	208	23,296
XC2V10000	240	30,720

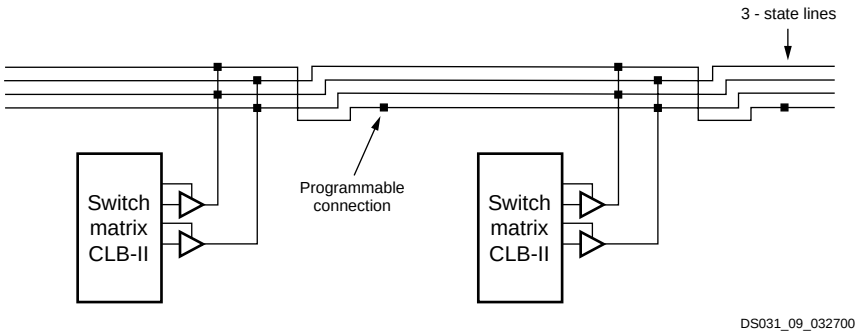


Figure 26: **3-State Buffer Connection to Horizontal Lines**

CLB/Slice Configurations

Table 11 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 12 shows the available resources in all CLBs.

Table 11: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 12: **Virtex-II Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2V40	8 x 8	256	516	8,192	516	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224
XC2V10000	128 x 120	61,440	122,880	1,966,080	122,880	240	256

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18-Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18-Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18-Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 13.

Table 13: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18-Kbit memory locations in any of the 2K x 9-bit,

1K x 18-bit, or 512 x 36-bit configurations and to 16-Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 27. Input data bus and output data bus widths are identical.

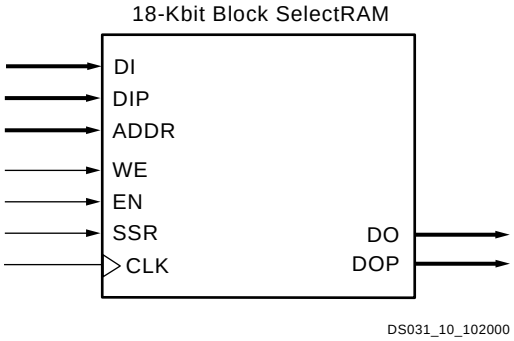


Figure 27: **18-Kbit Block SelectRAM Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18-Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 14 illustrates the different configurations available on ports A & B.

Table 14: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18-Kbit block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18-Kbit memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbits.

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 28. The two ports have independent inputs and outputs and are independently clocked.

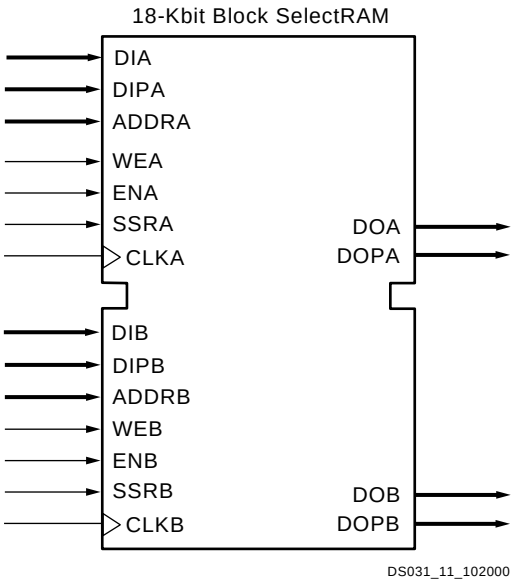


Figure 28: **18-Kbit Block SelectRAM in Dual-Port Mode**

Port Aspect Ratios

Table 15 shows the depth and the width aspect ratios for the 18-Kbit block SelectRAM. Virtex-II block SelectRAM also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

Table 15: **18-Kbit Block SelectRAM Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. There are three different options are available, each set by configuration:

1. “WRITE_FIRST”

   The “WRITE_FIRST” option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 29.

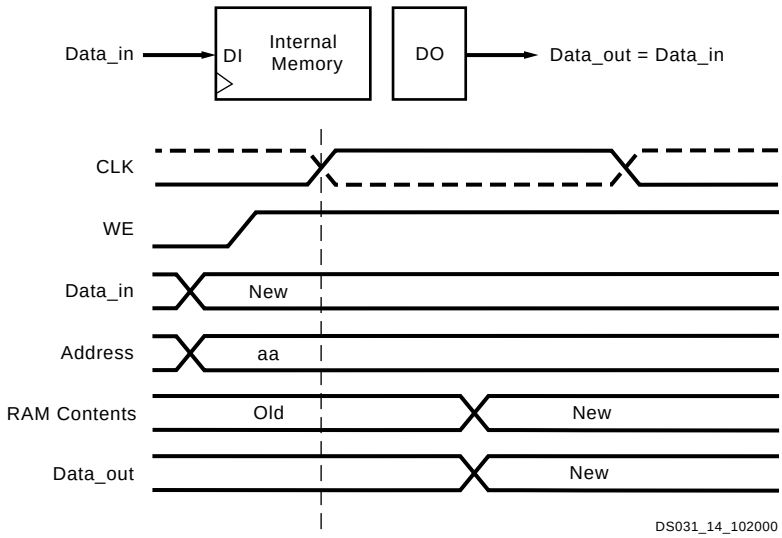


Figure 29: **WRITE_FIRST Mode**

2. “READ_FIRST”

The “READ_FIRST” option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 30.

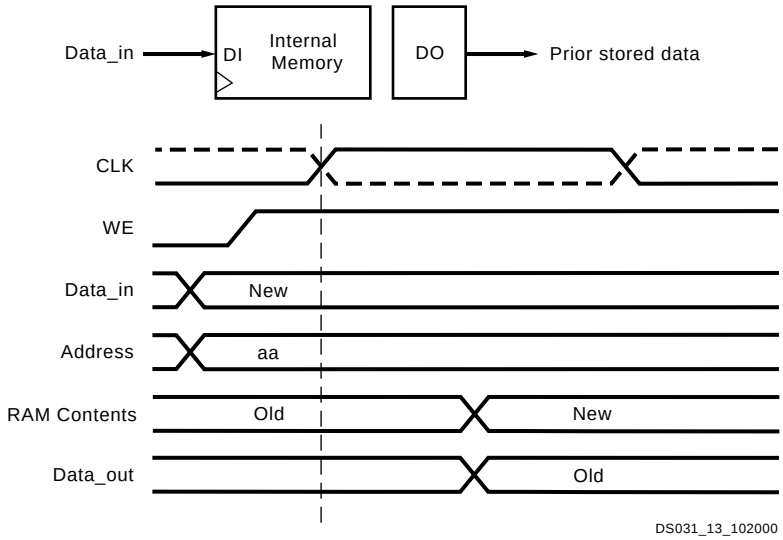


Figure 30: **READ_FIRST Mode**

3. “NO_CHANGE”

The “NO_CHANGE” option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as “NO_CHANGE”, only a read operation loads a new value in the output register DO, as shown in Figure 31.

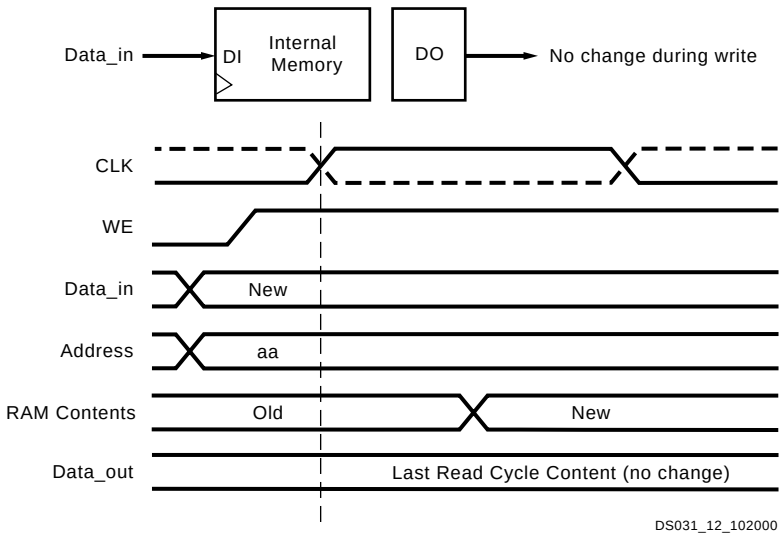


Figure 31: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 16. All control inputs including the clock have an optional inversion.

Table 16: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are organized in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the number of CLBs in a column divided by four. Column locations are shown in Table 17.

Table 17: **SelectRAM Memory Floor Plan**

Device	Columns	SelectRAM Blocks	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168
XC2V10000	6	32	192

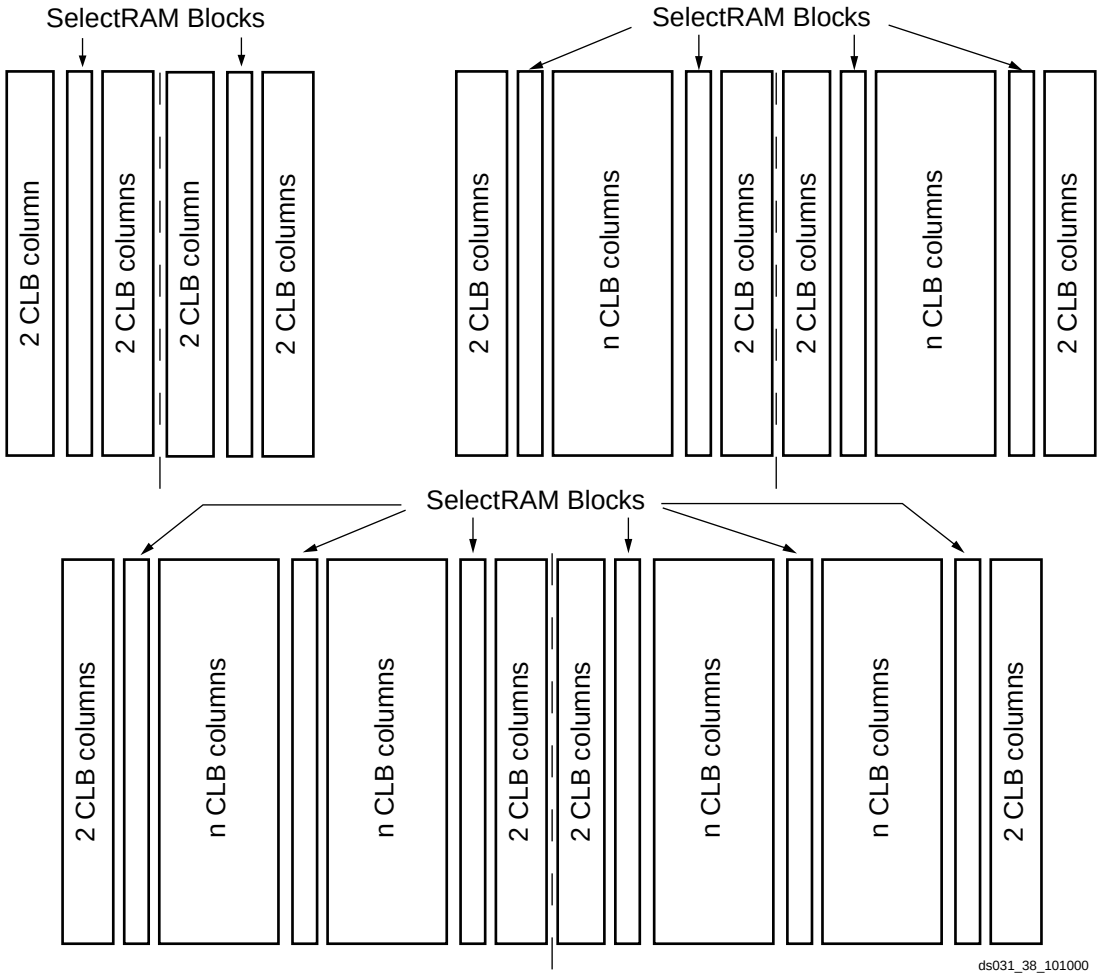


Figure 32: **Block SelectRAM (2-column, 4-column, and 6-column)**

Total Amount of SelectRAM Memory

Table 18 shows the amount of block SelectRAM memory available for each Virtex-II device. The 18-Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 18: **Virtex-II SelectRAM Memory Available**

Device	Total SelectRAM Memory		
	Blocks	in Kbits	in Bits
XC2V40	4	72	73,728
XC2V80	8	144	147,456
XC2V250	24	432	442,368
XC2V500	32	576	589,824
XC2V1000	40	720	737,280
XC2V1500	48	864	884,736
XC2V2000	56	1,008	1,032,192
XC2V3000	96	1,728	1,769,472
XC2V4000	120	2,160	2,211,840
XC2V6000	144	2,592	2,654,208
XC2V8000	168	3,024	3,096,576
XC2V10000	192	3,456	3,538,944

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18-Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM memory and multiplier block is tied to four switch matrices, as shown in Figure 33.

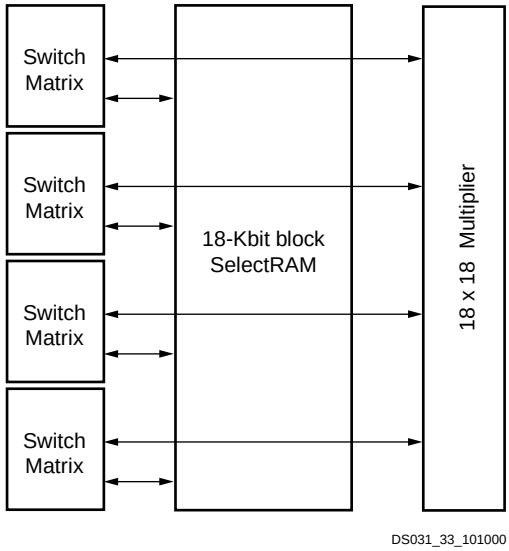


Figure 33: **SelectRAM and Multiplier Blocks**

Association With Block SelectRAM Memory

The interconnect is designed to allow SelectRAM memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM and the multiplier. Thus, SelectRAM memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM resource feeding the multiplier. The use of SelectRAM memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 34 shows a multiplier block.

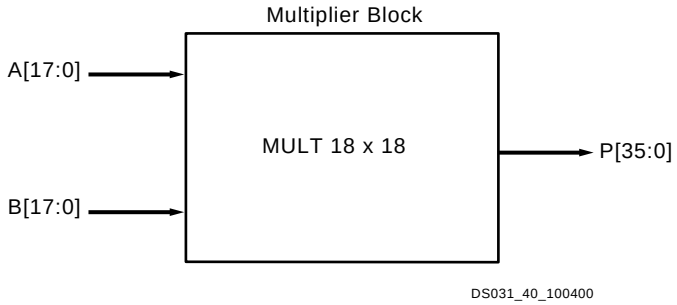


Figure 34: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18-Kbit SelectRAM organization, because each multiplier is associated with an 18-Kbit block SelectRAM resource.

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to **Configurable Logic Blocks (CLBs)**).

Table 19: **Multiplier Floor Plan**

Device	Columns	Multipliers	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168
XC2V10000	6	32	192

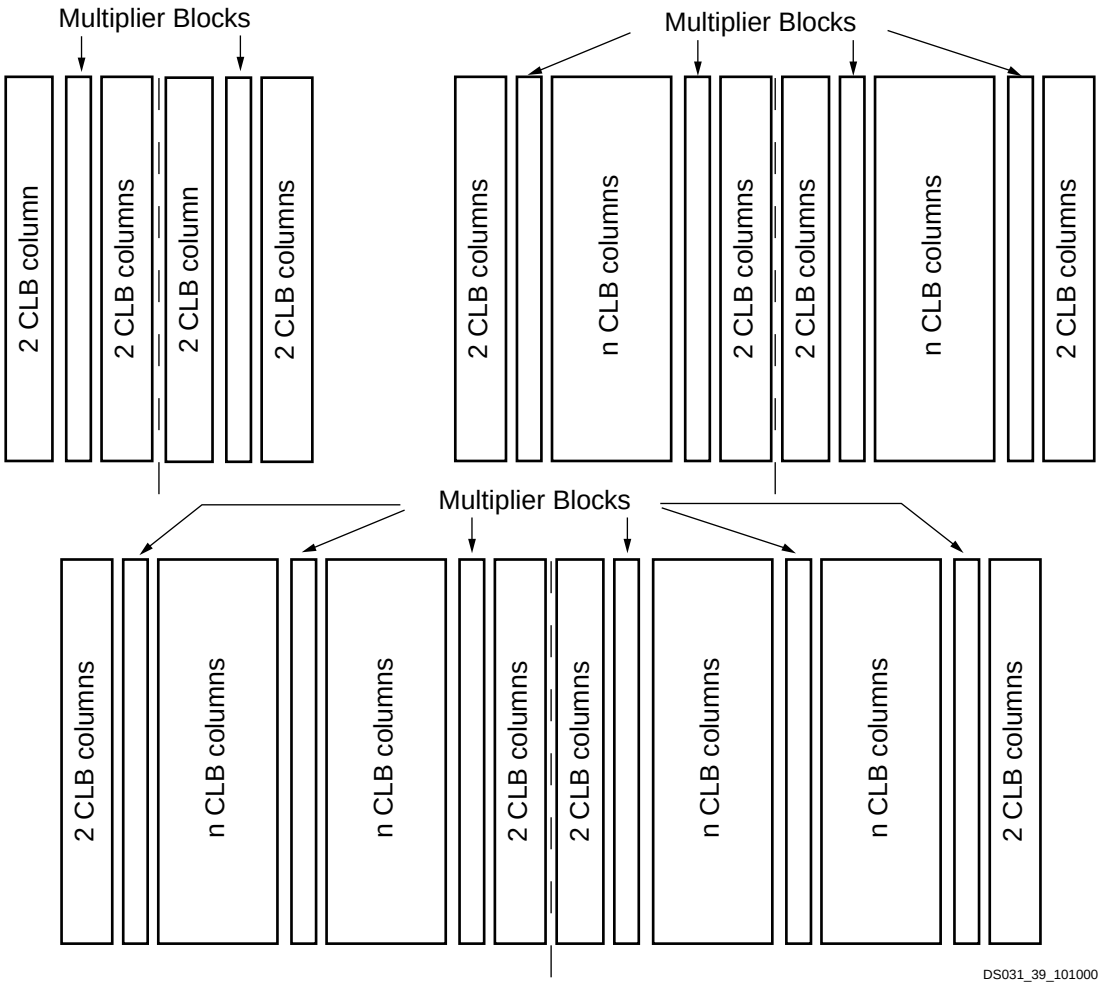


Figure 35: **Multipliers (2-column, 4-column, and 6-column)**

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 36.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

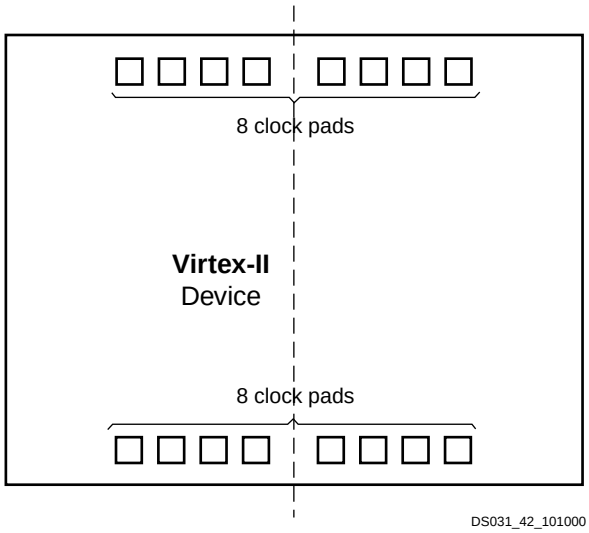


Figure 36: **Virtex-II Clock Pads**

Each global clock buffer can either be driven by the clock pad to distribute a clock directly to the device, or driven by the Digital Clock Manager (DCM), discussed in **Digital Clock Manager (DCM)**, page 27. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 37.

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks.

Eight global clocks can be used in each quadrant of the Virtex-II device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning (see the Virtex-II *User Guide*).

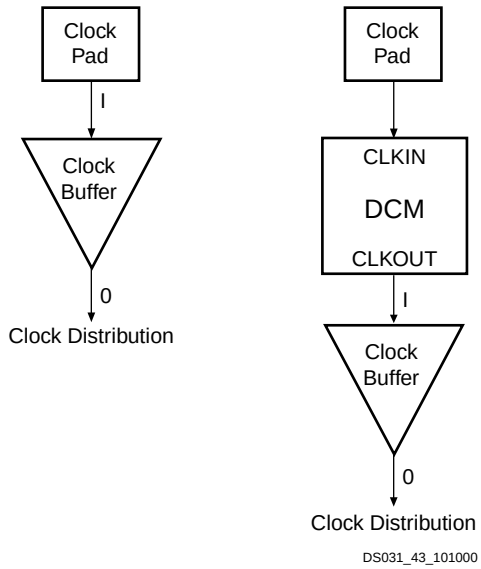


Figure 37: **Virtex-II Clock Distribution Configurations**

Figure 38 shows clock distribution in Virtex-II devices.

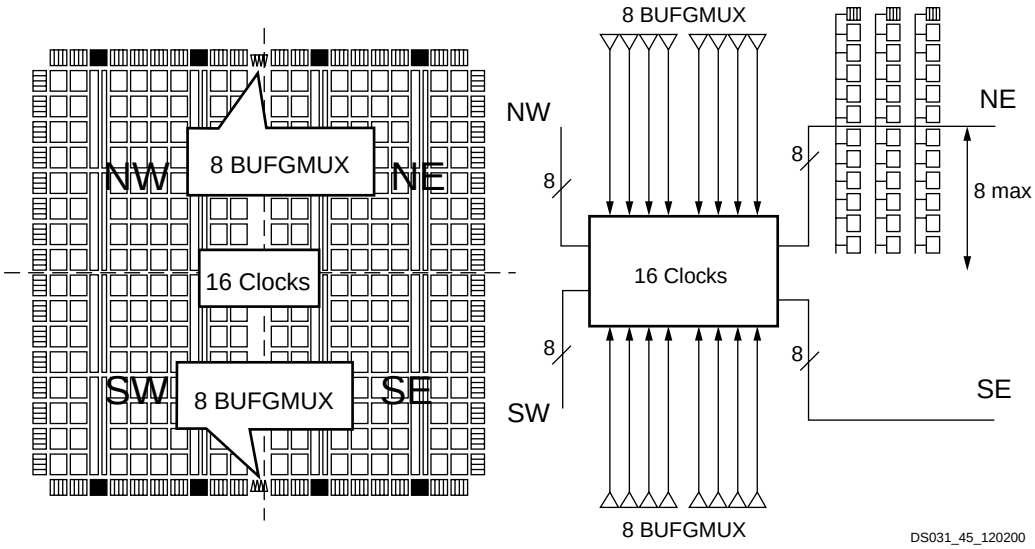


Figure 38: **Virtex-II Clock Distribution**

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

The global clock multiplexer buffers have two clock inputs, a select input, and a clock output. The select input selects between I_O and I_1 without generating glitches.

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in Figure 39.

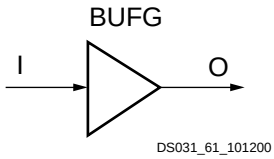


Figure 39: **Virtex-II BUFG Function**

In Figure 40 the global buffer can also perform a clock enable function (clock gating). The CE input is synchronized inside the BUFG so any change in CE is only effective when the clock input is Low. This eliminates any glitches or runt pulses on the output, even when CE changes asynchronously to the clock.

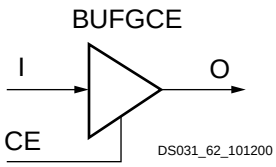


Figure 40: **Virtex-II BUFGCE Function**

The two clock inputs can be connected to any synchronous or asynchronous clock (from a clock pad or DCM clock output). When the select input (S) is Low, the clock connected to the I_0 input is distributed, as shown in Figure 41. Setting S High, causes the clock connected to the I_1 input to be distributed.

The clock multiplexer can also switch between two unrelated clocks. The S input can be changed asynchronously to both clocks. Internal synchronization switches away for the present clock when it is low but switches to the new clock only after the subsequent falling edge.

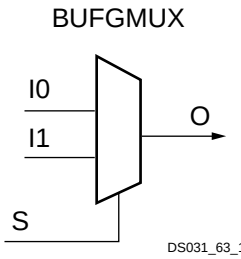


Figure 41: **Virtex-II BUFGMUX Function**

When S changes state, the transition on the output occurs without creating a runt pulse. The output pulse is never shorter than the I_0 or I_1 input pulse. The S input has a setup requirement.

The global clock multiplexer buffers has two options:

- Transition on Low clock states
- Transition on High clock states

The transition on Low follows different steps, as illustrated in Figure 42.

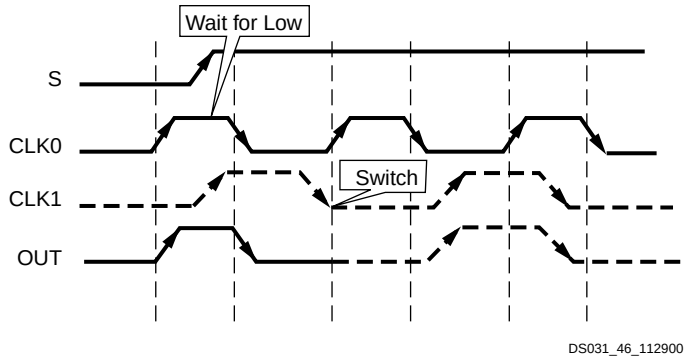


Figure 42: **Clock Multiplexer Waveform Diagram**

- The current clock is CLK0.
- S is activated High (setup is required before the next negative CLK0 edge).
- If CLK0 is currently High, the multiplexer waits for the next negative edge.
- Once CLK0 is Low, the multiplexer output stays Low, until CLK1 goes Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

The transition on High clock state is similar, with the positive edge of the second clock Low.

All Virtex-II devices have 16 global clock multiplexer buffers.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.
- **EMI Reduction**: The DCM provides the capability to reduce electromagnetic interference (EMI) by broadening the output clock frequency spectrum.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four DCM clock outputs can drive global clock multiplexer buffer inputs simultaneously (see Figure 43). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

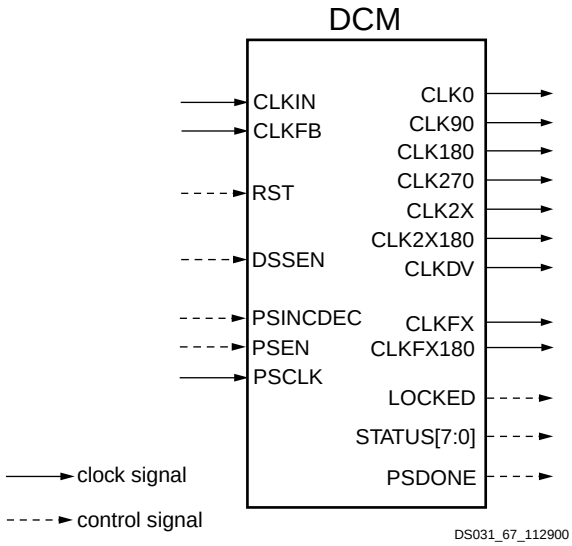


Figure 43: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 20.

Table 20: **DCM Status Pins**

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	N/A
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAM synchronous to clock edges arriving at the input. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs can be used to double the clock frequency. The CLKDV output can be used to create divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$FREQ_{CLKFX} = (M/D) * FREQ_{CLKIN}$$

where M and D are two integers, each between 1 and 4096. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high frequency mode).

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, allowing coarse phase adjustments.

Fine phase adjustment applies to all DCM output clocks when activated. The phase shift between the rising edges of CLKIN and CLKFB is configured to be a specified fraction of the input clock period, and it can be dynamically adjusted with the dedicated signals, PSINCDEC, PSEN, PSCLK, and PSDONE. The phase shift value (PS) is specified as an integer between –255 and +255. The amount of phase shift achieved is given by the equation:

$$\text{Phase shift} = (PS/256) * PERIOD_{CLKIN}$$

In variable mode, the PS value can be dynamically incremented or decremented according to PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 44 illustrates the effects of fine phase shifting.

Table 21 lists fine phase shifting control pins, when used in variable mode.

Table 21: **Fine Phase Shifting Control Pins**

Control Pin	Direction	Function
PSINCDEC	in	Increment or decrement
PSEN	in	Enable ± phase shift
PSCLK	in	Clock for phase shift
PSDONE	out	Active when completed

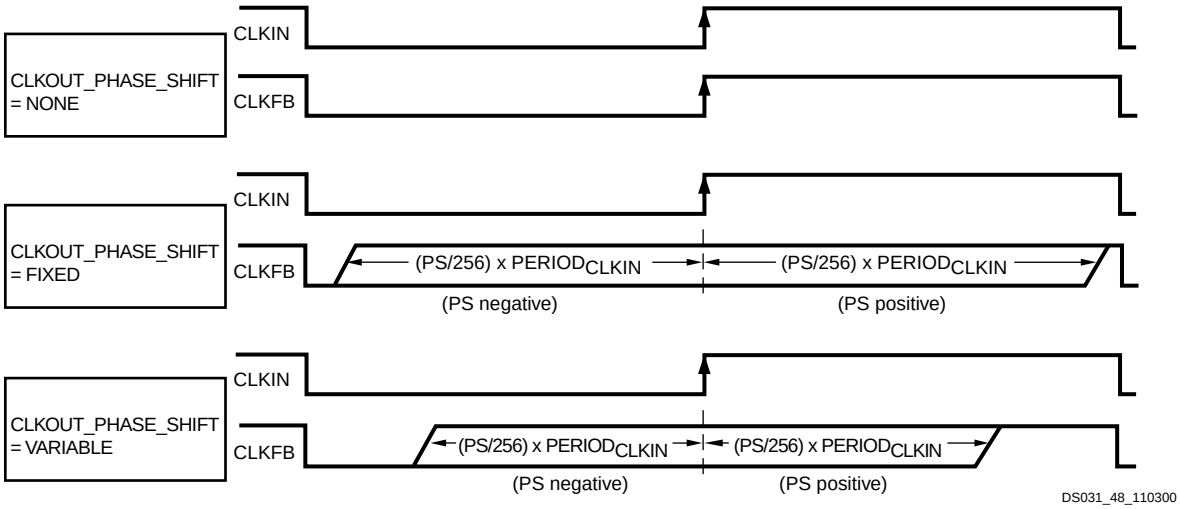


Figure 44: **Fine Phase Shifting Effects**

EMI Reduction

The DCM offers a Digital Spread Spectrum (DSS) feature that broadens the frequency spectrum of the clock outputs. The spectrum spreading applies directly to the CLK0, CLK90, CLK180, and CLK270 clock outputs when it is active. The other DCM clock outputs are affected to only a small degree. Spreading the spectrum of the clock frequency reduces the electromagnetic interference (EMI), or energy radiation, within the relevant frequency bandwidth window. This technique aids in meeting FCC EMI regulations.

When enabled, spectrum spreading begins immediately after the LOCKED signal goes HIGH. The DSSEN input can be used to enable/disable the feature during operation. Table 22 lists available DSS options.

Table 22: **DSS Options**

Number of Frequencies Added	Mode	Clock Period Range
2	SPREAD_2	± 1 x DCM_TAP
4	SPREAD_4	± 2 x DCM_TAP
6	SPREAD_6	± 3 x DCM_TAP
8	SPREAD_8	± 4 x DCM_TAP

Notes:
1. DCM_TAP value is defined in the AC characteristics section

Operating Modes

The frequency ranges of the DCM input and output clocks depend on the operating mode specified, either low frequency mode or high frequency mode, according to Table 23, page 29. (For actual values, see **Virtex-II Switching Characteristics**). The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high frequency mode.

Table 23: **DCM Frequency Ranges**

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	CLK Output	CLKIN Input	CLK Output
CLK0, CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90, CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X, CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX, CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

Locations/Organization

Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in Table 24.

Table 24: **DCM Organization**

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12
XC2V10000	6	12

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All routing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 45.

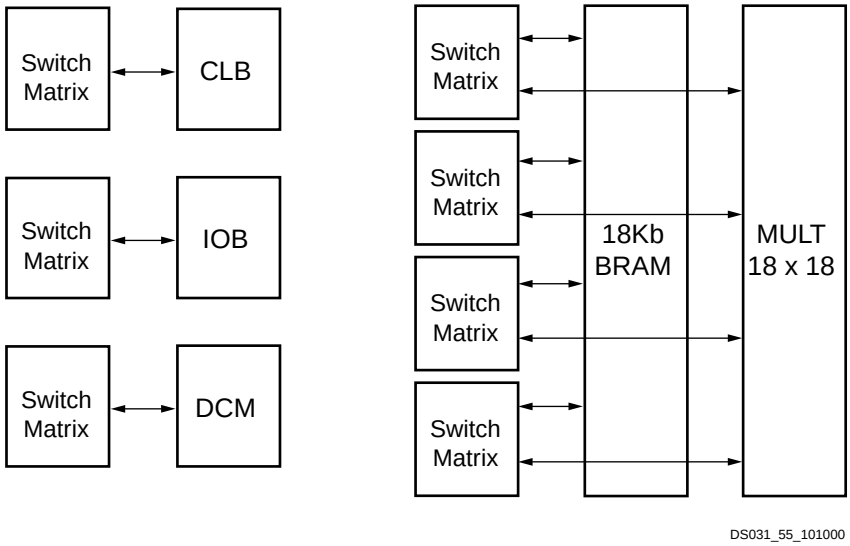


Figure 45: **Active Interconnect Technology**

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 46.

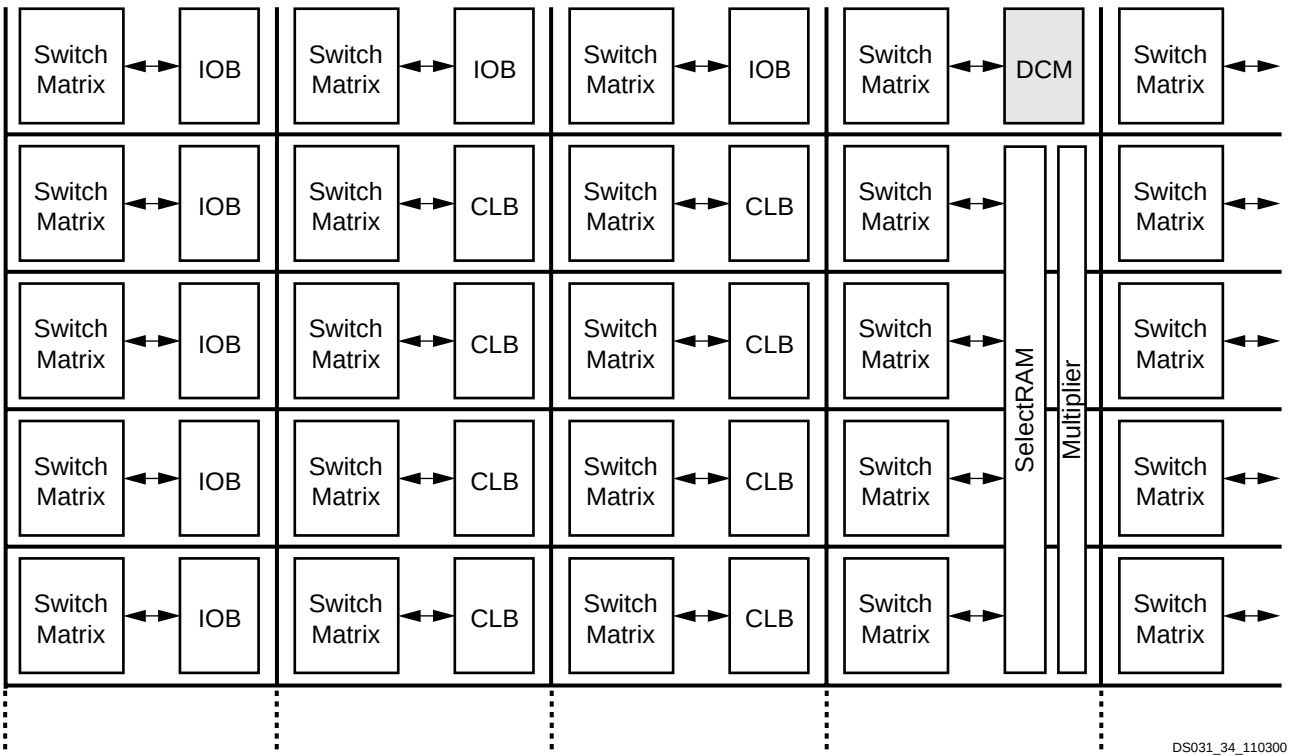


Figure 46: **Routing Resources**

Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

As shown in Figure 46, Virtex-II has fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.

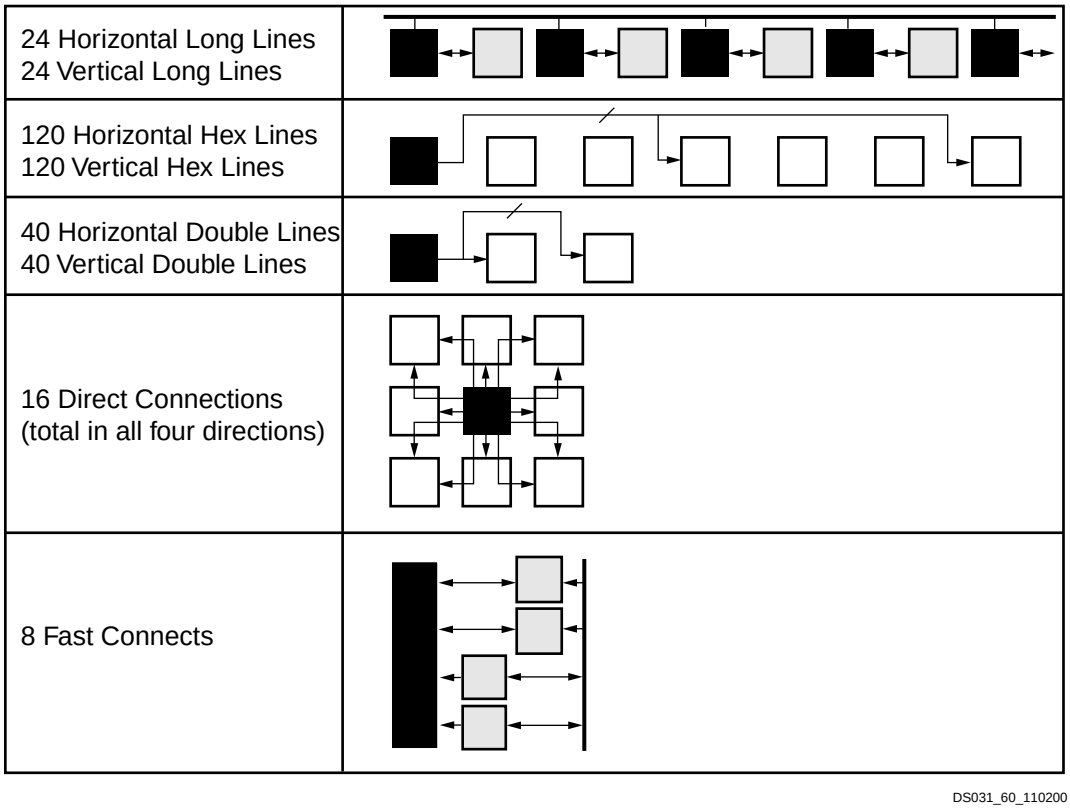


Figure 47: **Hierarchical Routing Resources**

- The long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- The hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).
- The double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).
- The direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- The fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available.

- There are eight global clock nets per quadrant (see **Global Clock Multiplexer Buffers**).
- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row. (See **3-State Buffers**.)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY

output signals vertically to the adjacent slice. (See **CLB/Slice Configurations**.)

- One dedicated SOP chain per slice row (two per CLB row) propagate ORCY output logic signals horizontally to the adjacent slice. (See **Sum of Products**.)
- One dedicated shift-chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See **Shift Registers**, page 12.)

Creating a Design

Creating Virtex-II designs is easy with Xilinx development systems, supporting advanced design capabilities including incremental synthesis, modular design, integrated logic analysis, and the fastest place and route runtimes in the industry. This means designers get the performance they need, quickly.

As a result of the ongoing cooperative development efforts between Xilinx and EDA Alliance partners, designers can take advantage of the benefits provided by EDA technologies in the programmable logic design process. Xilinx development systems are available in a number of easy to use configurations within the Alliance Series and Foundation Series product families.

Alliance Series Solutions

Alliance Series solutions are designed to plug and play within a chosen design environment. Built using industry standard data formats and netlists, these stable, flexible products also enable Alliance EDA partners to deliver their best design automation capabilities to Xilinx customers, providing incremental synthesis, modular design, and error navigation -- all features developed with Xilinx EDA partners, for use with Xilinx development systems first.

Foundation Series Solutions

Foundation Series solutions feature Foundation Integrated Synthesis Environment (ISE) tools, a family of products that deliver all of the benefits of true HDL-based design in a seamlessly integrated design environment. An intuitive project navigator, as well as powerful HDL design and two HDL synthesis tools, ensure that high-quality results are achieved quickly and easily. The Foundation ISE product includes:

- State Diagram entry using StateCAD XE
- Automatic HDL Testbench generation using HDLBencher XE
- HDL Simulation using ModelSim XE-starter (MXE-starter).

MXE Starter is particularly useful in demonstrating the seamless integration available between the ISE design environment and ModelSim HDL Simulation tools.

Design Flow

Virtex-II design flow proceeds as follows:

- Design Entry
- Synthesis
- Implementation
- Verification

Most programmable logic designers iterate through these steps several times in the process of completing a design.

Design Entry

Xilinx development systems support the mainstream EDA design entry capabilities, ranging from schematic design to advanced HDL design methodologies. Given the high densities of the Virtex-II family, designs are most efficiently created using HDLs. To improve efficiency, many Xilinx customers employ incremental, modular, and Intellectual Property (IP) design techniques. When properly used, these techniques further accelerate the logic design process.

To enable designers to leverage existing investments in EDA tools, and to ensure high performance design flows, Xilinx jointly develops tools with leading EDA vendors, including:

- Aldec
- Cadence
- Exemplar
- Mentor Graphics
- Model Technology
- Synopsys
- Synplicity
- VSS

Complete information on Alliance Series partners and their associated design flows is available from the Xilinx Alliance Series web page:

www.xilinx.com/products/alliance.htm

Xilinx Foundation Series products offer schematic entry and HDL design capabilities as part of an integrated design solution - enabling one-stop shopping. These capabilities are powerful, easy to use, and they support the full portfolio of Xilinx programmable logic devices. HDL design capabilities include a color-coded HDL editor with integrated language templates, state diagram entry, and Core generation capabilities.

Synthesis

Alliance Series products are engineered to support advanced design flows with the industry's best synthesis tools for:

- Incremental synthesis
- RTL floorplanning
- Automated timing convergence
- Direct physical mapping

The Xilinx Foundation ISE product family includes synthesis capabilities from both FPGA Express and a proprietary synthesis tool referred to as Xilinx Synthesis Technology. Having two seamlessly integrated synthesis engines within the Foundation ISE products provides an alternative set of optimization techniques for designs, helping to ensure that Foundation ISE can meet even the toughest timing requirements.

Both FPGA Express and Xilinx Synthesis Technology support the synthesis of VHDL and Verilog; however, only FPGA Express enables mixed-language synthesis. Future releases of the ISE design environment are planned to also integrate other third party synthesis tools, like Synplicity Synplify and Exemplar's Leonardo Spectrum.

Design Implementation

The Alliance Series and Foundation Series development systems both include Xilinx timing-driven implementation tools, frequently called “place and route” software. This robust suite of tools enables the creation of an intuitive, flexible, tightly integrated design flow that efficiently bridges the “logical” and “physical” design domains. This simplifies the task of defining a design, including its behavior, timing requirements, and optional layout (or floorplanning), as well as simplifying the task of analyzing reports generated during the implementation process.

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or dynamic timing analysis (simulation), powerful in-circuit debugging techniques using Xilinx ChipScope ILA (Integrated Logic Analysis) is available. In these reconfigurable Xilinx FPGAs, designs can be verified in real time without the need for extensive sets of software simulation vectors. The development system supports both software simulation and in-circuit debugging techniques.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry’s most powerful simulation flows. Alternatively, the user can verify timing-critical portions of a design using the TRCE® static timing analyzer, or using a third party static timing analysis tool by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is “Modular Design”, part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical “logic block”, and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners’ floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical “logic block” to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from “my module works in simulation” to “my module works in the FPGA”. This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Configuration

Virtex-II devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the boundary-scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and boundary scan pins are independent of the V_{CCO}. The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. (See **Virtex-II DC Characteristics**.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532/IEEE 1149)

A detailed description of configuration modes is provided in the Virtex-II *User Guide*.

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II FPGA device. Timing is similar to the Slave SelectMAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In boundary-scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary scan is compliant with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes.

Table 25: **Virtex-II Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pullups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pullups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: **Virtex-II Bitstream Lengths**

Device	# of Configuration Bits
XC2V40	338,208
XC2V80	597,408
XC2V250	1,591,584
XC2V500	2,557,856
XC2V1000	3,749,408
XC2V1500	5,166,240
XC2V2000	6,808,352
XC2V3000	9,589,408
XC2V4000	14,220,192
XC2V6000	19,752,096
XC2V8000	26,185,120
XC2V10000	33,519,264

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the Virtex-II *User Guide.*

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the Virtex-II *User Guide*.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

Power-Down Sequence

The power-down sequence enables a designer to set the device into a low-power, inactive state. The sequence is initiated by pulling the PWRDWN_B pin Low.

If the PWRDWN_STAT option is selected using BitGen, the DONE pin can serve as the power-down status pin. When asserted, power-down has completed. After a successful wake-up, the status pin deasserts. While powered down, the only active pins are the PWRDWN_B and DONE. All inputs are off and all outputs are 3-stated.

While in the POWERDOWN state, the Power On Reset (POR) circuit is still active, but it does not reset the device if V_{CCINT}, V_{CCO}, or V_{CCAUX} falls below its minimum value. The POR circuit waits until the PWRDWN_B pin is released before resetting the device. Also, the PROG_B pin is not sampled while the device is in the POWERDOWN state. The PROG_B pin becomes active when the PWRDWN_B pin is released. Therefore, the device cannot be reset while in the POWERDOWN state.

The wake-up sequence is the reverse of the power-down sequence.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). A note was added to Table 1, “Supported Single-Ended I/O Standards,” on page 1.
04/02/01	1.5	• Under **Input/Output Individual Options**, page 4, the range of values for optional pull-up and pull-down resistors was changed to 10 - 60 KΩ from 50 - 100 KΩ. • Skipped v1.4 to sync up modules. Reverted to traditional double-column format.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- DS031-1, Virtex-II 1.5V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS031-2, Virtex-II 1.5V FPGAs: Functional Description (Module 2)
- DS031-3, Virtex-II 1.5V FPGAs: **DC and Switching Characteristics (Module 3)**
- DS031-4, Virtex-II 1.5V FPGAs: **Pinout Tables (Module 4)**

Virtex-II 1.5V Field-Programmable Gate Arrays Pinout Information

DS031-4 (v1.5) April 2, 2001

Advance Product Specification

This document provides **Virtex®-II Device/Package Combinations and Maximum I/Os Available** and **Virtex-II Pin Definitions**, followed by pinout tables for the following packages:

- **CS144 Chip-Scale BGA Package**
- **FG256 Fine-Pitch BGA Package**
- **FG456 Fine-Pitch BGA Package**
- **FG676 Fine-Pitch BGA Package**
- **BG575 Standard BGA Package**
- **BG728 Standard BGA Package**
- **FF896 Flip-Chip Fine-Pitch BGA Package**
- **FF1152 Flip-Chip Fine-Pitch BGA Package**
- **FF1517 Flip-Chip Fine-Pitch BGA Package**
- **BF957 Flip-Chip BGA Package**

Virtex®-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

Table 3 shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: **Wire-Bond Packages Information**

Package	CS144	FG256	FG456	FG676	BG575	BG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Table 2: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 3: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os**

Package	Available I/Os											
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000	XC2V 10000
CS144	88	92	92									
FG256	88	120	172	172	172							
FG456			200	264	324							
FG676						392	456	484				
FF896					432	528	624					
FF1152								720	824	824	824	824
FF1517									912	1,104	1,108	1,108
BG575					328	392	408					
BG728							456	516				
BF957							624	684	684	684	684	684

Virtex-II Pin Definitions

This section describes the pinouts for Virtex-II devices in the following packages:

- CS144: wire-bond chip-scale ball grid array (BGA) of 0.80 mm pitch
- FG256, FG456, and FG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF896, FF1152, FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages. Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the Virtex-II *Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

The FG256 pinouts (Table 6) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at **http://www.xilinx.com**).

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, or LDT pairs. Each user I/O is labeled "**IO_LXXY**_#", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. # indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, DIN/D0 – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
DIN / D0, D1, D2, D3, D4, D5, D6, D7	Input/Output	In SelectMAP mode, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. In bit-serial modes, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 4: **Virtex-II Pin Definitions *(Continued)***

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pullups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input	Power down pin.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Do not connect if battery is not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

CS144 Chip-Scale BGA Package

As shown in Table 5, XC2V40, XC2V80, and XC2V250 Virtex-II devices are available in the CS144 package. Pins in the XC2V40, XC2V80, and XC2V250 devices are the same except for pin differences in the XC2V40 device, shown in the No Connect column. Following this table are the **CS144 Chip-Scale BGA Package Specifications (0.80mm pitch)**.

Table 5: **CS144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
0	IO_L01N_0	B3	
0	IO_L01P_0	A3	
0	IO_L02N_0	C4	
0	IO_L02P_0	B4	
0	IO_L03N_0/VRP_0	A4	
0	IO_L03P_0/VRN_0	D5	
0	IO_L94N_0/VREF_0	A5	
0	IO_L94P_0	D6	
0	IO_L95N_0/GCLK7P	C6	
0	IO_L95P_0/GCLK6S	B6	
0	IO_L96N_0/GCLK5P	A6	
0	IO_L96P_0/GCLK4S	D7	
1	IO_L96N_1/GCLK3P	A7	
1	IO_L96P_1/GCLK2S	B7	
1	IO_L95N_1/GCLK1P	A8	
1	IO_L95P_1/GCLK0S	B8	
1	IO_L94N_1	C8	
1	IO_L94P_1/VREF_1	D8	
1	IO_L03N_1/VRP_1	C9	
1	IO_L03P_1/VRN_1	D9	
1	IO_L02N_1	A10	
1	IO_L02P_1	B10	
1	IO_L01N_1	C10	
1	IO_L01P_1	D10	
2	IO_L01N_2	C13	
2	IO_L01P_2	D11	
2	IO_L02N_2/VRP_2	D12	
2	IO_L02P_2/VRN_2	D13	
2	IO_L03N_2	E10	
2	IO_L03P_2/VREF_2	E11	
2	IO_L93N_2	E13	NC
2	IO_L93P_2/VREF_2	F11	NC
2	IO_L94N_2	F12	
2	IO_L94P_2	G10	

Table 5: **CS144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
2	IO_L96N_2	G11	
2	IO_L96P_2	G13	
3	IO_L96N_3	G12	
3	IO_L96P_3	H12	
3	IO_L94N_3	H11	
3	IO_L94P_3	J13	
3	IO_L03N_3/VREF_3	J10	
3	IO_L03P_3	K13	
3	IO_L02N_3/VRP_3	K12	
3	IO_L02P_3/VRN_3	K11	
3	IO_L01N_3	K10	
3	IO_L01P_3	L13	
4	IO_L01N_4/DOUT	M11	
4	IO_L01P_4/INIT_B	N11	
4	IO_L02N_4/D0	L10	
4	IO_L02P_4/D1	M10	
4	IO_L03N_4/D2/ALT_VRP_4	N10	
4	IO_L03P_4/D3/ALT_VRN_4	K9	
4	IO_L94N_4/VREF_4	N9	
4	IO_L94P_4	K8	
4	IO_L95N_4/GCLK3S	L8	
4	IO_L95P_4/GCLK2P	M8	
4	IO_L96N_4/GCLK1S	N8	
4	IO_L96P_4/GCLK0P	K7	
5	IO_L96N_5/GCLK7S	N7	
5	IO_L96P_5/GCLK6P	M7	
5	IO_L95N_5/GCLK5S	N6	
5	IO_L95P_5/GCLK4P	M6	
5	IO_L94N_5	L6	
5	IO_L94P_5/VREF_5	K6	
5	IO_L03N_5/D4/ALT_VRP_5	L5	
5	IO_L03P_5/D5/ALT_VRN_5	K5	
5	IO_L02N_5/D6	N4	
5	IO_L02P_5/D7	M4	
5	IO_L01N_5/RDWR_B	L4	
5	IO_L01P_5/CS_B	K4	

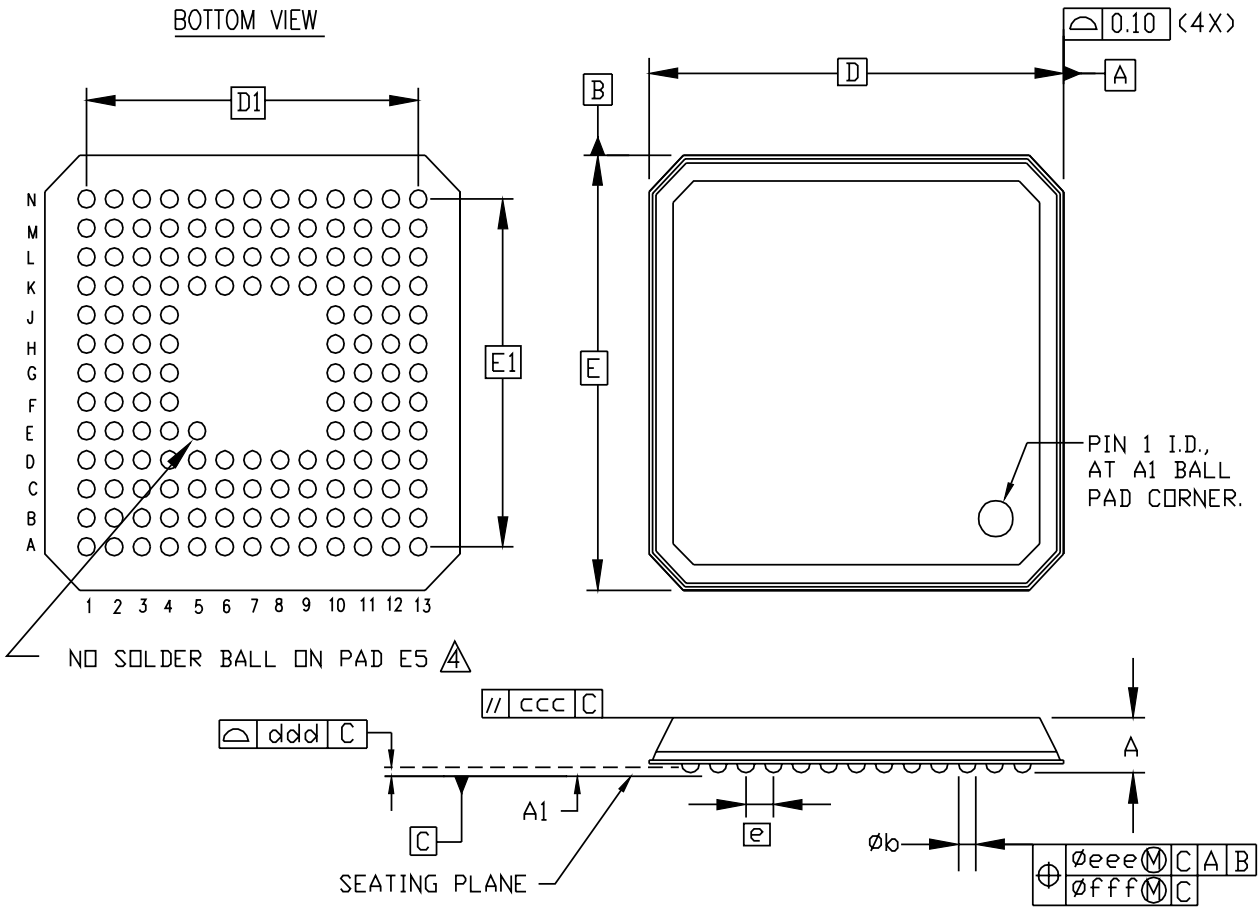
Table 5: **CS144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

Table 5: **CS144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
NA	CCLK	M13	
NA	PROG_B	B1	
NA	DONE	N12	
NA	M0	N2	
NA	M1	M2	
NA	M2	M3	
NA	TCK	B12	
NA	TDI	C1	
NA	TDO	C11	
NA	TMS	A13	
NA	PWRDWN_B	M12	
NA	HSWAP_EN	A1	
NA	RSVD	A2	
NA	RSVD	B2	
NA	VBATT	A12	
NA	RSVD	B11	
NA	VCCAUX	C2	
NA	VCCAUX	N1	
NA	VCCAUX	N13	
NA	VCCAUX	B13	
NA	VCCINT	H2	
NA	VCCINT	L7	
NA	VCCINT	H13	
NA	VCCINT	C7	
NA	GND	E1	
NA	GND	G2	
NA	GND	J1	
NA	GND	J4	
NA	GND	M5	
NA	GND	L9	
NA	GND	J11	
NA	GND	H10	
NA	GND	F13	
NA	GND	E12	
NA	GND	B9	
NA	GND	C5	

CS144 Chip-Scale BGA Package Specifications (0.80mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A_1	0.35	0.40	0.45
D/E	12.00 BSC		
D_1/E_1	9.60 BSC		
e	0.80 BSC		
øb	0.45	0.50	0.55
ccc	---	---	0.10
ddd	---	---	0.12
eee	---	---	0.15
fff	---	---	0.08
M	13		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-205-BE (DEPOPULATED).
4. PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

Figure 1: **CS144 Chip-Scale BGA Package Specifications**

FG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the **FG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
1	IO_L92P_1	E11	NC	NC
1	IO_L05N_1	A11	NC	NC
1	IO_L05P_1	B11	NC	NC
1	IO_L04N_1	C11	NC	NC
1	IO_L04P_1/VREF_1	D11	NC	NC
1	IO_L03N_1/VRP_1	A12		
1	IO_L03P_1/VRN_1	B12		
1	IO_L02N_1	C12		
1	IO_L02P_1	D12		
1	IO_L01N_1	B13		
1	IO_L01P_1	C13		
2	IO_L01N_2	C16		
2	IO_L01P_2	D16		
2	IO_L02N_2/VRP_2	D14		
2	IO_L02P_2/VRN_2	D15		
2	IO_L03N_2	E13		
2	IO_L03P_2/VREF_2	E14		
2	IO_L04N_2	E15	NC	
2	IO_L04P_2	E16	NC	
2	IO_L06N_2	F13	NC	
2	IO_L06P_2	F14	NC	
2	IO_L43N_2	F15	NC	NC
2	IO_L43P_2	F16	NC	NC
2	IO_L45N_2	F12	NC	NC
2	IO_L45P_2/VREF_2	G12	NC	NC
2	IO_L91N_2	G13	NC	
2	IO_L91P_2	G14	NC	
2	IO_L93N_2	G15	NC	
2	IO_L93P_2/VREF_2	G16	NC	
2	IO_L94N_2	H13		
2	IO_L94P_2	H14		
2	IO_L96N_2	H15		
2	IO_L96P_2	H16		

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/DOUT	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
5	IO_L01P_5/CS_B	T3		
6	IO_L01P_6	P1		
6	IO_L01N_6	N1		
6	IO_L02P_6/VRN_6	N3		
6	IO_L02N_6/VRP_6	N2		
6	IO_L03P_6	M4		
6	IO_L03N_6/VREF_6	M3		
6	IO_L04P_6	M2	NC	
6	IO_L04N_6	M1	NC	
6	IO_L06P_6	L4	NC	
6	IO_L06N_6	L3	NC	
6	IO_L43P_6	L2	NC	NC
6	IO_L43N_6	L1	NC	NC
6	IO_L45P_6	L5	NC	NC
6	IO_L45N_6/VREF_6	K5	NC	NC
6	IO_L91P_6	K4	NC	
6	IO_L91N_6	K3	NC	
6	IO_L93P_6	K2	NC	
6	IO_L93N_6/VREF_6	K1	NC	
6	IO_L94P_6	J4		
6	IO_L94N_6	J3		
6	IO_L96P_6	J2		
6	IO_L96N_6	J1		
7	IO_L96P_7	H1		
7	IO_L96N_7	H2		
7	IO_L94P_7	H3		
7	IO_L94N_7	H4		
7	IO_L93P_7/VREF_7	G1	NC	
7	IO_L93N_7	G2	NC	
7	IO_L91P_7	G3	NC	
7	IO_L91N_7	G4	NC	
7	IO_L45P_7/VREF_7	G5	NC	NC

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		

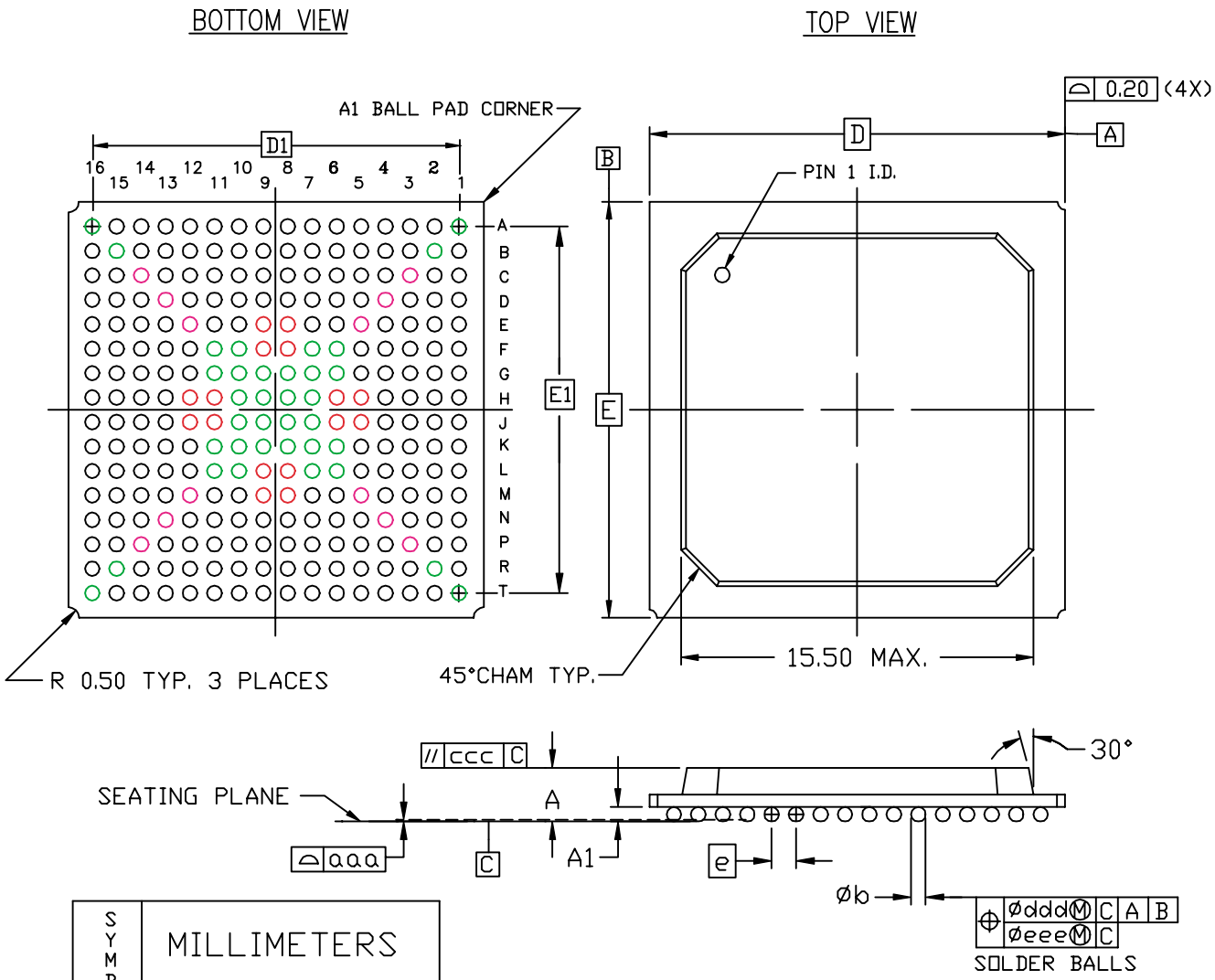
Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

Table 6: **FG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
NA	GND	T16		
NA	GND	T1		
NA	GND	R15		
NA	GND	R2		
NA	GND	P14		
NA	GND	P3		
NA	GND	L11		
NA	GND	L6		
NA	GND	K10		
NA	GND	K9		
NA	GND	K8		
NA	GND	K7		
NA	GND	J10		
NA	GND	J9		
NA	GND	J8		
NA	GND	J7		
NA	GND	H10		
NA	GND	H9		
NA	GND	H8		
NA	GND	H7		
NA	GND	G10		
NA	GND	G9		
NA	GND	G8		
NA	GND	G7		
NA	GND	F11		
NA	GND	F6		
NA	GND	C14		
NA	GND	C3		
NA	GND	B15		
NA	GND	B2		
NA	GND	A16		
NA	GND	A1		

FG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.73	2.00
A_1	0.40	0.50	0.60
D/E	17.00 BSC		
D_1/E_1	15.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	16		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MO–151 AAF–1.

Figure 2: **FG256 Fine-Pitch BGA Package Specifications**

FG456 Fine-Pitch BGA Package

As shown in Table 7, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG456 fine-pitch BGA package. Pins in the XC2V250, XC2V500, and XC2V1000 devices are the same, except for the pin differences in the XC2V250 and XC2V500 devices shown in the No Connect columns. Following this table are the **FG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L01N_0	B4		
0	IO_L01P_0	A4		
0	IO_L02N_0	C4		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6		
0	IO_L04P_0	C6		
0	IO_L05N_0	B6		
0	IO_L05P_0	A6		
0	IO_L06N_0	E7		
0	IO_L06P_0	E8		
0	IO_L21N_0	D7	NC	NC
0	IO_L21P_0/VREF_0	C7	NC	NC
0	IO_L22N_0	B7	NC	NC
0	IO_L22P_0	A7	NC	NC
0	IO_L24N_0	D8	NC	NC
0	IO_L24P_0	C8	NC	NC
0	IO_L49N_0	B8	NC	
0	IO_L49P_0	A8	NC	
0	IO_L51N_0	E9	NC	
0	IO_L51P_0/VREF_0	F9	NC	
0	IO_L52N_0	D9	NC	
0	IO_L52P_0	C9	NC	
0	IO_L54N_0	B9	NC	
0	IO_L54P_0	A9	NC	
0	IO_L91N_0/VREF_0	E10		
0	IO_L91P_0	F10		
0	IO_L92N_0	D10		
0	IO_L92P_0	C10		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L93N_0	B10		
0	IO_L93P_0	A10		
0	IO_L94N_0/VREF_0	E11		
0	IO_L94P_0	F11		
0	IO_L95N_0/GCLK7P	D11		
0	IO_L95P_0/GCLK6S	C11		
0	IO_L96N_0/GCLK5P	B11		
0	IO_L96P_0/GCLK4S	A11		
1	IO_L96N_1/GCLK3P	F12		
1	IO_L96P_1/GCLK2S	F13		
1	IO_L95N_1/GCLK1P	E12		
1	IO_L95P_1/GCLK0S	D12		
1	IO_L94N_1	C12		
1	IO_L94P_1/VREF_1	B12		
1	IO_L93N_1	A13		
1	IO_L93P_1	B13		
1	IO_L92N_1	C13		
1	IO_L92P_1	D13		
1	IO_L91N_1	E13		
1	IO_L91P_1/VREF_1	E14		
1	IO_L54N_1	A14	NC	
1	IO_L54P_1	B14	NC	
1	IO_L52N_1	C14	NC	
1	IO_L52P_1	D14	NC	
1	IO_L51N_1/VREF_1	A15	NC	
1	IO_L51P_1	B15	NC	
1	IO_L49N_1	C15	NC	
1	IO_L49P_1	D15	NC	
1	IO_L24N_1	F14	NC	NC
1	IO_L24P_1	E15	NC	NC
1	IO_L22N_1	A16	NC	NC
1	IO_L22P_1	B16	NC	NC
1	IO_L21N_1/VREF_1	C16	NC	NC

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
1	IO_L21P_1	D16	NC	NC
1	IO_L06N_1	E16		
1	IO_L06P_1	E17		
1	IO_L05N_1	A17		
1	IO_L05P_1	B17		
1	IO_L04N_1	C17		
1	IO_L04P_1/VREF_1	D17		
1	IO_L03N_1/VRP_1	A18		
1	IO_L03P_1/VRN_1	B18		
1	IO_L02N_1	C18		
1	IO_L02P_1	D18		
1	IO_L01N_1	A19		
1	IO_L01P_1	B19		
2	IO_L01N_2	C21		
2	IO_L01P_2	C22		
2	IO_L02N_2/VRP_2	E18		
2	IO_L02P_2/VRN_2	F18		
2	IO_L03N_2	D21		
2	IO_L03P_2/VREF_2	D22		
2	IO_L04N_2	E19		
2	IO_L04P_2	E20		
2	IO_L06N_2	E21		
2	IO_L06P_2	E22		
2	IO_L19N_2	F19	NC	NC
2	IO_L19P_2	F20	NC	NC
2	IO_L21N_2	F21	NC	NC
2	IO_L21P_2/VREF_2	F22	NC	NC
2	IO_L22N_2	G18	NC	NC
2	IO_L22P_2	H18	NC	NC
2	IO_L24N_2	G19	NC	NC
2	IO_L24P_2	G20	NC	NC
2	IO_L43N_2	G21		
2	IO_L43P_2	G22		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/DOUT	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L02N_4/D0	V18		
4	IO_L02P_4/D1	V17		
4	IO_L03N_4/D2/ALT_VRP_4	W18		
4	IO_L03P_4/D3/ALT_VRN_4	Y18		
4	IO_L04N_4/VREF_4	AA18		
4	IO_L04P_4	AB18		
4	IO_L05N_4/VRP_4	W17		
4	IO_L05P_4/VRN_4	Y17		
4	IO_L06N_4	AA17		
4	IO_L06P_4	AB17		
4	IO_L19N_4	V16	NC	NC
4	IO_L19P_4	V15	NC	NC
4	IO_L21N_4	W16	NC	NC
4	IO_L21P_4/VREF_4	Y16	NC	NC
4	IO_L22N_4	AA16	NC	NC
4	IO_L22P_4	AB16	NC	NC
4	IO_L24N_4	W15	NC	NC
4	IO_L24P_4	Y15	NC	NC
4	IO_L49N_4	AA15	NC	
4	IO_L49P_4	AB15	NC	
4	IO_L51N_4	U14	NC	
4	IO_L51P_4/VREF_4	V14	NC	
4	IO_L52N_4	W14	NC	
4	IO_L52P_4	Y14	NC	
4	IO_L54N_4	AA14	NC	
4	IO_L54P_4	AB14	NC	
4	IO_L91N_4/VREF_4	U13		
4	IO_L91P_4	V13		
4	IO_L92N_4	W13		
4	IO_L92P_4	Y13		
4	IO_L93N_4	AA13		
4	IO_L93P_4	AB13		
4	IO_L94N_4/VREF_4	U12		
4	IO_L94P_4	V12		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
4	IO_L95N_4/GCLK3S	W12		
4	IO_L95P_4/GCLK2P	Y12		
4	IO_L96N_4/GCLK1S	AA12		
4	IO_L96P_4/GCLK0P	AB12		
5	IO_L96N_5/GCLK7S	AA11		
5	IO_L96P_5/GCLK6P	Y11		
5	IO_L95N_5/GCLK5S	W11		
5	IO_L95P_5/GCLK4P	V11		
5	IO_L94N_5	U11		
5	IO_L94P_5/VREF_5	U10		
5	IO_L93N_5	AB10		
5	IO_L93P_5	AA10		
5	IO_L92N_5	Y10		
5	IO_L92P_5	W10		
5	IO_L91N_5	V10		
5	IO_L91P_5/VREF_5	V9		
5	IO_L54N_5	AB9	NC	
5	IO_L54P_5	AA9	NC	
5	IO_L52N_5	Y9	NC	
5	IO_L52P_5	W9	NC	
5	IO_L51N_5/VREF_5	AB8	NC	
5	IO_L51P_5	AA8	NC	
5	IO_L49N_5	Y8	NC	
5	IO_L49P_5	W8	NC	
5	IO_L24N_5	U9	NC	NC
5	IO_L24P_5	V8	NC	NC
5	IO_L22N_5	AB7	NC	NC
5	IO_L22P_5	AA7	NC	NC
5	IO_L21N_5/VREF_5	Y7	NC	NC
5	IO_L21P_5	W7	NC	NC
5	IO_L19N_5	AB6	NC	NC
5	IO_L19P_5	AA6	NC	NC
5	IO_L06N_5	Y6		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
5	IO_L06P_5	W6		
5	IO_L05N_5/VRP_5	V7		
5	IO_L05P_5/VRN_5	V6		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	Y5		
5	IO_L03P_5/D5/ALT_VRN_5	W5		
5	IO_L02N_5/D6	AB4		
5	IO_L02P_5/D7	AA4		
5	IO_L01N_5/RDWR_B	Y4		
5	IO_L01P_5/CS_B	AA3		
6	IO_L01P_6	V5		
6	IO_L01N_6	U5		
6	IO_L02P_6/VRN_6	Y2		
6	IO_L02N_6/VRP_6	Y1		
6	IO_L03P_6	V4		
6	IO_L03N_6/VREF_6	V3		
6	IO_L04P_6	W2		
6	IO_L04N_6	W1		
6	IO_L06P_6	U4		
6	IO_L06N_6	U3		
6	IO_L19P_6	V2	NC	NC
6	IO_L19N_6	V1	NC	NC
6	IO_L21P_6	U2	NC	NC
6	IO_L21N_6/VREF_6	U1	NC	NC
6	IO_L22P_6	T5	NC	NC
6	IO_L22N_6	R5	NC	NC
6	IO_L24P_6	T4	NC	NC
6	IO_L24N_6	T3	NC	NC
6	IO_L43P_6	T2		
6	IO_L43N_6	T1		
6	IO_L45P_6	R4		
6	IO_L45N_6/VREF_6	R3		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
6	IO_L46P_6	R2		
6	IO_L46N_6	R1		
6	IO_L48P_6	P6		
6	IO_L48N_6	P5		
6	IO_L49P_6	P4	NC	
6	IO_L49N_6	P3	NC	
6	IO_L51P_6	P2	NC	
6	IO_L51N_6/VREF_6	P1	NC	
6	IO_L52P_6	N6	NC	
6	IO_L52N_6	N5	NC	
6	IO_L54P_6	N4	NC	
6	IO_L54N_6	N3	NC	
6	IO_L91P_6	N2		
6	IO_L91N_6	N1		
6	IO_L93P_6	M6		
6	IO_L93N_6/VREF_6	M5		
6	IO_L94P_6	M4		
6	IO_L94N_6	M3		
6	IO_L96P_6	M2		
6	IO_L96N_6	M1		
7	IO_L96P_7	L2		
7	IO_L96N_7	L3		
7	IO_L94P_7	L4		
7	IO_L94N_7	L5		
7	IO_L93P_7/VREF_7	K1		
7	IO_L93N_7	K2		
7	IO_L91P_7	K3		
7	IO_L91N_7	K4		
7	IO_L54P_7	L6	NC	
7	IO_L54N_7	K6	NC	
7	IO_L52P_7	K5	NC	
7	IO_L52N_7	J5	NC	
7	IO_L51P_7/VREF_7	J1	NC	

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	IO_L51N_7	J2	NC	
7	IO_L49P_7	J3	NC	
7	IO_L49N_7	J4	NC	
7	IO_L48P_7	H1		
7	IO_L48N_7	H2		
7	IO_L46P_7	H3		
7	IO_L46N_7	H4		
7	IO_L45P_7/VREF_7	J6		
7	IO_L45N_7	H5		
7	IO_L43P_7	G1		
7	IO_L43N_7	G2		
7	IO_L24P_7	G3	NC	NC
7	IO_L24N_7	G4	NC	NC
7	IO_L22P_7	F1	NC	NC
7	IO_L22N_7	F2	NC	NC
7	IO_L21P_7/VREF_7	F3	NC	NC
7	IO_L21N_7	F4	NC	NC
7	IO_L19P_7	G5	NC	NC
7	IO_L19N_7	F5	NC	NC
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	D1		
7	IO_L03N_7	D2		
7	IO_L02P_7/VRN_7	C1		
7	IO_L02N_7/VRP_7	C2		
7	IO_L01P_7	E5		
7	IO_L01N_7	E6		
0	VCCO_0	G11		
0	VCCO_0	G10		
0	VCCO_0	G9		
0	VCCO_0	F8		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	VCCO_0	F7		
1	VCCO_1	G14		
1	VCCO_1	G13		
1	VCCO_1	G12		
1	VCCO_1	F16		
1	VCCO_1	F15		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	J16		
2	VCCO_2	H17		
2	VCCO_2	G17		
3	VCCO_3	T17		
3	VCCO_3	R17		
3	VCCO_3	P16		
3	VCCO_3	N16		
3	VCCO_3	M16		
4	VCCO_4	U16		
4	VCCO_4	U15		
4	VCCO_4	T14		
4	VCCO_4	T13		
4	VCCO_4	T12		
5	VCCO_5	U8		
5	VCCO_5	U7		
5	VCCO_5	T11		
5	VCCO_5	T10		
5	VCCO_5	T9		
6	VCCO_6	T6		
6	VCCO_6	R6		
6	VCCO_6	P7		
6	VCCO_6	N7		
6	VCCO_6	M7		
7	VCCO_7	L7		
7	VCCO_7	K7		
7	VCCO_7	J7		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

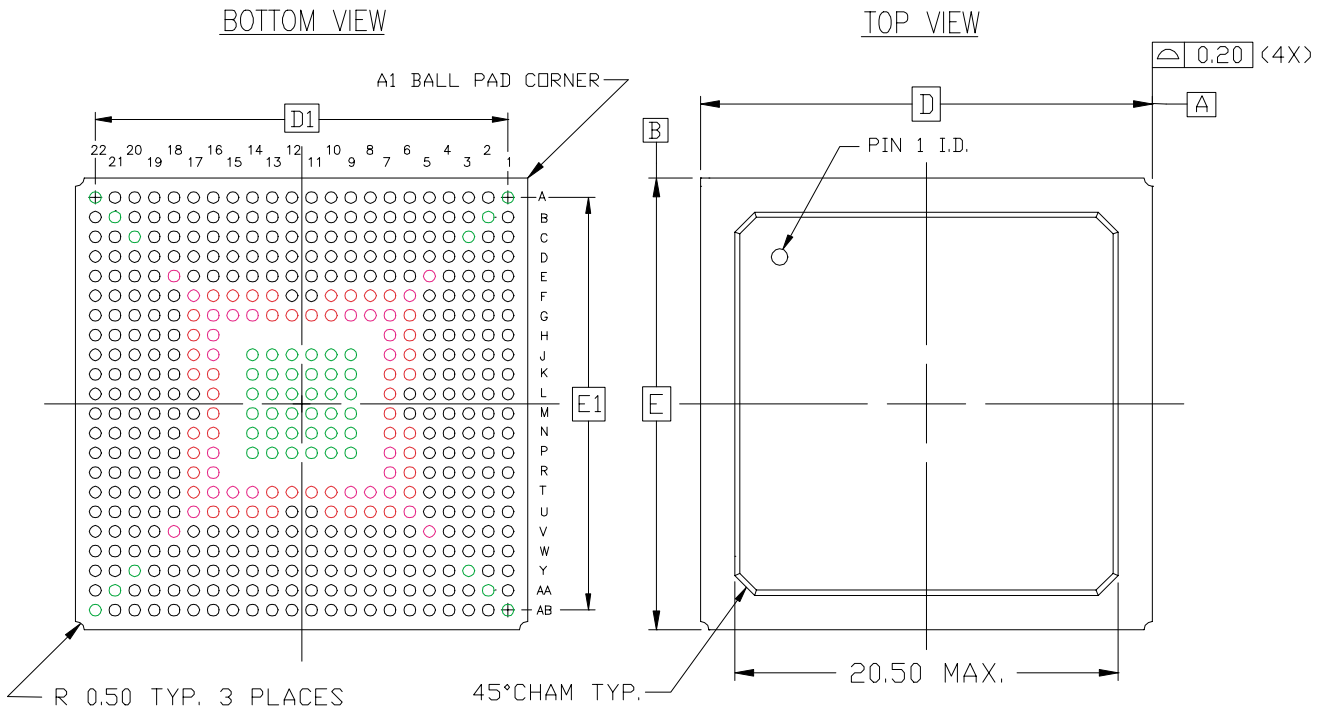
Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 7: **FG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

FG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.20	2.60
A_1	0.40	0.50	0.60
D/E	23.00 BSC		
D_1/E_1	21.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	22		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MO–151 AAJ–1 (DEPOPULATED)

Figure 3: **FG456 Fine-Pitch BGA Package Specifications**

FG676 Fine-Pitch BGA Package

As shown in Table 8, XC2V1500, XC2V2000, and XC2V3000 Virtex-II devices are available in the FG676 fine-pitch BGA package. Pins in the XC2V1500, XC2V2000, and XC2V3000 devices are the same, except for the pin differences in the XC2V1500 and XC2V2000 devices shown in the No Connect columns. Following this table are the **FG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
0	IO_L01N_0	D6		
0	IO_L01P_0	C6		
0	IO_L02N_0	B1		
0	IO_L02P_0	A2		
0	IO_L03N_0/VRP_0	D7		
0	IO_L03P_0/VRN_0	C7		
0	IO_L04N_0/VREF_0	B3		
0	IO_L04P_0	A3		
0	IO_L05N_0	G6		
0	IO_L05P_0	G7		
0	IO_L06N_0	E6		
0	IO_L06P_0	E7		
0	IO_L19N_0	B4		
0	IO_L19P_0	A4		
0	IO_L21N_0	B5		
0	IO_L21P_0/VREF_0	A5		
0	IO_L22N_0	B6		
0	IO_L22P_0	A6		
0	IO_L24N_0	A7		
0	IO_L24P_0	A8		
0	IO_L25N_0	E8	NC	NC
0	IO_L25P_0	D8	NC	NC
0	IO_L27N_0	G8	NC	NC
0	IO_L27P_0/VREF_0	F8	NC	NC
0	IO_L49N_0	C8		
0	IO_L49P_0	B8		
0	IO_L51N_0	D9		
0	IO_L51P_0/VREF_0	E9		
0	IO_L52N_0	F9		
0	IO_L52P_0	G9		
0	IO_L54N_0	B9		
0	IO_L54P_0	A9		
0	IO_L67N_0	C9		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
0	IO_L67P_0	C10		
0	IO_L69N_0	F10		
0	IO_L69P_0/VREF_0	G10		
0	IO_L70N_0	E10		
0	IO_L70P_0	D10		
0	IO_L72N_0	A10		
0	IO_L72P_0	A11		
0	IO_L73N_0	F11	NC	
0	IO_L73P_0	E11	NC	
0	IO_L75N_0	G11	NC	
0	IO_L75P_0/VREF_0	H11	NC	
0	IO_L76N_0	D11	NC	
0	IO_L76P_0	C11	NC	
0	IO_L78N_0	B11	NC	
0	IO_L78P_0	B12	NC	
0	IO_L91N_0/VREF_0	G12		
0	IO_L91P_0	H12		
0	IO_L92N_0	F12		
0	IO_L92P_0	E12		
0	IO_L93N_0	D12		
0	IO_L93P_0	C12		
0	IO_L94N_0/VREF_0	G13		
0	IO_L94P_0	H13		
0	IO_L95N_0/GCLK7P	F13		
0	IO_L95P_0/GCLK6S	E13		
0	IO_L96N_0/GCLK5P	D13		
0	IO_L96P_0/GCLK4S	C13		
1	IO_L96N_1/GCLK3P	H14		
1	IO_L96P_1/GCLK2S	H15		
1	IO_L95N_1/GCLK1P	G14		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	E14		
1	IO_L94P_1/VREF_1	D14		
1	IO_L93N_1	A12		
1	IO_L93P_1	A13		
1	IO_L92N_1	A14		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L92P_1	A15		
1	IO_L91N_1	B15		
1	IO_L91P_1/VREF_1	C15		
1	IO_L78N_1	D15	NC	
1	IO_L78P_1	E15	NC	
1	IO_L76N_1	F15	NC	
1	IO_L76P_1	G15	NC	
1	IO_L75N_1/VREF_1	G16	NC	
1	IO_L75P_1	F16	NC	
1	IO_L73N_1	A16	NC	
1	IO_L73P_1	A17	NC	
1	IO_L72N_1	B16		
1	IO_L72P_1	C16		
1	IO_L70N_1	D16		
1	IO_L70P_1	E16		
1	IO_L69N_1/VREF_1	C17		
1	IO_L69P_1	D17		
1	IO_L67N_1	H16		
1	IO_L67P_1	G17		
1	IO_L54N_1	E17		
1	IO_L54P_1	F17		
1	IO_L52N_1	A18		
1	IO_L52P_1	A19		
1	IO_L51N_1/VREF_1	E18		
1	IO_L51P_1	D18		
1	IO_L49N_1	B18		
1	IO_L49P_1	C18		
1	IO_L27N_1/VREF_1	F19	NC	NC
1	IO_L27P_1	F18	NC	NC
1	IO_L25N_1	G18	NC	NC
1	IO_L25P_1	G19	NC	NC
1	IO_L24N_1	B19		
1	IO_L24P_1	C19		
1	IO_L22N_1	D19		
1	IO_L22P_1	E19		
1	IO_L21N_1/VREF_1	A20		
1	IO_L21P_1	A21		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L19N_1	E20		
1	IO_L19P_1	F20		
1	IO_L06N_1	B21		
1	IO_L06P_1	B22		
1	IO_L05N_1	A22		
1	IO_L05P_1	A23		
1	IO_L04N_1	C21		
1	IO_L04P_1/VREF_1	D21		
1	IO_L03N_1/VRP_1	C20		
1	IO_L03P_1/VRN_1	D20		
1	IO_L02N_1	A24		
1	IO_L02P_1	A25		
1	IO_L01N_1	B23		
1	IO_L01P_1	B24		
2	IO_L01N_2	B26		
2	IO_L01P_2	C26		
2	IO_L02N_2/VRP_2	G20		
2	IO_L02P_2/VRN_2	H20		
2	IO_L03N_2	C25		
2	IO_L03P_2/VREF_2	D25		
2	IO_L04N_2	E23		
2	IO_L04P_2	E24		
2	IO_L06N_2	G21		
2	IO_L06P_2	G22		
2	IO_L19N_2	D26		
2	IO_L19P_2	E26		
2	IO_L21N_2	F23		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	E25		
2	IO_L22P_2	F25		
2	IO_L24N_2	H22		
2	IO_L24P_2	H21		
2	IO_L25N_2	G23	NC	NC
2	IO_L25P_2	G24	NC	NC
2	IO_L43N_2	F26		
2	IO_L43P_2	G26		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L96P_2	N23		
3	IO_L96N_3	N26		
3	IO_L96P_3	P26		
3	IO_L94N_3	P23		
3	IO_L94P_3	P22		
3	IO_L93N_3/VREF_3	P19		
3	IO_L93P_3	N19		
3	IO_L91N_3	P21		
3	IO_L91P_3	P20		
3	IO_L78N_3	R26	NC	
3	IO_L78P_3	R25	NC	
3	IO_L76N_3	R20	NC	
3	IO_L76P_3	R19	NC	
3	IO_L75N_3/VREF_3	R24	NC	
3	IO_L75P_3	R23	NC	
3	IO_L73N_3	R22	NC	
3	IO_L73P_3	R21	NC	
3	IO_L72N_3	T26		
3	IO_L72P_3	T25		
3	IO_L70N_3	T20		
3	IO_L70P_3	T19		
3	IO_L69N_3/VREF_3	T24		
3	IO_L69P_3	T23		
3	IO_L67N_3	T22		
3	IO_L67P_3	T21		
3	IO_L54N_3	U26		
3	IO_L54P_3	V26		
3	IO_L52N_3	U24		
3	IO_L52P_3	U23		
3	IO_L51N_3/VREF_3	U22		
3	IO_L51P_3	U21		
3	IO_L49N_3	V25		
3	IO_L49P_3	V24		
3	IO_L48N_3	V23		
3	IO_L48P_3	V22		
3	IO_L46N_3	W26		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	IO_L46P_3	Y26		
3	IO_L45N_3/VREF_3	U20		
3	IO_L45P_3	V20		
3	IO_L43N_3	W25		
3	IO_L43P_3	W24		
3	IO_L25N_3	V21	NC	NC
3	IO_L25P_3	W21	NC	NC
3	IO_L24N_3	AA26		
3	IO_L24P_3	AA25		
3	IO_L22N_3	Y24		
3	IO_L22P_3	Y23		
3	IO_L21N_3/VREF_3	W22		
3	IO_L21P_3	W23		
3	IO_L19N_3	AB26		
3	IO_L19P_3	AB25		
3	IO_L06N_3	AC26		
3	IO_L06P_3	AC25		
3	IO_L04N_3	AD26		
3	IO_L04P_3	AD25		
3	IO_L03N_3/VREF_3	AA24		
3	IO_L03P_3	AA23		
3	IO_L02N_3/VRP_3	AB24		
3	IO_L02P_3/VRN_3	AB23		
3	IO_L01N_3	Y22		
3	IO_L01P_3	AA22		
4	IO_L01N_4/DOUT	AD21		
4	IO_L01P_4/INIT_B	AC21		
4	IO_L02N_4/D0	Y20		
4	IO_L02P_4/D1	Y19		
4	IO_L03N_4/D2/ALT_VRP_4	AA20		
4	IO_L03P_4/D3/ALT_VRN_4	AB20		
4	IO_L04N_4/VREF_4	AC22		
4	IO_L04P_4	AE21		
4	IO_L05N_4/VRP_4	AE26		
4	IO_L05P_4/VRN_4	AF25		
4	IO_L06N_4	W20		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L06P_4	Y21		
4	IO_L19N_4	AE24		
4	IO_L19P_4	AF24		
4	IO_L21N_4	AE23		
4	IO_L21P_4/VREF_4	AF23		
4	IO_L22N_4	AE22		
4	IO_L22P_4	AF22		
4	IO_L24N_4	AF21		
4	IO_L24P_4	AF20		
4	IO_L25N_4	AA19	NC	NC
4	IO_L25P_4	AB19	NC	NC
4	IO_L27N_4	AD20	NC	NC
4	IO_L27P_4/VREF_4	AC20	NC	NC
4	IO_L28N_4	AC19	NC	NC
4	IO_L28P_4	AD19	NC	NC
4	IO_L49N_4	AE19		
4	IO_L49P_4	AF19		
4	IO_L51N_4	AA18		
4	IO_L51P_4/VREF_4	AB18		
4	IO_L52N_4	Y18		
4	IO_L52P_4	Y17		
4	IO_L54N_4	AC18		
4	IO_L54P_4	AD18		
4	IO_L67N_4	AE18		
4	IO_L67P_4	AF18		
4	IO_L69N_4	AA17		
4	IO_L69P_4/VREF_4	AB17		
4	IO_L70N_4	AC17		
4	IO_L70P_4	AD17		
4	IO_L72N_4	AF17		
4	IO_L72P_4	AF16		
4	IO_L73N_4	AB16	NC	
4	IO_L73P_4	AC16	NC	
4	IO_L75N_4	AA16	NC	
4	IO_L75P_4/VREF_4	Y16	NC	
4	IO_L76N_4	AD16	NC	
4	IO_L76P_4	AE16	NC	

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L78N_4	Y15	NC	
4	IO_L78P_4	AA15	NC	
4	IO_L91N_4/VREF_4	W15		
4	IO_L91P_4	W16		
4	IO_L92N_4	AB15		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AD15		
4	IO_L93P_4	AE15		
4	IO_L94N_4/VREF_4	W14		
4	IO_L94P_4	Y14		
4	IO_L95N_4/GCLK3S	AA14		
4	IO_L95P_4/GCLK2P	AB14		
4	IO_L96N_4/GCLK1S	AC14		
4	IO_L96P_4/GCLK0P	AD14		
5	IO_L96N_5/GCLK7S	AC13		
5	IO_L96P_5/GCLK6P	AB13		
5	IO_L95N_5/GCLK5S	AA13		
5	IO_L95P_5/GCLK4P	Y13		
5	IO_L94N_5	W13		
5	IO_L94P_5/VREF_5	W12		
5	IO_L93N_5	AF15		
5	IO_L93P_5	AF14		
5	IO_L92N_5	AF13		
5	IO_L92P_5	AF12		
5	IO_L91N_5	AE12		
5	IO_L91P_5/VREF_5	AD12		
5	IO_L78N_5	AC12	NC	
5	IO_L78P_5	AB12	NC	
5	IO_L76N_5	AA12	NC	
5	IO_L76P_5	Y12	NC	
5	IO_L75N_5/VREF_5	AF11	NC	
5	IO_L75P_5	AF10	NC	
5	IO_L73N_5	AE11	NC	
5	IO_L73P_5	AD11	NC	
5	IO_L72N_5	AC11		
5	IO_L72P_5	AB11		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L02P_5/D7	AC6		
5	IO_L01N_5/RDWR_B	AB6		
5	IO_L01P_5/CS_B	AC5		
6	IO_L01P_6	AF2		
6	IO_L01N_6	AE1		
6	IO_L02P_6/VRN_6	AB4		
6	IO_L02N_6/VRP_6	AB3		
6	IO_L03P_6	AD2		
6	IO_L03N_6/VREF_6	AD1		
6	IO_L04P_6	AC2		
6	IO_L04N_6	AC1		
6	IO_L06P_6	AB2		
6	IO_L06N_6	AB1		
6	IO_L19P_6	AA4		
6	IO_L19N_6	AA3		
6	IO_L21P_6	Y6		
6	IO_L21N_6/VREF_6	Y5		
6	IO_L22P_6	W6		
6	IO_L22N_6	W7		
6	IO_L24P_6	AA2		
6	IO_L24N_6	AA1		
6	IO_L25P_6	Y4	NC	NC
6	IO_L25N_6	Y3	NC	NC
6	IO_L43P_6	W5		
6	IO_L43N_6	W4		
6	IO_L45P_6	W2		
6	IO_L45N_6/VREF_6	W3		
6	IO_L46P_6	Y1		
6	IO_L46N_6	W1		
6	IO_L48P_6	V6		
6	IO_L48N_6	V7		
6	IO_L49P_6	V5		
6	IO_L49N_6	V4		
6	IO_L51P_6	V3		
6	IO_L51N_6/VREF_6	V2		
6	IO_L52P_6	V1		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
6	IO_L52N_6	U1		
6	IO_L54P_6	U7		
6	IO_L54N_6	T7		
6	IO_L67P_6	U4		
6	IO_L67N_6	U3		
6	IO_L69P_6	U6		
6	IO_L69N_6/VREF_6	U5		
6	IO_L70P_6	T5		
6	IO_L70N_6	T6		
6	IO_L72P_6	T8		
6	IO_L72N_6	R8		
6	IO_L73P_6	T2	NC	
6	IO_L73N_6	T1	NC	
6	IO_L75P_6	T4	NC	
6	IO_L75N_6/VREF_6	T3	NC	
6	IO_L76P_6	R6	NC	
6	IO_L76N_6	R5	NC	
6	IO_L78P_6	R4	NC	
6	IO_L78N_6	R3	NC	
6	IO_L91P_6	R2		
6	IO_L91N_6	R1		
6	IO_L93P_6	R7		
6	IO_L93N_6/VREF_6	P7		
6	IO_L94P_6	P6		
6	IO_L94N_6	P5		
6	IO_L96P_6	P4		
6	IO_L96N_6	P3		
7	IO_L96P_7	P1		
7	IO_L96N_7	N1		
7	IO_L94P_7	N4		
7	IO_L94N_7	N5		
7	IO_L93P_7/VREF_7	N6		
7	IO_L93N_7	N7		
7	IO_L91P_7	P8		
7	IO_L91N_7	N8		
7	IO_L78P_7	M1	NC	

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L21P_7/VREF_7	F3		
7	IO_L21N_7	F2		
7	IO_L19P_7	H6		
7	IO_L19N_7	H7		
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	D1		
7	IO_L04N_7	D2		
7	IO_L03P_7/VREF_7	C1		
7	IO_L03N_7	C2		
7	IO_L02P_7/VRN_7	E3		
7	IO_L02N_7/VRP_7	E4		
7	IO_L01P_7	G5		
7	IO_L01N_7	F4		
0	VCCO_0	J13		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	H10		
0	VCCO_0	H9		
0	VCCO_0	B10		
0	VCCO_0	B7		
1	VCCO_1	B17		
1	VCCO_1	J16		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	H18		
1	VCCO_1	H17		
1	VCCO_1	B20		
2	VCCO_2	N18		
2	VCCO_2	M18		
2	VCCO_2	L18		
2	VCCO_2	K25		
2	VCCO_2	K19		
2	VCCO_2	J19		
2	VCCO_2	G25		
3	VCCO_3	Y25		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	VCCO_3	V19		
3	VCCO_3	U25		
3	VCCO_3	U19		
3	VCCO_3	T18		
3	VCCO_3	R18		
3	VCCO_3	P18		
4	VCCO_4	AE20		
4	VCCO_4	AE17		
4	VCCO_4	W18		
4	VCCO_4	W17		
4	VCCO_4	V16		
4	VCCO_4	V15		
4	VCCO_4	V14		
5	VCCO_5	AE10		
5	VCCO_5	AE7		
5	VCCO_5	W10		
5	VCCO_5	W9		
5	VCCO_5	V13		
5	VCCO_5	V12		
5	VCCO_5	V11		
6	VCCO_6	Y2		
6	VCCO_6	V8		
6	VCCO_6	U8		
6	VCCO_6	U2		
6	VCCO_6	T9		
6	VCCO_6	R9		
6	VCCO_6	P9		
7	VCCO_7	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	K8		
7	VCCO_7	K2		
7	VCCO_7	J8		
7	VCCO_7	G2		
NA	CCLK	AB21		
NA	PROG_B	C4		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	DONE	AD22		
NA	M0	AD4		
NA	M1	AA5		
NA	M2	AD5		
NA	HSWAP_EN	D5		
NA	TCK	E21		
NA	TDI	F5		
NA	TDO	F22		
NA	TMS	D22		
NA	PWRDWN_B	AD23		
NA	DXN	F7		
NA	DXP	C5		
NA	VBATT	C23		
NA	RSVD	C22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC24		
NA	VCCAUX	AC3		
NA	VCCAUX	P24		
NA	VCCAUX	N3		
NA	VCCAUX	D24		
NA	VCCAUX	D3		
NA	VCCAUX	C14		
NA	VCCINT	W19		
NA	VCCINT	W8		
NA	VCCINT	V18		
NA	VCCINT	V17		
NA	VCCINT	V10		
NA	VCCINT	V9		
NA	VCCINT	U18		
NA	VCCINT	U9		
NA	VCCINT	K18		
NA	VCCINT	K9		
NA	VCCINT	J18		
NA	VCCINT	J17		
NA	VCCINT	J10		
NA	VCCINT	J9		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	VCCINT	H19		
NA	VCCINT	H8		
NA	GND	AF26		
NA	GND	AF1		
NA	GND	AE25		
NA	GND	AE14		
NA	GND	AE13		
NA	GND	AE2		
NA	GND	AD24		
NA	GND	AD3		
NA	GND	AC23		
NA	GND	AC4		
NA	GND	AB22		
NA	GND	AB5		
NA	GND	AA21		
NA	GND	AA6		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U11		
NA	GND	U10		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		
NA	GND	T13		
NA	GND	T12		
NA	GND	T11		
NA	GND	T10		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		

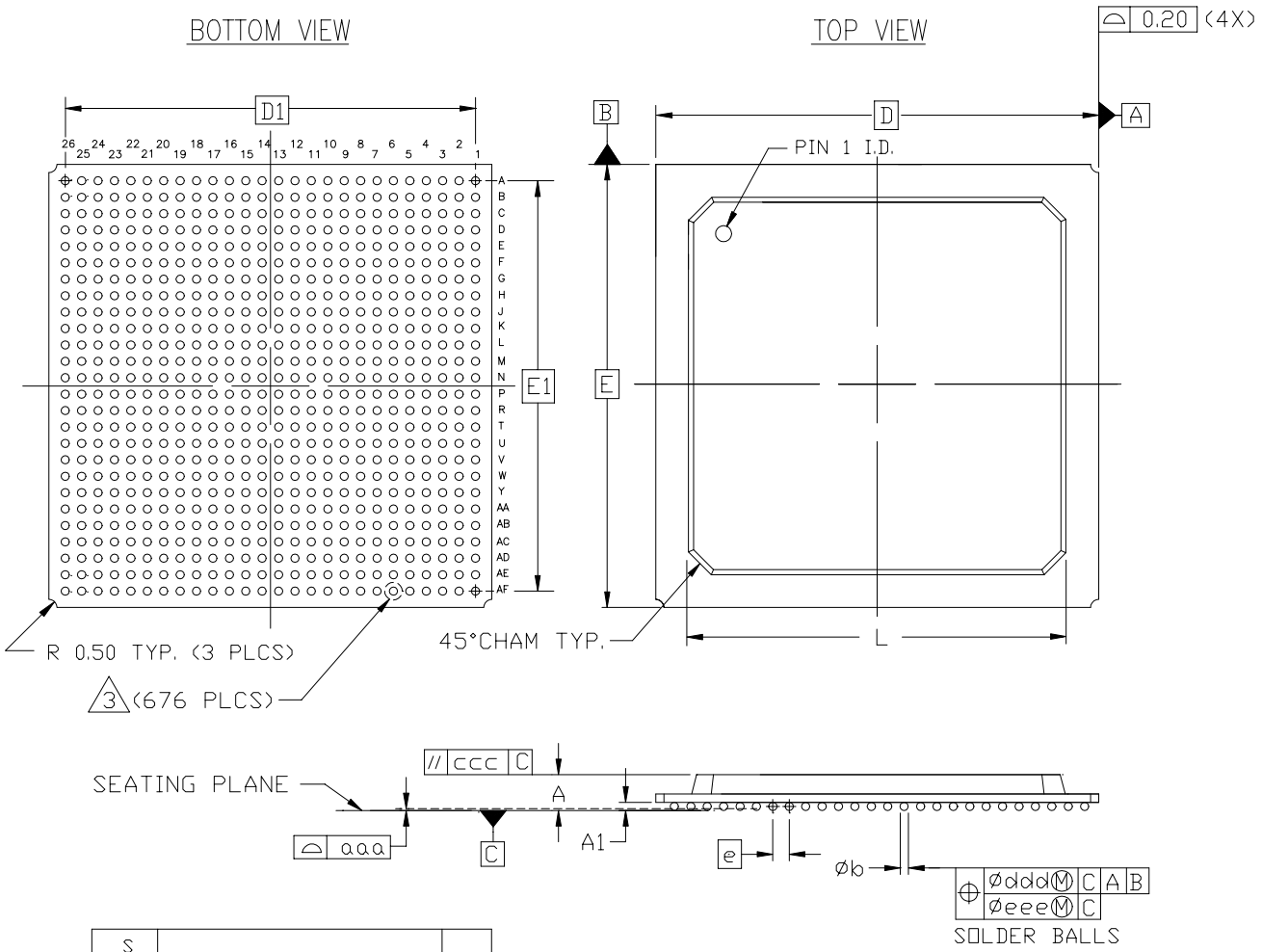
Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	R12		
NA	GND	R11		
NA	GND	R10		
NA	GND	P25		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P2		
NA	GND	N25		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N2		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	M10		
NA	GND	L17		
NA	GND	L16		
NA	GND	L15		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		

Table 8: **FG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	L11		
NA	GND	L10		
NA	GND	K17		
NA	GND	K16		
NA	GND	K15		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	F21		
NA	GND	F6		
NA	GND	E22		
NA	GND	E5		
NA	GND	D23		
NA	GND	D4		
NA	GND	C24		
NA	GND	C3		
NA	GND	B25		
NA	GND	B14		
NA	GND	B13		
NA	GND	B2		
NA	GND	A26		
NA	GND	A1		

FG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		2.25	2.60	
A_1	0.40	0.50	0.60	
D/E	27.00 BSC			
D_1/E_1	25.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
L			25.70	
M	26			2
REF.	JEDEC MO-151-AAL-1			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. LAND PAD OPENING – SOLDER MASK DEFINED ø0.485mm (0.019")

Figure 4: **FG676 Fine-Pitch BGA Package Specifications**

BG575 Standard BGA Package

As shown in Table 9, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the BG575 BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the **BG575 Standard BGA Package Specifications (1.27mm pitch)**.

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L01N_0	A3		
0	IO_L01P_0	A4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	E6		
0	IO_L03P_0/VRN_0	D6		
0	IO_L04N_0/VREF_0	F7		
0	IO_L04P_0	E7		
0	IO_L05N_0	G8		
0	IO_L05P_0	H9		
0	IO_L06N_0	A5		
0	IO_L06P_0	A6		
0	IO_L19N_0	B5		
0	IO_L19P_0	B6		
0	IO_L21N_0	D7		
0	IO_L21P_0/VREF_0	C7		
0	IO_L22N_0	F8		
0	IO_L22P_0	E8		
0	IO_L24N_0	G9		
0	IO_L24P_0	F9		
0	IO_L49N_0	G10		
0	IO_L49P_0	H10		
0	IO_L51N_0	B7		
0	IO_L51P_0/VREF_0	B8		
0	IO_L52N_0	D8		
0	IO_L52P_0	C8		
0	IO_L54N_0	E9		
0	IO_L54P_0	D9		
0	IO_L67N_0	A8	NC	
0	IO_L67P_0	A9	NC	
0	IO_L69N_0	C9	NC	

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L69P_0/VREF_0	B9	NC	
0	IO_L70N_0	F10	NC	
0	IO_L70P_0	E10	NC	
0	IO_L72N_0	A10	NC	
0	IO_L72P_0	A11	NC	
0	IO_L73N_0	C10	NC	NC
0	IO_L73P_0	B10	NC	NC
0	IO_L91N_0/VREF_0	D11		
0	IO_L91P_0	C11		
0	IO_L92N_0	G11		
0	IO_L92P_0	E11		
0	IO_L93N_0	C12		
0	IO_L93P_0	B12		
0	IO_L94N_0/VREF_0	E12		
0	IO_L94P_0	D12		
0	IO_L95N_0/GCLK7P	G12		
0	IO_L95P_0/GCLK6S	F12		
0	IO_L96N_0/GCLK5P	H11		
0	IO_L96P_0/GCLK4S	H12		
1	IO_L96N_1/GCLK3P	A13		
1	IO_L96P_1/GCLK2S	A14		
1	IO_L95N_1/GCLK1P	B13		
1	IO_L95P_1/GCLK0S	C13		
1	IO_L94N_1	D13		
1	IO_L94P_1/VREF_1	E13		
1	IO_L93N_1	F13		
1	IO_L93P_1	G13		
1	IO_L92N_1	H13		
1	IO_L92P_1	H14		
1	IO_L91N_1	C14		
1	IO_L91P_1/VREF_1	D14		
1	IO_L73N_1	E14	NC	NC
1	IO_L73P_1	G14	NC	NC
1	IO_L72N_1	A15	NC	
1	IO_L72P_1	A16	NC	

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	IO_L70N_1	B15	NC	
1	IO_L70P_1	C15	NC	
1	IO_L69N_1/VREF_1	E15	NC	
1	IO_L69P_1	F15	NC	
1	IO_L67N_1	G15	NC	
1	IO_L67P_1	H15	NC	
1	IO_L54N_1	B16		
1	IO_L54P_1	C16		
1	IO_L52N_1	D16		
1	IO_L52P_1	E16		
1	IO_L51N_1/VREF_1	F16		
1	IO_L51P_1	G16		
1	IO_L49N_1	A17		
1	IO_L49P_1	A19		
1	IO_L24N_1	B17		
1	IO_L24P_1	B18		
1	IO_L22N_1	C17		
1	IO_L22P_1	D17		
1	IO_L21N_1/VREF_1	F17		
1	IO_L21P_1	E17		
1	IO_L19N_1	A20		
1	IO_L19P_1	A21		
1	IO_L06N_1	B19		
1	IO_L06P_1	B20		
1	IO_L05N_1	C18		
1	IO_L05P_1	D18		
1	IO_L04N_1	C20		
1	IO_L04P_1/VREF_1	D20		
1	IO_L03N_1/VRP_1	D19		
1	IO_L03P_1/VRN_1	E19		
1	IO_L02N_1	E18		
1	IO_L02P_1	F18		
1	IO_L01N_1	H16		
1	IO_L01P_1	G17		
2	IO_L01N_2	D22		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L69P_2/VREF_2	L18	NC	
2	IO_L70N_2	K23	NC	
2	IO_L70P_2	L24	NC	
2	IO_L72N_2	K22	NC	
2	IO_L72P_2	L22	NC	
2	IO_L73N_2	L21	NC	NC
2	IO_L73P_2	L20	NC	NC
2	IO_L91N_2	M23		
2	IO_L91P_2	N24		
2	IO_L93N_2	M21		
2	IO_L93P_2/VREF_2	M22		
2	IO_L94N_2	M19		
2	IO_L94P_2	M20		
2	IO_L96N_2	M17		
2	IO_L96P_2	M18		
3	IO_L96N_3	N23		
3	IO_L96P_3	N22		
3	IO_L94N_3	N20		
3	IO_L94P_3	N21		
3	IO_L93N_3/VREF_3	N19		
3	IO_L93P_3	N18		
3	IO_L91N_3	N17		
3	IO_L91P_3	P17		
3	IO_L73N_3	P24	NC	NC
3	IO_L73P_3	R24	NC	NC
3	IO_L72N_3	R23	NC	
3	IO_L72P_3	R22	NC	
3	IO_L70N_3	P22	NC	
3	IO_L70P_3	P21	NC	
3	IO_L69N_3/VREF_3	P20	NC	
3	IO_L69P_3	P18	NC	
3	IO_L67N_3	T24	NC	
3	IO_L67P_3	U24	NC	
3	IO_L54N_3	T23		
3	IO_L54P_3	T22		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
3	IO_L52N_3	T21		
3	IO_L52P_3	T20		
3	IO_L51N_3/VREF_3	R20		
3	IO_L51P_3	R19		
3	IO_L49N_3	W24		
3	IO_L49P_3	W23		
3	IO_L48N_3	U23		
3	IO_L48P_3	V23		
3	IO_L46N_3	U22		
3	IO_L46P_3	U21		
3	IO_L45N_3/VREF_3	V22		
3	IO_L45P_3	V21		
3	IO_L43N_3	U19		
3	IO_L43P_3	U20		
3	IO_L24N_3	T19		
3	IO_L24P_3	T18		
3	IO_L22N_3	R18		
3	IO_L22P_3	R17		
3	IO_L21N_3/VREF_3	Y24		
3	IO_L21P_3	Y23		
3	IO_L19N_3	AA24		
3	IO_L19P_3	AB24		
3	IO_L06N_3	AA23		
3	IO_L06P_3	AA22		
3	IO_L04N_3	Y22		
3	IO_L04P_3	Y21		
3	IO_L03N_3/VREF_3	W21		
3	IO_L03P_3	W20		
3	IO_L02N_3/VRP_3	V20		
3	IO_L02P_3/VRN_3	V19		
3	IO_L01N_3	U18		
3	IO_L01P_3	T17		
4	IO_L01N_4/DOUT	AD22		
4	IO_L01P_4/INIT_B	AD21		
4	IO_L02N_4/D0	AA20		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L02P_4/D1	AB20		
4	IO_L03N_4/D2/ALT_VRP_4	Y19		
4	IO_L03P_4/D3/ALT_VRN_4	AA19		
4	IO_L04N_4/VREF_4	W18		
4	IO_L04P_4	Y18		
4	IO_L05N_4/VRP_4	U16		
4	IO_L05P_4/VRN_4	V17		
4	IO_L06N_4	AD20		
4	IO_L06P_4	AD19		
4	IO_L19N_4	AC20		
4	IO_L19P_4	AC19		
4	IO_L21N_4	AA18		
4	IO_L21P_4/VREF_4	AB18		
4	IO_L22N_4	AC18		
4	IO_L22P_4	AC17		
4	IO_L24N_4	AA17		
4	IO_L24P_4	AB17		
4	IO_L49N_4	Y17		
4	IO_L49P_4	W17		
4	IO_L51N_4	V16		
4	IO_L51P_4/VREF_4	W16		
4	IO_L52N_4	AD17		
4	IO_L52P_4	AD16		
4	IO_L54N_4	AB16		
4	IO_L54P_4	AC16		
4	IO_L67N_4	Y16	NC	
4	IO_L67P_4	AA16	NC	
4	IO_L69N_4	W15	NC	
4	IO_L69P_4/VREF_4	Y15	NC	
4	IO_L70N_4	U15	NC	
4	IO_L70P_4	V15	NC	
4	IO_L72N_4	AD15	NC	
4	IO_L72P_4	AD14	NC	
4	IO_L73N_4	AB15	NC	NC
4	IO_L73P_4	AC15	NC	NC
4	IO_L91N_4/VREF_4	AA14		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L91P_4	AB14		
4	IO_L92N_4	V14		
4	IO_L92P_4	Y14		
4	IO_L93N_4	AB13		
4	IO_L93P_4	AC13		
4	IO_L94N_4/VREF_4	Y13		
4	IO_L94P_4	AA13		
4	IO_L95N_4/GCLK3S	V13		
4	IO_L95P_4/GCLK2P	W13		
4	IO_L96N_4/GCLK1S	U14		
4	IO_L96P_4/GCLK0P	U13		
5	IO_L96N_5/GCLK7S	AD12		
5	IO_L96P_5/GCLK6P	AD11		
5	IO_L95N_5/GCLK5S	AC12		
5	IO_L95P_5/GCLK4P	AB12		
5	IO_L94N_5	AA12		
5	IO_L94P_5/VREF_5	Y12		
5	IO_L93N_5	W12		
5	IO_L93P_5	V12		
5	IO_L92N_5	U12		
5	IO_L92P_5	U11		
5	IO_L91N_5	AB11		
5	IO_L91P_5/VREF_5	AA11		
5	IO_L73N_5	Y11	NC	NC
5	IO_L73P_5	V11	NC	NC
5	IO_L72N_5	AD10	NC	
5	IO_L72P_5	AD9	NC	
5	IO_L70N_5	AC10	NC	
5	IO_L70P_5	AB10	NC	
5	IO_L69N_5/VREF_5	Y10	NC	
5	IO_L69P_5	W10	NC	
5	IO_L67N_5	V10	NC	
5	IO_L67P_5	U10	NC	
5	IO_L54N_5	AC9		
5	IO_L54P_5	AB9		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
5	IO_L52N_5	AA9		
5	IO_L52P_5	Y9		
5	IO_L51N_5/VREF_5	W9		
5	IO_L51P_5	V9		
5	IO_L49N_5	AD8		
5	IO_L49P_5	AD6		
5	IO_L24N_5	AC8		
5	IO_L24P_5	AC7		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	W8		
5	IO_L21P_5	Y8		
5	IO_L19N_5	AD5		
5	IO_L19P_5	AD4		
5	IO_L06N_5	AC6		
5	IO_L06P_5	AC5		
5	IO_L05N_5/VRP_5	AB7		
5	IO_L05P_5/VRN_5	AA7		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	AA6		
5	IO_L03P_5/D5/ALT_VRN_5	Y6		
5	IO_L02N_5/D6	Y7		
5	IO_L02P_5/D7	W7		
5	IO_L01N_5/RDWR_B	V8		
5	IO_L01P_5/CS_B	U9		
6	IO_L01P_6	AB2		
6	IO_L01N_6	AB1		
6	IO_L02P_6/VRN_6	AA3		
6	IO_L02N_6/VRP_6	AA2		
6	IO_L03P_6	Y4		
6	IO_L03N_6/VREF_6	Y3		
6	IO_L04P_6	W4		
6	IO_L04N_6	W5		
6	IO_L06P_6	V5		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L06N_6	V6		
6	IO_L19P_6	U7		
6	IO_L19N_6	T8		
6	IO_L21P_6	AA1		
6	IO_L21N_6/VREF_6	Y2		
6	IO_L22P_6	Y1		
6	IO_L22N_6	W1		
6	IO_L24P_6	W2		
6	IO_L24N_6	V2		
6	IO_L43P_6	V4		
6	IO_L43N_6	V3		
6	IO_L45P_6	U6		
6	IO_L45N_6/VREF_6	U5		
6	IO_L46P_6	T7		
6	IO_L46N_6	T6		
6	IO_L48P_6	R8		
6	IO_L48N_6	R7		
6	IO_L49P_6	U2		
6	IO_L49N_6	U1		
6	IO_L51P_6	U4		
6	IO_L51N_6/VREF_6	U3		
6	IO_L52P_6	T1		
6	IO_L52N_6	R1		
6	IO_L54P_6	T3		
6	IO_L54N_6	T2		
6	IO_L67P_6	T5	NC	
6	IO_L67N_6	T4	NC	
6	IO_L69P_6	R6	NC	
6	IO_L69N_6/VREF_6	R5	NC	
6	IO_L70P_6	P8	NC	
6	IO_L70N_6	P7	NC	
6	IO_L72P_6	R2	NC	
6	IO_L72N_6	P1	NC	
6	IO_L73P_6	R3	NC	NC
6	IO_L73N_6	P3	NC	NC
6	IO_L91P_6	P5		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L91N_6	P4		
6	IO_L93P_6	N4		
6	IO_L93N_6/VREF_6	N3		
6	IO_L94P_6	N6		
6	IO_L94N_6	N5		
6	IO_L96P_6	N8		
6	IO_L96N_6	N7		
7	IO_L96P_7	N2		
7	IO_L96N_7	M1		
7	IO_L94P_7	M2		
7	IO_L94N_7	M3		
7	IO_L93P_7/VREF_7	M4		
7	IO_L93N_7	M5		
7	IO_L91P_7	M6		
7	IO_L91N_7	M7		
7	IO_L73P_7	M8	NC	NC
7	IO_L73N_7	L8	NC	NC
7	IO_L72P_7	L1	NC	
7	IO_L72N_7	K1	NC	
7	IO_L70P_7	K2	NC	
7	IO_L70N_7	K3	NC	
7	IO_L69P_7/VREF_7	L3	NC	
7	IO_L69N_7	L4	NC	
7	IO_L67P_7	L5	NC	
7	IO_L67N_7	L7	NC	
7	IO_L54P_7	J1		
7	IO_L54N_7	H1		
7	IO_L52P_7	J2		
7	IO_L52N_7	J3		
7	IO_L51P_7/VREF_7	J4		
7	IO_L51N_7	J5		
7	IO_L49P_7	K5		
7	IO_L49N_7	K6		
7	IO_L48P_7	F1		
7	IO_L48N_7	F2		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	IO_L46P_7	H2		
7	IO_L46N_7	G2		
7	IO_L45P_7/VREF_7	H3		
7	IO_L45N_7	H4		
7	IO_L43P_7	G3		
7	IO_L43N_7	G4		
7	IO_L24P_7	H5		
7	IO_L24N_7	H6		
7	IO_L22P_7	J6		
7	IO_L22N_7	J7		
7	IO_L21P_7/VREF_7	K7		
7	IO_L21N_7	K8		
7	IO_L19P_7	E1		
7	IO_L19N_7	E2		
7	IO_L06P_7	D2		
7	IO_L06N_7	D3		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	F4		
7	IO_L03N_7	F5		
7	IO_L02P_7/VRN_7	G5		
7	IO_L02N_7/VRP_7	G6		
7	IO_L01P_7	H7		
7	IO_L01N_7	J8		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	J10		
0	VCCO_0	F11		
0	VCCO_0	C6		
0	VCCO_0	B11		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	J13		
1	VCCO_1	F14		
1	VCCO_1	C19		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	VCCO_1	B14		
2	VCCO_2	M16		
2	VCCO_2	L23		
2	VCCO_2	L19		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	F22		
3	VCCO_3	W22		
3	VCCO_3	R16		
3	VCCO_3	P23		
3	VCCO_3	P19		
3	VCCO_3	P16		
3	VCCO_3	N16		
4	VCCO_4	AC14		
4	VCCO_4	AB19		
4	VCCO_4	W14		
4	VCCO_4	T15		
4	VCCO_4	T14		
4	VCCO_4	T13		
5	VCCO_5	AC11		
5	VCCO_5	AB6		
5	VCCO_5	W11		
5	VCCO_5	T12		
5	VCCO_5	T11		
5	VCCO_5	T10		
6	VCCO_6	W3		
6	VCCO_6	R9		
6	VCCO_6	P9		
6	VCCO_6	P6		
6	VCCO_6	P2		
6	VCCO_6	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	L6		
7	VCCO_7	L2		
7	VCCO_7	K9		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	VCCO_7	F3		
NA	CCLK	AB23		
NA	PROG_B	C1		
NA	DONE	AB21		
NA	M0	AC4		
NA	M1	AB4		
NA	M2	AD3		
NA	HSWAP_EN	C2		
NA	TCK	C23		
NA	TDI	D1		
NA	TDO	C24		
NA	TMS	C21		
NA	PWRDWN_B	AC21		
NA	DXN	B4		
NA	DXP	C4		
NA	VBATT	B21		
NA	RSVD	A22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC22		
NA	VCCAUX	AC3		
NA	VCCAUX	N1		
NA	VCCAUX	M24		
NA	VCCAUX	B22		
NA	VCCAUX	B3		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U8		
NA	VCCINT	T16		
NA	VCCINT	T9		
NA	VCCINT	R15		
NA	VCCINT	R14		
NA	VCCINT	R13		
NA	VCCINT	R12		
NA	VCCINT	R11		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	VCCINT	R10		
NA	VCCINT	P15		
NA	VCCINT	P10		
NA	VCCINT	N15		
NA	VCCINT	N10		
NA	VCCINT	M15		
NA	VCCINT	M10		
NA	VCCINT	L15		
NA	VCCINT	L10		
NA	VCCINT	K15		
NA	VCCINT	K14		
NA	VCCINT	K13		
NA	VCCINT	K12		
NA	VCCINT	K11		
NA	VCCINT	K10		
NA	VCCINT	J16		
NA	VCCINT	J9		
NA	VCCINT	H17		
NA	VCCINT	H8		
NA	GND	AD24		
NA	GND	AD23		
NA	GND	AD18		
NA	GND	AD7		
NA	GND	AD2		
NA	GND	AD1		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC2		
NA	GND	AC1		
NA	GND	AB22		
NA	GND	AB3		
NA	GND	AA21		
NA	GND	AA15		
NA	GND	AA10		
NA	GND	AA4		
NA	GND	Y20		

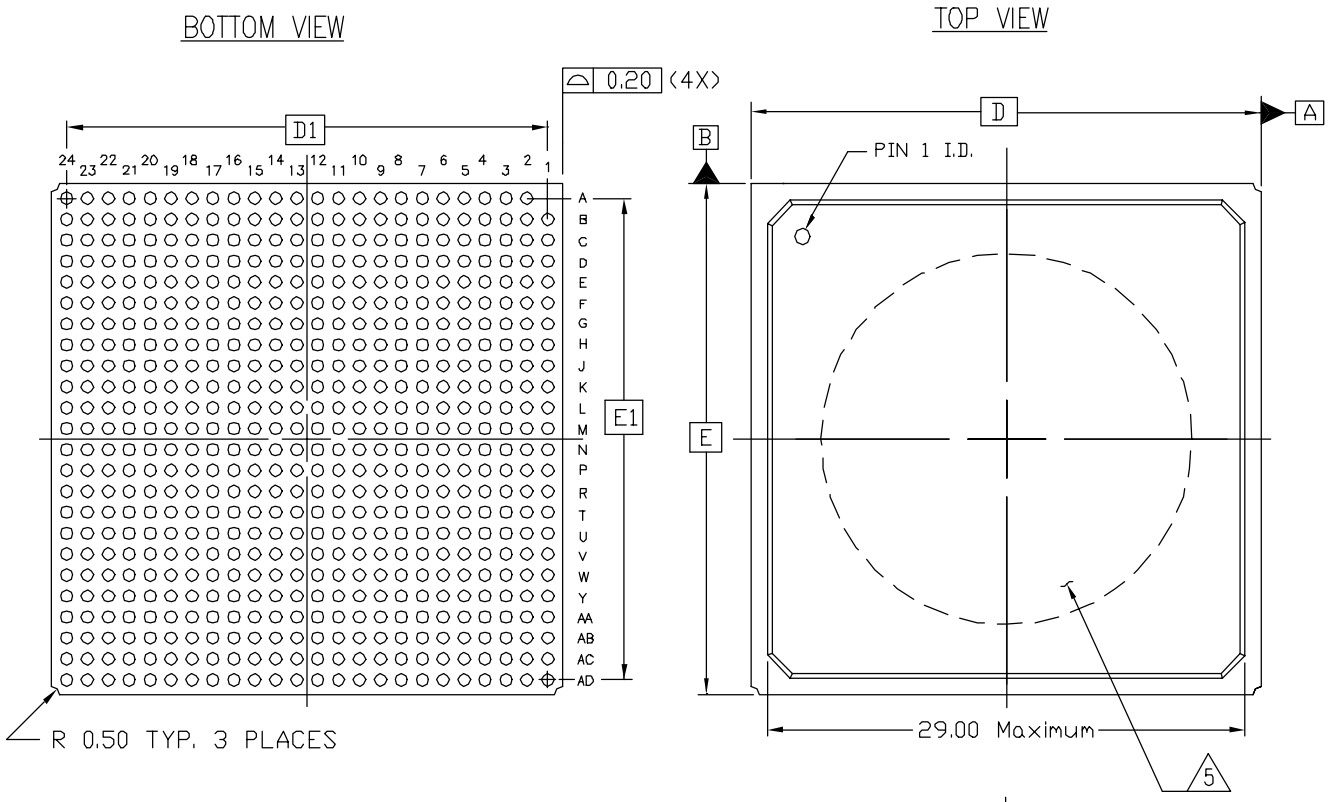
Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

Table 9: **BG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	D15		
NA	GND	D10		
NA	GND	D4		
NA	GND	C22		
NA	GND	C3		
NA	GND	B24		
NA	GND	B23		
NA	GND	B2		
NA	GND	B1		
NA	GND	A24		
NA	GND	A23		
NA	GND	A18		
NA	GND	A7		
NA	GND	A2		

BG575 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 BAN–1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

Figure 5: **BG575 Standard BGA Package Specifications**

BG728 Standard BGA Package

As shown in Table 10, XC2V2000 and XC2V3000 Virtex-II devices are available in the BG728 BGA package. Pins in the XC2V2000 and XC2V3000 devices are the same, except for the pin differences in the XC2V2000 device, shown in the No Connect column. Following this table are the **BG728 Standard BGA Package Specifications (1.27mm pitch)**.

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L01N_0	B3	
0	IO_L01P_0	A3	
0	IO_L02N_0	B4	
0	IO_L02P_0	A4	
0	IO_L03N_0/VRP_0	C5	
0	IO_L03P_0/VRN_0	C6	
0	IO_L04N_0/VREF_0	B5	
0	IO_L04P_0	A5	
0	IO_L05N_0	E6	
0	IO_L05P_0	D6	
0	IO_L06N_0	B6	
0	IO_L06P_0	A6	
0	IO_L19N_0	E7	
0	IO_L19P_0	D8	
0	IO_L21N_0	F8	
0	IO_L21P_0/VREF_0	E8	
0	IO_L22N_0	C7	
0	IO_L22P_0	C8	
0	IO_L24N_0	B7	
0	IO_L24P_0	A7	
0	IO_L25N_0	H9	NC
0	IO_L25P_0	J9	NC
0	IO_L27N_0	F9	NC
0	IO_L27P_0/VREF_0	G9	NC
0	IO_L28N_0	E9	NC
0	IO_L28P_0	D9	NC
0	IO_L30N_0	C9	NC
0	IO_L30P_0	B9	NC
0	IO_L49N_0	A8	
0	IO_L49P_0	A9	
0	IO_L51N_0	G10	
0	IO_L51P_0/VREF_0	H10	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L52N_0	F10	
0	IO_L52P_0	E10	
0	IO_L54N_0	D10	
0	IO_L54P_0	C10	
0	IO_L67N_0	B10	
0	IO_L67P_0	A10	
0	IO_L69N_0	G11	
0	IO_L69P_0/VREF_0	H11	
0	IO_L70N_0	F11	
0	IO_L70P_0	F12	
0	IO_L72N_0	D11	
0	IO_L72P_0	C11	
0	IO_L73N_0	B11	
0	IO_L73P_0	A11	
0	IO_L75N_0	H12	
0	IO_L75P_0/VREF_0	J12	
0	IO_L76N_0	E12	
0	IO_L76P_0	D12	
0	IO_L78N_0	B12	
0	IO_L78P_0	A12	
0	IO_L91N_0/VREF_0	J13	
0	IO_L91P_0	H13	
0	IO_L92N_0	G13	
0	IO_L92P_0	F13	
0	IO_L93N_0	E13	
0	IO_L93P_0	D13	
0	IO_L94N_0/VREF_0	B13	
0	IO_L94P_0	A13	
0	IO_L95N_0/GCLK7P	C13	
0	IO_L95P_0/GCLK6S	C14	
0	IO_L96N_0/GCLK5P	F14	
0	IO_L96P_0/GCLK4S	E14	
1	IO_L96N_1/GCLK3P	G14	
1	IO_L96P_1/GCLK2S	H14	
1	IO_L95N_1/GCLK1P	A15	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L95P_1/GCLK0S	B15	
1	IO_L94N_1	C15	
1	IO_L94P_1/VREF_1	D15	
1	IO_L93N_1	E15	
1	IO_L93P_1	F15	
1	IO_L92N_1	G15	
1	IO_L92P_1	H15	
1	IO_L91N_1	J15	
1	IO_L91P_1/VREF_1	J16	
1	IO_L78N_1	A16	
1	IO_L78P_1	B16	
1	IO_L76N_1	D16	
1	IO_L76P_1	E16	
1	IO_L75N_1/VREF_1	F16	
1	IO_L75P_1	F17	
1	IO_L73N_1	H16	
1	IO_L73P_1	H17	
1	IO_L72N_1	A17	
1	IO_L72P_1	B17	
1	IO_L70N_1	C17	
1	IO_L70P_1	D17	
1	IO_L69N_1/VREF_1	G18	
1	IO_L69P_1	G17	
1	IO_L67N_1	A18	
1	IO_L67P_1	B18	
1	IO_L54N_1	C18	
1	IO_L54P_1	D18	
1	IO_L52N_1	E18	
1	IO_L52P_1	F18	
1	IO_L51N_1/VREF_1	H19	
1	IO_L51P_1	H18	
1	IO_L49N_1	A19	
1	IO_L49P_1	A20	
1	IO_L30N_1	B19	NC
1	IO_L30P_1	C19	NC
1	IO_L28N_1	D19	NC

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L28P_1	E19	NC
1	IO_L27N_1/VREF_1	F19	NC
1	IO_L27P_1	G19	NC
1	IO_L25N_1	J19	NC
1	IO_L25P_1	J20	NC
1	IO_L24N_1	C20	
1	IO_L24P_1	C21	
1	IO_L22N_1	D20	
1	IO_L22P_1	E21	
1	IO_L21N_1/VREF_1	E20	
1	IO_L21P_1	F20	
1	IO_L19N_1	A21	
1	IO_L19P_1	B21	
1	IO_L06N_1	A22	
1	IO_L06P_1	B22	
1	IO_L05N_1	C22	
1	IO_L05P_1	C23	
1	IO_L04N_1	D22	
1	IO_L04P_1/VREF_1	E22	
1	IO_L03N_1/VRP_1	A23	
1	IO_L03P_1/VRN_1	B23	
1	IO_L02N_1	A24	
1	IO_L02P_1	B24	
1	IO_L01N_1	A25	
1	IO_L01P_1	B25	
2	IO_L01N_2	C27	
2	IO_L01P_2	D27	
2	IO_L02N_2/VRP_2	D25	
2	IO_L02P_2/VRN_2	D26	
2	IO_L03N_2	E24	
2	IO_L03P_2/VREF_2	E25	
2	IO_L04N_2	E26	
2	IO_L04P_2	E27	
2	IO_L06N_2	F23	
2	IO_L06P_2	F24	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L19N_2	F25	
2	IO_L19P_2	F26	
2	IO_L21N_2	F27	
2	IO_L21P_2/VREF_2	G27	
2	IO_L22N_2	G23	
2	IO_L22P_2	H23	
2	IO_L24N_2	G25	
2	IO_L24P_2	G26	
2	IO_L25N_2	H21	NC
2	IO_L25P_2	J21	NC
2	IO_L27N_2	H22	NC
2	IO_L27P_2/VREF_2	J22	NC
2	IO_L28N_2	H24	NC
2	IO_L28P_2	H25	NC
2	IO_L30N_2	H27	NC
2	IO_L30P_2	J27	NC
2	IO_L43N_2	J23	
2	IO_L43P_2	J24	
2	IO_L45N_2	J25	
2	IO_L45P_2/VREF_2	J26	
2	IO_L46N_2	K20	
2	IO_L46P_2	K21	
2	IO_L48N_2	K22	
2	IO_L48P_2	K23	
2	IO_L49N_2	K24	
2	IO_L49P_2	K25	
2	IO_L51N_2	K26	
2	IO_L51P_2/VREF_2	K27	
2	IO_L52N_2	L20	
2	IO_L52P_2	M20	
2	IO_L54N_2	L21	
2	IO_L54P_2	L22	
2	IO_L67N_2	L24	
2	IO_L67P_2	L25	
2	IO_L69N_2	L26	
2	IO_L69P_2/VREF_2	L27	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L70N_2	M19	
2	IO_L70P_2	N19	
2	IO_L72N_2	M22	
2	IO_L72P_2	M23	
2	IO_L73N_2	M24	
2	IO_L73P_2	N24	
2	IO_L75N_2	M26	
2	IO_L75P_2/VREF_2	M27	
2	IO_L76N_2	N20	
2	IO_L76P_2	N21	
2	IO_L78N_2	N22	
2	IO_L78P_2	N23	
2	IO_L91N_2	N25	
2	IO_L91P_2	P25	
2	IO_L93N_2	N26	
2	IO_L93P_2/VREF_2	N27	
2	IO_L94N_2	P20	
2	IO_L94P_2	P21	
2	IO_L96N_2	P22	
2	IO_L96P_2	P23	
3	IO_L96N_3	R27	
3	IO_L96P_3	R26	
3	IO_L94N_3	R25	
3	IO_L94P_3	R24	
3	IO_L93N_3/VREF_3	R23	
3	IO_L93P_3	T23	
3	IO_L91N_3	R22	
3	IO_L91P_3	R21	
3	IO_L78N_3	R20	
3	IO_L78P_3	R19	
3	IO_L76N_3	T27	
3	IO_L76P_3	T26	
3	IO_L75N_3/VREF_3	T24	
3	IO_L75P_3	U24	
3	IO_L73N_3	T22	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L73P_3	U22	
3	IO_L72N_3	T20	
3	IO_L72P_3	T19	
3	IO_L70N_3	U27	
3	IO_L70P_3	U26	
3	IO_L69N_3/VREF_3	U25	
3	IO_L69P_3	V25	
3	IO_L67N_3	U21	
3	IO_L67P_3	U20	
3	IO_L54N_3	V27	
3	IO_L54P_3	V26	
3	IO_L52N_3	V24	
3	IO_L52P_3	V23	
3	IO_L51N_3/VREF_3	V22	
3	IO_L51P_3	W22	
3	IO_L49N_3	V21	
3	IO_L49P_3	V20	
3	IO_L48N_3	W27	
3	IO_L48P_3	Y27	
3	IO_L46N_3	W26	
3	IO_L46P_3	W25	
3	IO_L45N_3/VREF_3	W24	
3	IO_L45P_3	W23	
3	IO_L43N_3	W21	
3	IO_L43P_3	W20	
3	IO_L28N_3	W19	NC
3	IO_L28P_3	Y19	NC
3	IO_L27N_3/VREF_3	Y25	NC
3	IO_L27P_3	Y24	NC
3	IO_L25N_3	Y23	NC
3	IO_L25P_3	AA23	NC
3	IO_L24N_3	Y22	
3	IO_L24P_3	Y21	
3	IO_L22N_3	AA27	
3	IO_L22P_3	AB27	
3	IO_L21N_3/VREF_3	AA26	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L21P_3	AA25	
3	IO_L19N_3	AB26	
3	IO_L19P_3	AB25	
3	IO_L06N_3	AB24	
3	IO_L06P_3	AB23	
3	IO_L04N_3	AC27	
3	IO_L04P_3	AC26	
3	IO_L03N_3/VREF_3	AC25	
3	IO_L03P_3	AC24	
3	IO_L02N_3/VRP_3	AD27	
3	IO_L02P_3/VRN_3	AE27	
3	IO_L01N_3	AD26	
3	IO_L01P_3	AD25	
4	IO_L01N_4/DOUT	AF25	
4	IO_L01P_4/INIT_B	AG25	
4	IO_L02N_4/D0	AF24	
4	IO_L02P_4/D1	AG24	
4	IO_L03N_4/D2/ALT_VRP_4	AD23	
4	IO_L03P_4/D3/ALT_VRN_4	AE23	
4	IO_L04N_4/VREF_4	AF23	
4	IO_L04P_4	AG23	
4	IO_L05N_4/VRP_4	AD22	
4	IO_L05P_4/VRN_4	AE22	
4	IO_L06N_4	AF22	
4	IO_L06P_4	AG22	
4	IO_L19N_4	AC21	
4	IO_L19P_4	AB21	
4	IO_L21N_4	AE21	
4	IO_L21P_4/VREF_4	AE20	
4	IO_L22N_4	AF21	
4	IO_L22P_4	AG21	
4	IO_L24N_4	AB20	
4	IO_L24P_4	AA20	
4	IO_L25N_4	AC20	NC
4	IO_L25P_4	AD20	NC

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L27N_4	AG20	NC
4	IO_L27P_4/VREF_4	AG19	NC
4	IO_L28N_4	AB19	NC
4	IO_L28P_4	AA19	NC
4	IO_L30N_4	AC19	NC
4	IO_L30P_4	AD19	NC
4	IO_L49N_4	AE19	
4	IO_L49P_4	AF19	
4	IO_L51N_4	AA18	
4	IO_L51P_4/VREF_4	Y18	
4	IO_L52N_4	AB18	
4	IO_L52P_4	AC18	
4	IO_L54N_4	AD18	
4	IO_L54P_4	AE18	
4	IO_L67N_4	AF18	
4	IO_L67P_4	AG18	
4	IO_L69N_4	AA17	
4	IO_L69P_4/VREF_4	Y17	
4	IO_L70N_4	AB17	
4	IO_L70P_4	AB16	
4	IO_L72N_4	AD17	
4	IO_L72P_4	AE17	
4	IO_L73N_4	AF17	
4	IO_L73P_4	AG17	
4	IO_L75N_4	Y16	
4	IO_L75P_4/VREF_4	W16	
4	IO_L76N_4	AC16	
4	IO_L76P_4	AD16	
4	IO_L78N_4	AF16	
4	IO_L78P_4	AG16	
4	IO_L91N_4/VREF_4	W15	
4	IO_L91P_4	Y15	
4	IO_L92N_4	AB15	
4	IO_L92P_4	AA15	
4	IO_L93N_4	AC15	
4	IO_L93P_4	AD15	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L94N_4/VREF_4	AE15	
4	IO_L94P_4	AE14	
4	IO_L95N_4/GCLK3S	AF15	
4	IO_L95P_4/GCLK2P	AG15	
4	IO_L96N_4/GCLK1S	Y14	
4	IO_L96P_4/GCLK0P	AA14	
5	IO_L96N_5/GCLK7S	AC14	
5	IO_L96P_5/GCLK6P	AB14	
5	IO_L95N_5/GCLK5S	AG13	
5	IO_L95P_5/GCLK4P	AF13	
5	IO_L94N_5	AE13	
5	IO_L94P_5/VREF_5	AD13	
5	IO_L93N_5	AC13	
5	IO_L93P_5	AB13	
5	IO_L92N_5	AA13	
5	IO_L92P_5	Y13	
5	IO_L91N_5	W13	
5	IO_L91P_5/VREF_5	W12	
5	IO_L78N_5	AG12	
5	IO_L78P_5	AF12	
5	IO_L76N_5	AD12	
5	IO_L76P_5	AC12	
5	IO_L75N_5/VREF_5	AB12	
5	IO_L75P_5	AB11	
5	IO_L73N_5	Y12	
5	IO_L73P_5	Y11	
5	IO_L72N_5	AG11	
5	IO_L72P_5	AF11	
5	IO_L70N_5	AE11	
5	IO_L70P_5	AD11	
5	IO_L69N_5/VREF_5	AA10	
5	IO_L69P_5	AA11	
5	IO_L67N_5	AG10	
5	IO_L67P_5	AF10	
5	IO_L54N_5	AE10	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L54P_5	AD10	
5	IO_L52N_5	AC10	
5	IO_L52P_5	AB10	
5	IO_L51N_5/VREF_5	Y9	
5	IO_L51P_5	Y10	
5	IO_L49N_5	AG9	
5	IO_L49P_5	AG8	
5	IO_L30N_5	AF9	NC
5	IO_L30P_5	AE9	NC
5	IO_L28N_5	AD9	NC
5	IO_L28P_5	AC9	NC
5	IO_L27N_5/VREF_5	AB9	NC
5	IO_L27P_5	AA9	NC
5	IO_L25N_5	AE8	NC
5	IO_L25P_5	AE7	NC
5	IO_L24N_5	AD8	
5	IO_L24P_5	AC8	
5	IO_L22N_5	AB8	
5	IO_L22P_5	AA8	
5	IO_L21N_5/VREF_5	AG7	
5	IO_L21P_5	AF7	
5	IO_L19N_5	AC7	
5	IO_L19P_5	AB7	
5	IO_L06N_5	AG6	
5	IO_L06P_5	AF6	
5	IO_L05N_5/VRP_5	AE6	
5	IO_L05P_5/VRN_5	AD6	
5	IO_L04N_5	AG5	
5	IO_L04P_5/VREF_5	AF5	
5	IO_L03N_5/D4/ALT_VRP_5	AE5	
5	IO_L03P_5/D5/ALT_VRN_5	AD5	
5	IO_L02N_5/D6	AG4	
5	IO_L02P_5/D7	AF4	
5	IO_L01N_5/RDWR_B	AG3	
5	IO_L01P_5/CS_B	AF3	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L01P_6	AE1	
6	IO_L01N_6	AD1	
6	IO_L02P_6/VRN_6	AD3	
6	IO_L02N_6/VRP_6	AD2	
6	IO_L03P_6	AC4	
6	IO_L03N_6/VREF_6	AC3	
6	IO_L04P_6	AC2	
6	IO_L04N_6	AC1	
6	IO_L06P_6	AB5	
6	IO_L06N_6	AB4	
6	IO_L19P_6	AB3	
6	IO_L19N_6	AB2	
6	IO_L21P_6	AB1	
6	IO_L21N_6/VREF_6	AA1	
6	IO_L22P_6	AA5	
6	IO_L22N_6	AA6	
6	IO_L24P_6	AA3	
6	IO_L24N_6	AA2	
6	IO_L25P_6	Y5	NC
6	IO_L25N_6	Y6	NC
6	IO_L27P_6	Y4	NC
6	IO_L27N_6/VREF_6	Y3	NC
6	IO_L28P_6	Y1	NC
6	IO_L28N_6	W1	NC
6	IO_L43P_6	W8	
6	IO_L43N_6	W9	
6	IO_L45P_6	W6	
6	IO_L45N_6/VREF_6	W7	
6	IO_L46P_6	W5	
6	IO_L46N_6	W4	
6	IO_L48P_6	W3	
6	IO_L48N_6	W2	
6	IO_L49P_6	V7	
6	IO_L49N_6	V8	
6	IO_L51P_6	V5	
6	IO_L51N_6/VREF_6	V6	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L52P_6	V4	
6	IO_L52N_6	V3	
6	IO_L54P_6	V2	
6	IO_L54N_6	V1	
6	IO_L67P_6	U8	
6	IO_L67N_6	T8	
6	IO_L69P_6	U6	
6	IO_L69N_6/VREF_6	U7	
6	IO_L70P_6	U4	
6	IO_L70N_6	U3	
6	IO_L72P_6	U2	
6	IO_L72N_6	U1	
6	IO_L73P_6	T9	
6	IO_L73N_6	R9	
6	IO_L75P_6	T5	
6	IO_L75N_6/VREF_6	T6	
6	IO_L76P_6	T4	
6	IO_L76N_6	R4	
6	IO_L78P_6	T2	
6	IO_L78N_6	T1	
6	IO_L91P_6	R7	
6	IO_L91N_6	R8	
6	IO_L93P_6	R5	
6	IO_L93N_6/VREF_6	R6	
6	IO_L94P_6	R3	
6	IO_L94N_6	P3	
6	IO_L96P_6	R2	
6	IO_L96N_6	R1	
7	IO_L96P_7	P5	
7	IO_L96N_7	P6	
7	IO_L94P_7	P7	
7	IO_L94N_7	P8	
7	IO_L93P_7/VREF_7	N1	
7	IO_L93N_7	N2	
7	IO_L91P_7	N3	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L91N_7	N4	
7	IO_L78P_7	N6	
7	IO_L78N_7	N7	
7	IO_L76P_7	N9	
7	IO_L76N_7	N8	
7	IO_L75P_7/VREF_7	N5	
7	IO_L75N_7	M6	
7	IO_L73P_7	M1	
7	IO_L73N_7	M2	
7	IO_L72P_7	M4	
7	IO_L72N_7	M5	
7	IO_L70P_7	M8	
7	IO_L70N_7	M9	
7	IO_L69P_7/VREF_7	L1	
7	IO_L69N_7	L2	
7	IO_L67P_7	L3	
7	IO_L67N_7	L4	
7	IO_L54P_7	K1	
7	IO_L54N_7	K2	
7	IO_L52P_7	K4	
7	IO_L52N_7	K5	
7	IO_L51P_7/VREF_7	L6	
7	IO_L51N_7	L7	
7	IO_L49P_7	K6	
7	IO_L49N_7	K7	
7	IO_L48P_7	L8	
7	IO_L48N_7	K8	
7	IO_L46P_7	J1	
7	IO_L46N_7	H1	
7	IO_L45P_7/VREF_7	J2	
7	IO_L45N_7	J3	
7	IO_L43P_7	K3	
7	IO_L43N_7	J4	
7	IO_L30P_7	H3	NC
7	IO_L30N_7	H4	NC
7	IO_L28P_7	J5	NC

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L28N_7	J6	NC
7	IO_L27P_7/VREF_7	H5	NC
7	IO_L27N_7	H6	NC
7	IO_L25P_7	J7	NC
7	IO_L25N_7	J8	NC
7	IO_L24P_7	G1	
7	IO_L24N_7	F1	
7	IO_L22P_7	G2	
7	IO_L22N_7	G3	
7	IO_L21P_7/VREF_7	F2	
7	IO_L21N_7	F3	
7	IO_L19P_7	G5	
7	IO_L19N_7	G6	
7	IO_L06P_7	F4	
7	IO_L06N_7	F5	
7	IO_L04P_7	E1	
7	IO_L04N_7	E2	
7	IO_L03P_7/VREF_7	D1	
7	IO_L03N_7	C1	
7	IO_L02P_7/VRN_7	E3	
7	IO_L02N_7/VRP_7	E4	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	K13	
0	VCCO_0	K12	
0	VCCO_0	K11	
0	VCCO_0	J11	
0	VCCO_0	J10	
0	VCCO_0	G12	
0	VCCO_0	D7	
0	VCCO_0	C12	
1	VCCO_1	K17	
1	VCCO_1	K16	
1	VCCO_1	K15	
1	VCCO_1	J18	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	VCCO_1	J17	
1	VCCO_1	G16	
1	VCCO_1	D21	
1	VCCO_1	C16	
2	VCCO_2	N18	
2	VCCO_2	M25	
2	VCCO_2	M21	
2	VCCO_2	M18	
2	VCCO_2	L19	
2	VCCO_2	L18	
2	VCCO_2	K19	
2	VCCO_2	G24	
3	VCCO_3	AA24	
3	VCCO_3	V19	
3	VCCO_3	U19	
3	VCCO_3	U18	
3	VCCO_3	T25	
3	VCCO_3	T21	
3	VCCO_3	T18	
3	VCCO_3	R18	
4	VCCO_4	AE16	
4	VCCO_4	AD21	
4	VCCO_4	AA16	
4	VCCO_4	W18	
4	VCCO_4	W17	
4	VCCO_4	V17	
4	VCCO_4	V16	
4	VCCO_4	V15	
5	VCCO_5	AE12	
5	VCCO_5	AD7	
5	VCCO_5	AA12	
5	VCCO_5	W11	
5	VCCO_5	W10	
5	VCCO_5	V13	
5	VCCO_5	V12	
5	VCCO_5	V11	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	VCCO_6	AA4	
6	VCCO_6	V9	
6	VCCO_6	U10	
6	VCCO_6	U9	
6	VCCO_6	T10	
6	VCCO_6	T7	
6	VCCO_6	T3	
6	VCCO_6	R10	
7	VCCO_7	M10	
7	VCCO_7	M7	
7	VCCO_7	M3	
7	VCCO_7	L10	
7	VCCO_7	L9	
7	VCCO_7	K9	
7	VCCO_7	G4	
7	VCCO_7	N10	
NA	CCLK	AA22	
NA	PROG_B	C4	
NA	DONE	AC22	
NA	M0	AC6	
NA	M1	Y7	
NA	M2	AE4	
NA	HSWAP_EN	D5	
NA	TCK	G20	
NA	TDI	H7	
NA	TDO	G22	
NA	TMS	F21	
NA	PWRDWN_B	AE24	
NA	DXN	G8	
NA	DXP	F7	
NA	VBATT	D23	
NA	RSVD	C24	
NA	VCCAUX	AF14	
NA	VCCAUX	AE26	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCAUX	AE2	
NA	VCCAUX	P26	
NA	VCCAUX	P2	
NA	VCCAUX	C26	
NA	VCCAUX	C2	
NA	VCCAUX	B14	
NA	VCCINT	V18	
NA	VCCINT	V14	
NA	VCCINT	V10	
NA	VCCINT	U17	
NA	VCCINT	U16	
NA	VCCINT	U15	
NA	VCCINT	U14	
NA	VCCINT	U13	
NA	VCCINT	U12	
NA	VCCINT	U11	
NA	VCCINT	T17	
NA	VCCINT	T11	
NA	VCCINT	R17	
NA	VCCINT	R11	
NA	VCCINT	P18	
NA	VCCINT	P17	
NA	VCCINT	P11	
NA	VCCINT	P10	
NA	VCCINT	N17	
NA	VCCINT	N11	
NA	VCCINT	M17	
NA	VCCINT	M11	
NA	VCCINT	L17	
NA	VCCINT	L16	
NA	VCCINT	L15	
NA	VCCINT	L14	
NA	VCCINT	L13	
NA	VCCINT	L12	
NA	VCCINT	L11	
NA	VCCINT	K18	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCINT	K14	
NA	VCCINT	K10	
NA	GND	AG27	
NA	GND	AG26	
NA	GND	AG14	
NA	GND	AG2	
NA	GND	AG1	
NA	GND	AF27	
NA	GND	AF26	
NA	GND	AF20	
NA	GND	AF8	
NA	GND	AF2	
NA	GND	AF1	
NA	GND	AE25	
NA	GND	AE3	
NA	GND	AD24	
NA	GND	AD14	
NA	GND	AD4	
NA	GND	AC23	
NA	GND	AC17	
NA	GND	AC11	
NA	GND	AC5	
NA	GND	AB22	
NA	GND	AB6	
NA	GND	AA21	
NA	GND	AA7	
NA	GND	Y26	
NA	GND	Y20	
NA	GND	Y8	
NA	GND	Y2	
NA	GND	W14	
NA	GND	U23	
NA	GND	U5	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	

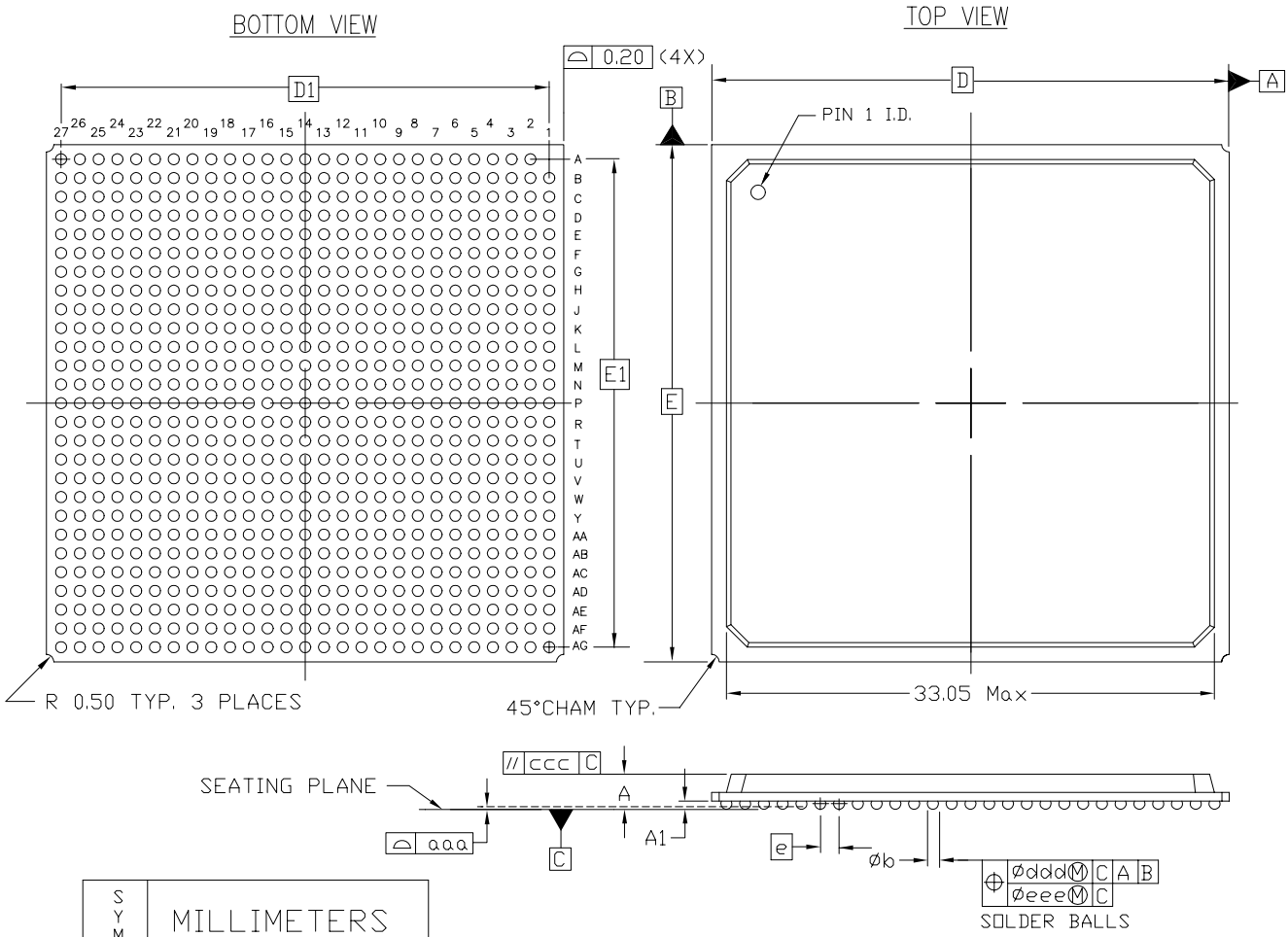
Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T13	
NA	GND	T12	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R13	
NA	GND	R12	
NA	GND	P27	
NA	GND	P24	
NA	GND	P19	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P13	
NA	GND	P12	
NA	GND	P9	
NA	GND	P4	
NA	GND	P1	
NA	GND	N16	
NA	GND	N15	
NA	GND	N14	
NA	GND	N13	
NA	GND	N12	
NA	GND	M16	
NA	GND	M15	
NA	GND	M14	
NA	GND	M13	
NA	GND	M12	
NA	GND	L23	
NA	GND	L5	
NA	GND	J14	
NA	GND	H26	
NA	GND	H20	
NA	GND	H8	
NA	GND	H2	
NA	GND	G21	

Table 10: **BG728 BGA — XC2V2000 and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	G7	
NA	GND	F22	
NA	GND	F6	
NA	GND	E23	
NA	GND	E17	
NA	GND	E11	
NA	GND	E5	
NA	GND	D24	
NA	GND	D14	
NA	GND	D4	
NA	GND	C25	
NA	GND	C3	
NA	GND	B27	
NA	GND	B26	
NA	GND	B20	
NA	GND	B8	
NA	GND	B2	
NA	GND	B1	
NA	GND	A27	
NA	GND	A26	
NA	GND	A14	
NA	GND	A2	

BG728 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	35.00 BSC		
D_1/E_1	33.02 REF		
e	1.27BSC		
øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	27		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–BAR–1
4. NO SOLDER BALL AND LAND ON A1.

Figure 6: **BG728 Standard BGA Package Specifications**

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the **FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L01N_0	B27		
0	IO_L01P_0	A27		
0	IO_L02N_0	F24		
0	IO_L02P_0	E24		
0	IO_L03N_0/VRP_0	C26		
0	IO_L03P_0/VRN_0	C25		
0	IO_L04N_0/VREF_0	A26		
0	IO_L04P_0	A25		
0	IO_L05N_0	F23		
0	IO_L05P_0	F22		
0	IO_L06N_0	C24		
0	IO_L06P_0	D25		
0	IO_L19N_0	A24		
0	IO_L19P_0	B25		
0	IO_L20N_0	G22		
0	IO_L20P_0	G21		
0	IO_L21N_0	D24		
0	IO_L21P_0/VREF_0	D23		
0	IO_L22N_0	B23		
0	IO_L22P_0	B24		
0	IO_L23N_0	H21		
0	IO_L23P_0	H20		
0	IO_L24N_0	E22		
0	IO_L24P_0	E23		
0	IO_L49N_0	A22		
0	IO_L49P_0	B22		
0	IO_L50N_0	F21		
0	IO_L50P_0	F20		
0	IO_L51N_0	C23		
0	IO_L51P_0/VREF_0	C22		
0	IO_L52N_0	B20		
0	IO_L52P_0	B21		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L53N_0	G20		
0	IO_L53P_0	G19		
0	IO_L54N_0	D21		
0	IO_L54P_0	D22		
0	IO_L67N_0	E20	NC	
0	IO_L67P_0	E21	NC	
0	IO_L68N_0	H19	NC	
0	IO_L68P_0	H18	NC	
0	IO_L69N_0	D20	NC	
0	IO_L69P_0/VREF_0	D19	NC	
0	IO_L70N_0	A20	NC	
0	IO_L70P_0	A21	NC	
0	IO_L71N_0	F19	NC	
0	IO_L71P_0	F18	NC	
0	IO_L72N_0	C19	NC	
0	IO_L72P_0	C20	NC	
0	IO_L73N_0	B18	NC	NC
0	IO_L73P_0	B19	NC	NC
0	IO_L74N_0	G18	NC	NC
0	IO_L74P_0	H17	NC	NC
0	IO_L75N_0	E18	NC	NC
0	IO_L75P_0/VREF_0	D18	NC	NC
0	IO_L76N_0	A18	NC	NC
0	IO_L76P_0	A19	NC	NC
0	IO_L77N_0	J17	NC	NC
0	IO_L77P_0	J16	NC	NC
0	IO_L78N_0	E16	NC	NC
0	IO_L78P_0	E17	NC	NC
0	IO_L91N_0/VREF_0	B17		
0	IO_L91P_0	B16		
0	IO_L92N_0	F17		
0	IO_L92P_0	F16		
0	IO_L93N_0	D16		
0	IO_L93P_0	D17		
0	IO_L94N_0/VREF_0	A17		
0	IO_L94P_0	A16		
0	IO_L95N_0/GCLK7P	H16		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L95P_0/GCLK6S	G16		
0	IO_L96N_0/GCLK5P	C17		
0	IO_L96P_0/GCLK4S	C16		
1	IO_L96N_1/GCLK3P	C15		
1	IO_L96P_1/GCLK2S	C14		
1	IO_L95N_1/GCLK1P	F15		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	B15		
1	IO_L94P_1/VREF_1	B14		
1	IO_L93N_1	D14		
1	IO_L93P_1	D15		
1	IO_L92N_1	G15		
1	IO_L92P_1	H15		
1	IO_L91N_1	A14		
1	IO_L91P_1/VREF_1	A13		
1	IO_L78N_1	E14	NC	NC
1	IO_L78P_1	E15	NC	NC
1	IO_L77N_1	J15	NC	NC
1	IO_L77P_1	J14	NC	NC
1	IO_L76N_1	B12	NC	NC
1	IO_L76P_1	B13	NC	NC
1	IO_L75N_1/VREF_1	D13	NC	NC
1	IO_L75P_1	E13	NC	NC
1	IO_L74N_1	H14	NC	NC
1	IO_L74P_1	H13	NC	NC
1	IO_L73N_1	A11	NC	NC
1	IO_L73P_1	A12	NC	NC
1	IO_L72N_1	C11	NC	
1	IO_L72P_1	C12	NC	
1	IO_L71N_1	F13	NC	
1	IO_L71P_1	F12	NC	
1	IO_L70N_1	B10	NC	
1	IO_L70P_1	B11	NC	
1	IO_L69N_1/VREF_1	D12	NC	
1	IO_L69P_1	D11	NC	
1	IO_L68N_1	G13	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L68P_1	G12	NC	
1	IO_L67N_1	A9	NC	
1	IO_L67P_1	A10	NC	
1	IO_L54N_1	E10		
1	IO_L54P_1	E11		
1	IO_L53N_1	H12		
1	IO_L53P_1	H11		
1	IO_L52N_1	D9		
1	IO_L52P_1	D10		
1	IO_L51N_1/VREF_1	C9		
1	IO_L51P_1	C8		
1	IO_L50N_1	F11		
1	IO_L50P_1	F10		
1	IO_L49N_1	B8		
1	IO_L49P_1	B9		
1	IO_L24N_1	E8		
1	IO_L24P_1	E9		
1	IO_L23N_1	G11		
1	IO_L23P_1	H10		
1	IO_L22N_1	B7		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	D8		
1	IO_L21P_1	E7		
1	IO_L20N_1	G10		
1	IO_L20P_1	G9		
1	IO_L19N_1	A5		
1	IO_L19P_1	A6		
1	IO_L06N_1	C6		
1	IO_L06P_1	C7		
1	IO_L05N_1	F9		
1	IO_L05P_1	G8		
1	IO_L04N_1	B6		
1	IO_L04P_1/VREF_1	C5		
1	IO_L03N_1/VRP_1	D7		
1	IO_L03P_1/VRN_1	D6		
1	IO_L02N_1	F8		
1	IO_L02P_1	F7		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L01N_1	B4		
1	IO_L01P_1	A4		
2	IO_L01N_2	C1		
2	IO_L01P_2	B1		
2	IO_L02N_2/VRP_2	H9		
2	IO_L02P_2/VRN_2	H8		
2	IO_L03N_2	D3		
2	IO_L03P_2/VREF_2	E3		
2	IO_L04N_2	D2		
2	IO_L04P_2	C2		
2	IO_L05N_2	G7		
2	IO_L05P_2	H7		
2	IO_L06N_2	F4		
2	IO_L06P_2	E4		
2	IO_L19N_2	E1		
2	IO_L19P_2	D1		
2	IO_L20N_2	G6		
2	IO_L20P_2	H6		
2	IO_L21N_2	F5		
2	IO_L21P_2/VREF_2	G5		
2	IO_L22N_2	G2		
2	IO_L22P_2	F2		
2	IO_L23N_2	J8		
2	IO_L23P_2	J7		
2	IO_L24N_2	G3		
2	IO_L24P_2	F3		
2	IO_L43N_2	G1		
2	IO_L43P_2	F1		
2	IO_L44N_2	K8		
2	IO_L44P_2	L8		
2	IO_L45N_2	G4		
2	IO_L45P_2/VREF_2	H4		
2	IO_L46N_2	J2		
2	IO_L46P_2	H2		
2	IO_L47N_2	J6		
2	IO_L47P_2	K6		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L48N_2	J5		
2	IO_L48P_2	H5		
2	IO_L49N_2	J3		
2	IO_L49P_2	H3		
2	IO_L50N_2	K7		
2	IO_L50P_2	L7		
2	IO_L51N_2	J4		
2	IO_L51P_2/VREF_2	K4		
2	IO_L52N_2	K1		
2	IO_L52P_2	J1		
2	IO_L53N_2	L6		
2	IO_L53P_2	M6		
2	IO_L54N_2	L5		
2	IO_L54P_2	K5		
2	IO_L67N_2	L2	NC	
2	IO_L67P_2	K2	NC	
2	IO_L68N_2	M8	NC	
2	IO_L68P_2	N8	NC	
2	IO_L69N_2	L4	NC	
2	IO_L69P_2/VREF_2	M4	NC	
2	IO_L70N_2	M1	NC	
2	IO_L70P_2	L1	NC	
2	IO_L71N_2	M7	NC	
2	IO_L71P_2	N7	NC	
2	IO_L72N_2	M3	NC	
2	IO_L72P_2	L3	NC	
2	IO_L73N_2	N2	NC	NC
2	IO_L73P_2	M2	NC	NC
2	IO_L74N_2	N6	NC	NC
2	IO_L74P_2	P6	NC	NC
2	IO_L75N_2	N5	NC	NC
2	IO_L75P_2/VREF_2	N4	NC	NC
2	IO_L76N_2	P1	NC	NC
2	IO_L76P_2	N1	NC	NC
2	IO_L77N_2	P9	NC	NC
2	IO_L77P_2	R9	NC	NC
2	IO_L78N_2	R5	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L78P_2	P5	NC	NC
2	IO_L91N_2	R2		
2	IO_L91P_2	P2		
2	IO_L92N_2	P8		
2	IO_L92P_2	R8		
2	IO_L93N_2	P4		
2	IO_L93P_2/VREF_2	R4		
2	IO_L94N_2	R1		
2	IO_L94P_2	T2		
2	IO_L95N_2	R7		
2	IO_L95P_2	R6		
2	IO_L96N_2	R3		
2	IO_L96P_2	P3		
3	IO_L96N_3	T7		
3	IO_L96P_3	T6		
3	IO_L95N_3	U1		
3	IO_L95P_3	V1		
3	IO_L94N_3	T3		
3	IO_L94P_3	U3		
3	IO_L93N_3/VREF_3	T8		
3	IO_L93P_3	U8		
3	IO_L92N_3	U2		
3	IO_L92P_3	V2		
3	IO_L91N_3	T4		
3	IO_L91P_3	U4		
3	IO_L78N_3	U9	NC	NC
3	IO_L78P_3	T9	NC	NC
3	IO_L77N_3	W1	NC	NC
3	IO_L77P_3	Y1	NC	NC
3	IO_L76N_3	T5	NC	NC
3	IO_L76P_3	U5	NC	NC
3	IO_L75N_3/VREF_3	U6	NC	NC
3	IO_L75P_3	V6	NC	NC
3	IO_L74N_3	W2	NC	NC
3	IO_L74P_3	Y2	NC	NC
3	IO_L73N_3	V4	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L73P_3	W4	NC	NC
3	IO_L72N_3	W7	NC	
3	IO_L72P_3	V7	NC	
3	IO_L71N_3	V5	NC	
3	IO_L71P_3	W6	NC	
3	IO_L70N_3	W3	NC	
3	IO_L70P_3	Y3	NC	
3	IO_L69N_3/VREF_3	V8	NC	
3	IO_L69P_3	W8	NC	
3	IO_L68N_3	AA1	NC	
3	IO_L68P_3	AB1	NC	
3	IO_L67N_3	Y4	NC	
3	IO_L67P_3	AA4	NC	
3	IO_L54N_3	AA6		
3	IO_L54P_3	Y6		
3	IO_L53N_3	AA2		
3	IO_L53P_3	AB2		
3	IO_L52N_3	Y5		
3	IO_L52P_3	AA5		
3	IO_L51N_3/VREF_3	Y8		
3	IO_L51P_3	AA8		
3	IO_L50N_3	AC2		
3	IO_L50P_3	AD2		
3	IO_L49N_3	Y7		
3	IO_L49P_3	AA7		
3	IO_L48N_3	AC6		
3	IO_L48P_3	AB6		
3	IO_L47N_3	AD1		
3	IO_L47P_3	AE1		
3	IO_L46N_3	AB3		
3	IO_L46P_3	AC3		
3	IO_L45N_3/VREF_3	AB7		
3	IO_L45P_3	AC7		
3	IO_L44N_3	AB4		
3	IO_L44P_3	AC4		
3	IO_L43N_3	AB5		
3	IO_L43P_3	AC5		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
3	IO_L24N_3	AC8		
3	IO_L24P_3	AB8		
3	IO_L23N_3	AE2		
3	IO_L23P_3	AF3		
3	IO_L22N_3	AD3		
3	IO_L22P_3	AE3		
3	IO_L21N_3/VREF_3	AD6		
3	IO_L21P_3	AD7		
3	IO_L20N_3	AF1		
3	IO_L20P_3	AG1		
3	IO_L19N_3	AD4		
3	IO_L19P_3	AE4		
3	IO_L06N_3	AD8		
3	IO_L06P_3	AE7		
3	IO_L05N_3	AG2		
3	IO_L05P_3	AH2		
3	IO_L04N_3	AD5		
3	IO_L04P_3	AE5		
3	IO_L03N_3/VREF_3	AC9		
3	IO_L03P_3	AD9		
3	IO_L02N_3/VRP_3	AH1		
3	IO_L02P_3/VRN_3	AJ1		
3	IO_L01N_3	AF4		
3	IO_L01P_3	AG3		
4	IO_L01N_4/DOUT	AK2		
4	IO_L01P_4/INIT_B	AJ3		
4	IO_L02N_4/D0	AE8		
4	IO_L02P_4/D1	AF9		
4	IO_L03N_4/D2/ALT_VRP_4	AH5		
4	IO_L03P_4/D3/ALT_VRN_4	AH6		
4	IO_L04N_4/VREF_4	AJ4		
4	IO_L04P_4	AK4		
4	IO_L05N_4/VRP_4	AC10		
4	IO_L05P_4/VRN_4	AC11		
4	IO_L06N_4	AH7		
4	IO_L06P_4	AG6		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L19N_4	AK6		
4	IO_L19P_4	AK5		
4	IO_L20N_4	AE9		
4	IO_L20P_4	AE10		
4	IO_L21N_4	AF7		
4	IO_L21P_4/VREF_4	AF8		
4	IO_L22N_4	AK7		
4	IO_L22P_4	AJ6		
4	IO_L23N_4	AD10		
4	IO_L23P_4	AD11		
4	IO_L24N_4	AG8		
4	IO_L24P_4	AG7		
4	IO_L49N_4	AJ8		
4	IO_L49P_4	AJ7		
4	IO_L50N_4	AE11		
4	IO_L50P_4	AE12		
4	IO_L51N_4	AG9		
4	IO_L51P_4/VREF_4	AG10		
4	IO_L52N_4	AK9		
4	IO_L52P_4	AJ9		
4	IO_L53N_4	AH8		
4	IO_L53P_4	AH9		
4	IO_L54N_4	AF11		
4	IO_L54P_4	AF10		
4	IO_L67N_4	AJ11	NC	
4	IO_L67P_4	AJ10	NC	
4	IO_L68N_4	AC12	NC	
4	IO_L68P_4	AC13	NC	
4	IO_L69N_4	AG11	NC	
4	IO_L69P_4/VREF_4	AG12	NC	
4	IO_L70N_4	AK11	NC	
4	IO_L70P_4	AK10	NC	
4	IO_L71N_4	AD12	NC	
4	IO_L71P_4	AD13	NC	
4	IO_L72N_4	AH12	NC	
4	IO_L72P_4	AH11	NC	
4	IO_L73N_4	AJ13	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L73P_4	AJ12	NC	NC
4	IO_L74N_4	AE13	NC	NC
4	IO_L74P_4	AE14	NC	NC
4	IO_L75N_4	AF13	NC	NC
4	IO_L75P_4/VREF_4	AG13	NC	NC
4	IO_L76N_4	AK13	NC	NC
4	IO_L76P_4	AK12	NC	NC
4	IO_L77N_4	AB14	NC	NC
4	IO_L77P_4	AB15	NC	NC
4	IO_L78N_4	AF15	NC	NC
4	IO_L78P_4	AF14	NC	NC
4	IO_L91N_4/VREF_4	AJ14		
4	IO_L91P_4	AJ15		
4	IO_L92N_4	AC14		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AG15		
4	IO_L93P_4	AG14		
4	IO_L94N_4/VREF_4	AK14		
4	IO_L94P_4	AK15		
4	IO_L95N_4/GCLK3S	AD15		
4	IO_L95P_4/GCLK2P	AE15		
4	IO_L96N_4/GCLK1S	AH14		
4	IO_L96P_4/GCLK0P	AH15		
5	IO_L96N_5/GCLK7S	AH16		
5	IO_L96P_5/GCLK6P	AH17		
5	IO_L95N_5/GCLK5S	AE16		
5	IO_L95P_5/GCLK4P	AD16		
5	IO_L94N_5	AJ16		
5	IO_L94P_5/VREF_5	AJ17		
5	IO_L93N_5	AG17		
5	IO_L93P_5	AG16		
5	IO_L92N_5	AC16		
5	IO_L92P_5	AC17		
5	IO_L91N_5	AK17		
5	IO_L91P_5/VREF_5	AK18		
5	IO_L78N_5	AF17	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L78P_5	AF16	NC	NC
5	IO_L77N_5	AB16	NC	NC
5	IO_L77P_5	AB17	NC	NC
5	IO_L76N_5	AJ19	NC	NC
5	IO_L76P_5	AJ18	NC	NC
5	IO_L75N_5/VREF_5	AG18	NC	NC
5	IO_L75P_5	AF18	NC	NC
5	IO_L74N_5	AE17	NC	NC
5	IO_L74P_5	AE18	NC	NC
5	IO_L73N_5	AK20	NC	NC
5	IO_L73P_5	AK19	NC	NC
5	IO_L72N_5	AH20	NC	
5	IO_L72P_5	AH19	NC	
5	IO_L71N_5	AD18	NC	
5	IO_L71P_5	AD19	NC	
5	IO_L70N_5	AJ21	NC	
5	IO_L70P_5	AJ20	NC	
5	IO_L69N_5/VREF_5	AG19	NC	
5	IO_L69P_5	AG20	NC	
5	IO_L68N_5	AC18	NC	
5	IO_L68P_5	AC19	NC	
5	IO_L67N_5	AK22	NC	
5	IO_L67P_5	AK21	NC	
5	IO_L54N_5	AF21		
5	IO_L54P_5	AF20		
5	IO_L53N_5	AH22		
5	IO_L53P_5	AH23		
5	IO_L52N_5	AG22		
5	IO_L52P_5	AG21		
5	IO_L51N_5/VREF_5	AF22		
5	IO_L51P_5	AF23		
5	IO_L50N_5	AE19		
5	IO_L50P_5	AE20		
5	IO_L49N_5	AJ23		
5	IO_L49P_5	AJ22		
5	IO_L24N_5	AF24		
5	IO_L24P_5	AG23		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L20P_6	AE26		
6	IO_L20N_6	AD26		
6	IO_L21P_6	AG30		
6	IO_L21N_6/VREF_6	AF30		
6	IO_L22P_6	AD25		
6	IO_L22N_6	AC25		
6	IO_L23P_6	AE28		
6	IO_L23N_6	AD28		
6	IO_L24P_6	AD29		
6	IO_L24N_6	AE29		
6	IO_L43P_6	AC24		
6	IO_L43N_6	AB24		
6	IO_L44P_6	AD27		
6	IO_L44N_6	AC27		
6	IO_L45P_6	AC26		
6	IO_L45N_6/VREF_6	AB26		
6	IO_L46P_6	AA23		
6	IO_L46N_6	Y23		
6	IO_L47P_6	AC28		
6	IO_L47N_6	AB28		
6	IO_L48P_6	AD30		
6	IO_L48N_6	AE30		
6	IO_L49P_6	AB25		
6	IO_L49N_6	AA25		
6	IO_L50P_6	AA24		
6	IO_L50N_6	Y24		
6	IO_L51P_6	AC29		
6	IO_L51N_6/VREF_6	AB30		
6	IO_L52P_6	Y25		
6	IO_L52N_6	W25		
6	IO_L53P_6	AB27		
6	IO_L53N_6	AA27		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AB29		
6	IO_L67P_6	W23	NC	
6	IO_L67N_6	V23	NC	
6	IO_L68P_6	AA26	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L68N_6	Y26	NC	
6	IO_L69P_6	AA30	NC	
6	IO_L69N_6/VREF_6	Y30	NC	
6	IO_L70P_6	W24	NC	
6	IO_L70N_6	V24	NC	
6	IO_L71P_6	Y27	NC	
6	IO_L71N_6	W27	NC	
6	IO_L72P_6	W28	NC	
6	IO_L72N_6	Y28	NC	
6	IO_L73P_6	V25	NC	NC
6	IO_L73N_6	U25	NC	NC
6	IO_L74P_6	V26	NC	NC
6	IO_L74N_6	V27	NC	NC
6	IO_L75P_6	Y29	NC	NC
6	IO_L75N_6/VREF_6	W29	NC	NC
6	IO_L76P_6	U22	NC	NC
6	IO_L76N_6	T22	NC	NC
6	IO_L77P_6	U26	NC	NC
6	IO_L77N_6	T26	NC	NC
6	IO_L78P_6	V30	NC	NC
6	IO_L78N_6	W30	NC	NC
6	IO_L91P_6	U23		
6	IO_L91N_6	T23		
6	IO_L92P_6	U27		
6	IO_L92N_6	T27		
6	IO_L93P_6	V29		
6	IO_L93N_6/VREF_6	U29		
6	IO_L94P_6	T24		
6	IO_L94N_6	T25		
6	IO_L95P_6	U28		
6	IO_L95N_6	T28		
6	IO_L96P_6	T30		
6	IO_L96N_6	U30		
7	IO_L96P_7	P28		
7	IO_L96N_7	R28		
7	IO_L95P_7	R25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L95N_7	R24		
7	IO_L94P_7	R29		
7	IO_L94N_7	T29		
7	IO_L93P_7/VREF_7	R27		
7	IO_L93N_7	P27		
7	IO_L92P_7	R23		
7	IO_L92N_7	P23		
7	IO_L91P_7	N30		
7	IO_L91N_7	P30		
7	IO_L78P_7	P26	NC	NC
7	IO_L78N_7	R26	NC	NC
7	IO_L77P_7	R22	NC	NC
7	IO_L77N_7	P22	NC	NC
7	IO_L76P_7	N29	NC	NC
7	IO_L76N_7	P29	NC	NC
7	IO_L75P_7/VREF_7	N27	NC	NC
7	IO_L75N_7	N26	NC	NC
7	IO_L74P_7	P25	NC	NC
7	IO_L74N_7	N25	NC	NC
7	IO_L73P_7	L30	NC	NC
7	IO_L73N_7	M30	NC	NC
7	IO_L72P_7	L28	NC	
7	IO_L72N_7	M28	NC	
7	IO_L71P_7	N24	NC	
7	IO_L71N_7	M24	NC	
7	IO_L70P_7	L29	NC	
7	IO_L70N_7	M29	NC	
7	IO_L69P_7/VREF_7	M27	NC	
7	IO_L69N_7	L27	NC	
7	IO_L68P_7	N23	NC	
7	IO_L68N_7	M23	NC	
7	IO_L67P_7	J30	NC	
7	IO_L67N_7	K30	NC	
7	IO_L54P_7	K26		
7	IO_L54N_7	L26		
7	IO_L53P_7	M25		
7	IO_L53N_7	L25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L52P_7	J29		
7	IO_L52N_7	K29		
7	IO_L51P_7/VREF_7	K27		
7	IO_L51N_7	J27		
7	IO_L50P_7	L24		
7	IO_L50N_7	K24		
7	IO_L49P_7	H27		
7	IO_L49N_7	J28		
7	IO_L48P_7	H26		
7	IO_L48N_7	J26		
7	IO_L47P_7	K25		
7	IO_L47N_7	J25		
7	IO_L46P_7	H28		
7	IO_L46N_7	H29		
7	IO_L45P_7/VREF_7	G28		
7	IO_L45N_7	F28		
7	IO_L44P_7	L23		
7	IO_L44N_7	K23		
7	IO_L43P_7	F30		
7	IO_L43N_7	G30		
7	IO_L24P_7	F26		
7	IO_L24N_7	G27		
7	IO_L23P_7	J24		
7	IO_L23N_7	H24		
7	IO_L22P_7	F29		
7	IO_L22N_7	G29		
7	IO_L21P_7/VREF_7	G26		
7	IO_L21N_7	G25		
7	IO_L20P_7	H25		
7	IO_L20N_7	G24		
7	IO_L19P_7	D30		
7	IO_L19N_7	E30		
7	IO_L06P_7	E27		
7	IO_L06N_7	F27		
7	IO_L05P_7	J23		
7	IO_L05N_7	H22		
7	IO_L04P_7	C29		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	VCCO_6	AF29		
6	VCCO_6	AA22		
6	VCCO_6	Y22		
6	VCCO_6	Y21		
6	VCCO_6	W22		
6	VCCO_6	W21		
6	VCCO_6	V28		
6	VCCO_6	V22		
6	VCCO_6	V21		
6	VCCO_6	U21		
6	VCCO_6	T21		
7	VCCO_7	R21		
7	VCCO_7	P21		
7	VCCO_7	N28		
7	VCCO_7	N22		
7	VCCO_7	N21		
7	VCCO_7	M22		
7	VCCO_7	M21		
7	VCCO_7	L22		
7	VCCO_7	L21		
7	VCCO_7	K22		
7	VCCO_7	E29		
NA	CCLK	AF6		
NA	PROG_B	B28		
NA	DONE	AG5		
NA	M0	AF25		
NA	M1	AG26		
NA	M2	AH27		
NA	HSWAP_EN	C27		
NA	TCK	D5		
NA	TDI	A29		
NA	TDO	B3		
NA	TMS	C4		
NA	PWRDWN_B	AH4		
NA	DXN	D26		
NA	DXP	E25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	VBATT	A2		
NA	RSVD	E6		
NA	VCCAUX	AK28		
NA	VCCAUX	AK16		
NA	VCCAUX	AK3		
NA	VCCAUX	T1		
NA	VCCAUX	R30		
NA	VCCAUX	A28		
NA	VCCAUX	A15		
NA	VCCAUX	A3		
NA	VCCINT	AB22		
NA	VCCINT	AB9		
NA	VCCINT	AA21		
NA	VCCINT	AA10		
NA	VCCINT	Y20		
NA	VCCINT	Y19		
NA	VCCINT	Y18		
NA	VCCINT	Y17		
NA	VCCINT	Y16		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	Y12		
NA	VCCINT	Y11		
NA	VCCINT	W20		
NA	VCCINT	W11		
NA	VCCINT	V20		
NA	VCCINT	V11		
NA	VCCINT	U20		
NA	VCCINT	U11		
NA	VCCINT	T20		
NA	VCCINT	T11		
NA	VCCINT	R20		
NA	VCCINT	R11		
NA	VCCINT	P20		
NA	VCCINT	P11		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	VCCINT	N20		
NA	VCCINT	N11		
NA	VCCINT	M20		
NA	VCCINT	M11		
NA	VCCINT	L20		
NA	VCCINT	L19		
NA	VCCINT	L18		
NA	VCCINT	L17		
NA	VCCINT	L16		
NA	VCCINT	L15		
NA	VCCINT	L14		
NA	VCCINT	L13		
NA	VCCINT	L12		
NA	VCCINT	L11		
NA	VCCINT	K21		
NA	VCCINT	K10		
NA	VCCINT	J22		
NA	VCCINT	J9		
NA	GND	AK23		
NA	GND	AK8		
NA	GND	AJ29		
NA	GND	AJ2		
NA	GND	AH28		
NA	GND	AH21		
NA	GND	AH10		
NA	GND	AH3		
NA	GND	AG27		
NA	GND	AG4		
NA	GND	AF26		
NA	GND	AF19		
NA	GND	AF12		
NA	GND	AF5		
NA	GND	AE25		
NA	GND	AE6		
NA	GND	AD17		
NA	GND	AD14		
NA	GND	AC30		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

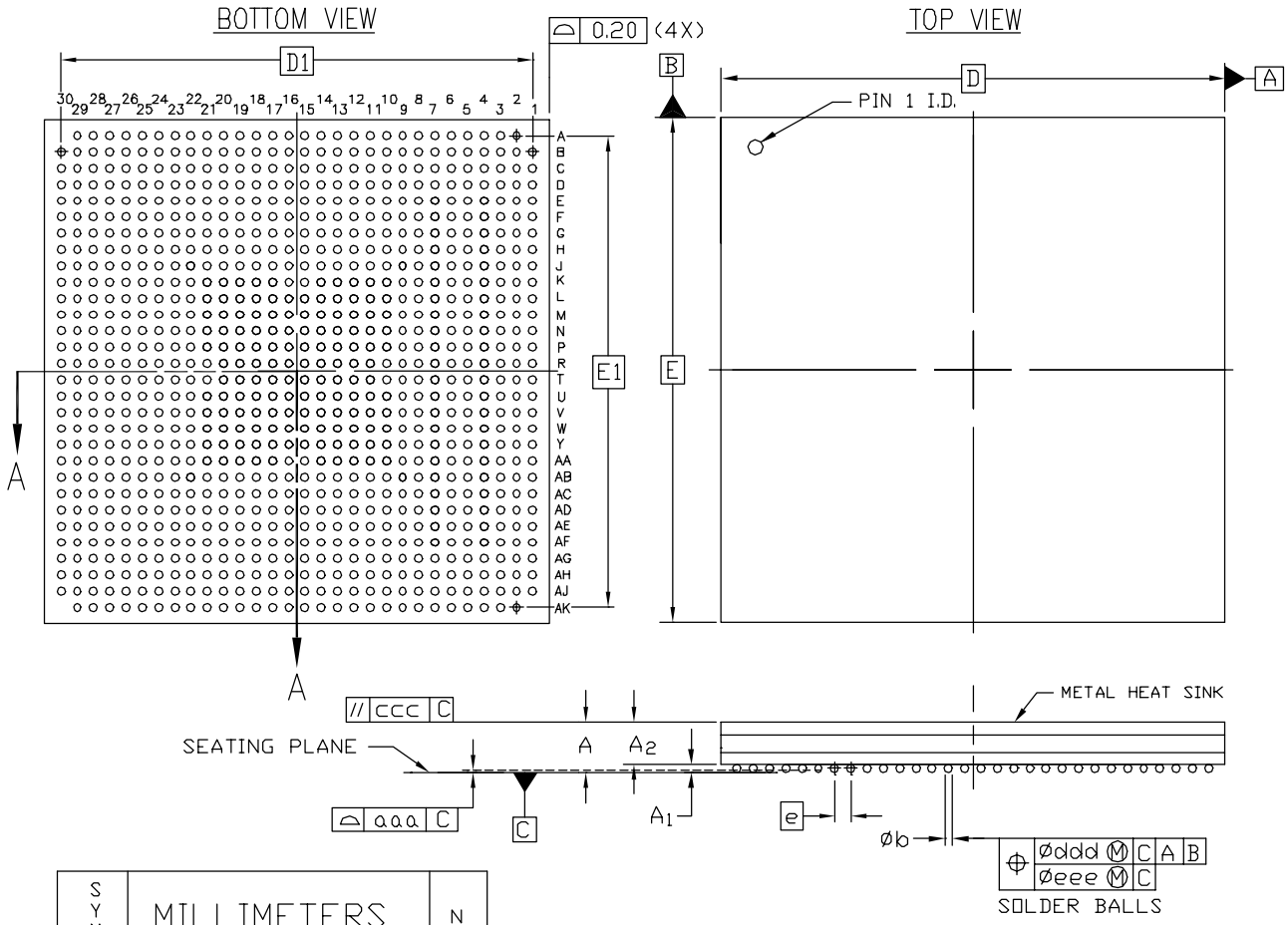
Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	T13		
NA	GND	T12		
NA	GND	R19		
NA	GND	R18		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		
NA	GND	R12		
NA	GND	P24		
NA	GND	P19		
NA	GND	P18		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P7		
NA	GND	N19		
NA	GND	N18		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	M26		
NA	GND	M19		
NA	GND	M18		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		

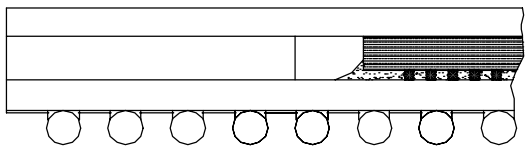
Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	M5		
NA	GND	K28		
NA	GND	K3		
NA	GND	H30		
NA	GND	H1		
NA	GND	G17		
NA	GND	G14		
NA	GND	F25		
NA	GND	F6		
NA	GND	E26		
NA	GND	E19		
NA	GND	E12		
NA	GND	E5		
NA	GND	D27		
NA	GND	D4		
NA	GND	C28		
NA	GND	C21		
NA	GND	C10		
NA	GND	C3		
NA	GND	B29		
NA	GND	B2		
NA	GND	A23		
NA	GND	A8		

FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	30			2



SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAN–1 (DEPOPULATED)

Figure 7: **FF896 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 12, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000 Virtex-II devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V3000 device shown in the No Connect column. Following this table are the **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L01N_0	D29	
0	IO_L01P_0	C29	
0	IO_L02N_0	H26	
0	IO_L02P_0	G26	
0	IO_L03N_0/VRP_0	E28	
0	IO_L03P_0/VRN_0	E27	
0	IO_L04N_0/VREF_0	F25	
0	IO_L04P_0	F26	
0	IO_L05N_0	H25	
0	IO_L05P_0	H24	
0	IO_L06N_0	E26	
0	IO_L06P_0	F27	
0	IO_L19N_0	B32	
0	IO_L19P_0	C33	
0	IO_L20N_0	J24	
0	IO_L20P_0	J23	
0	IO_L21N_0	C27	
0	IO_L21P_0/VREF_0	C28	
0	IO_L22N_0	B30	
0	IO_L22P_0	B31	
0	IO_L23N_0	K23	
0	IO_L23P_0	K22	
0	IO_L24N_0	C26	
0	IO_L24P_0	D27	
0	IO_L25N_0	A30	
0	IO_L25P_0	A31	
0	IO_L26N_0	G24	
0	IO_L26P_0	G25	
0	IO_L27N_0	E25	
0	IO_L27P_0/VREF_0	E24	
0	IO_L28N_0	D25	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L28P_0	D26	
0	IO_L29N_0	H23	
0	IO_L29P_0	H22	
0	IO_L30N_0	F23	
0	IO_L30P_0	F24	
0	IO_L49N_0	B28	
0	IO_L49P_0	B29	
0	IO_L50N_0	J22	
0	IO_L50P_0	J21	
0	IO_L51N_0	A28	
0	IO_L51P_0/VREF_0	A29	
0	IO_L52N_0	A26	
0	IO_L52P_0	B27	
0	IO_L53N_0	C24	
0	IO_L53P_0	D24	
0	IO_L54N_0	D22	
0	IO_L54P_0	D23	
0	IO_L60N_0	B25	NC
0	IO_L60P_0	B26	NC
0	IO_L67N_0	B23	
0	IO_L67P_0	B24	
0	IO_L68N_0	G22	
0	IO_L68P_0	G23	
0	IO_L69N_0	F22	
0	IO_L69P_0/VREF_0	F21	
0	IO_L70N_0	A23	
0	IO_L70P_0	A24	
0	IO_L71N_0	K21	
0	IO_L71P_0	K20	
0	IO_L72N_0	C22	
0	IO_L72P_0	C23	
0	IO_L73N_0	E21	
0	IO_L73P_0	E22	
0	IO_L74N_0	H21	
0	IO_L74P_0	H20	
0	IO_L75N_0	G20	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L75P_0/VREF_0	F20	
0	IO_L76N_0	B21	
0	IO_L76P_0	B22	
0	IO_L77N_0	J20	
0	IO_L77P_0	K19	
0	IO_L78N_0	D20	
0	IO_L78P_0	D21	
0	IO_L79N_0	A21	NC
0	IO_L79P_0	A22	NC
0	IO_L80N_0	L19	NC
0	IO_L80P_0	L18	NC
0	IO_L81N_0	B19	NC
0	IO_L81P_0/VREF_0	A20	NC
0	IO_L82N_0	A18	NC
0	IO_L82P_0	B18	NC
0	IO_L83N_0	H19	NC
0	IO_L83P_0	H18	NC
0	IO_L84N_0	C20	NC
0	IO_L84P_0	C21	NC
0	IO_L91N_0/VREF_0	D19	
0	IO_L91P_0	D18	
0	IO_L92N_0	G18	
0	IO_L92P_0	G19	
0	IO_L93N_0	F18	
0	IO_L93P_0	F19	
0	IO_L94N_0/VREF_0	C19	
0	IO_L94P_0	C18	
0	IO_L95N_0/GCLK7P	K18	
0	IO_L95P_0/GCLK6S	J18	
0	IO_L96N_0/GCLK5P	E19	
0	IO_L96P_0/GCLK4S	E18	
1	IO_L96N_1/GCLK3P	E17	
1	IO_L96P_1/GCLK2S	E16	
1	IO_L95N_1/GCLK1P	H17	
1	IO_L95P_1/GCLK0S	H16	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L94N_1	D17	
1	IO_L94P_1/VREF_1	D16	
1	IO_L93N_1	F16	
1	IO_L93P_1	F17	
1	IO_L92N_1	G16	
1	IO_L92P_1	G17	
1	IO_L91N_1	C16	
1	IO_L91P_1/VREF_1	C15	
1	IO_L84N_1	D14	NC
1	IO_L84P_1	D15	NC
1	IO_L83N_1	J17	NC
1	IO_L83P_1	K17	NC
1	IO_L82N_1	B17	NC
1	IO_L82P_1	A17	NC
1	IO_L81N_1/VREF_1	A15	NC
1	IO_L81P_1	B16	NC
1	IO_L80N_1	L17	NC
1	IO_L80P_1	L16	NC
1	IO_L79N_1	A13	NC
1	IO_L79P_1	A14	NC
1	IO_L78N_1	C13	
1	IO_L78P_1	C14	
1	IO_L77N_1	K16	
1	IO_L77P_1	K15	
1	IO_L76N_1	B13	
1	IO_L76P_1	B14	
1	IO_L75N_1/VREF_1	F15	
1	IO_L75P_1	G15	
1	IO_L74N_1	H15	
1	IO_L74P_1	H14	
1	IO_L73N_1	A11	
1	IO_L73P_1	A12	
1	IO_L72N_1	E13	
1	IO_L72P_1	E14	
1	IO_L71N_1	J15	
1	IO_L71P_1	J14	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L70N_1	D12	
1	IO_L70P_1	D13	
1	IO_L69N_1/VREF_1	F14	
1	IO_L69P_1	F13	
1	IO_L68N_1	C11	
1	IO_L68P_1	C12	
1	IO_L67N_1	B11	
1	IO_L67P_1	B12	
1	IO_L60N_1	F11	NC
1	IO_L60P_1	F12	NC
1	IO_L54N_1	D10	
1	IO_L54P_1	D11	
1	IO_L53N_1	G12	
1	IO_L53P_1	G13	
1	IO_L52N_1	B9	
1	IO_L52P_1	B10	
1	IO_L51N_1/VREF_1	B8	
1	IO_L51P_1	A9	
1	IO_L50N_1	K14	
1	IO_L50P_1	K13	
1	IO_L49N_1	A6	
1	IO_L49P_1	A7	
1	IO_L30N_1	D9	
1	IO_L30P_1	C9	
1	IO_L29N_1	H13	
1	IO_L29P_1	H12	
1	IO_L28N_1	C7	
1	IO_L28P_1	C8	
1	IO_L27N_1/VREF_1	E11	
1	IO_L27P_1	E10	
1	IO_L26N_1	J13	
1	IO_L26P_1	K12	
1	IO_L25N_1	B6	
1	IO_L25P_1	B7	
1	IO_L24N_1	E8	
1	IO_L24P_1	E9	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L23N_1	G10	
1	IO_L23P_1	G11	
1	IO_L22N_1	A4	
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	
2	IO_L21N_2	H7	
2	IO_L21P_2/VREF_2	J7	
2	IO_L22N_2	H6	
2	IO_L22P_2	G6	
2	IO_L23N_2	L10	
2	IO_L23P_2	L9	
2	IO_L24N_2	G3	
2	IO_L24P_2	F3	
2	IO_L25N_2	G2	
2	IO_L25P_2	F2	
2	IO_L26N_2	M10	
2	IO_L26P_2	N10	
2	IO_L27N_2	J6	
2	IO_L27P_2/VREF_2	K6	
2	IO_L28N_2	J5	
2	IO_L28P_2	H5	
2	IO_L29N_2	L7	
2	IO_L29P_2	K7	
2	IO_L30N_2	J4	
2	IO_L30P_2	H4	
2	IO_L43N_2	G1	
2	IO_L43P_2	F1	
2	IO_L44N_2	L8	
2	IO_L44P_2	M8	
2	IO_L45N_2	J1	
2	IO_L45P_2/VREF_2	H2	
2	IO_L46N_2	J3	
2	IO_L46P_2	H3	
2	IO_L47N_2	M9	
2	IO_L47P_2	N9	
2	IO_L48N_2	L5	
2	IO_L48P_2	K5	
2	IO_L49N_2	K2	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L49P_2	J2	
2	IO_L50N_2	N7	
2	IO_L50P_2	M7	
2	IO_L51N_2	L6	
2	IO_L51P_2/VREF_2	M6	
2	IO_L52N_2	M3	
2	IO_L52P_2	L3	
2	IO_L53N_2	L4	
2	IO_L53P_2	K4	
2	IO_L54N_2	N4	
2	IO_L54P_2	M4	
2	IO_L67N_2	M2	
2	IO_L67P_2	L2	
2	IO_L68N_2	N8	
2	IO_L68P_2	P8	
2	IO_L69N_2	N6	
2	IO_L69P_2/VREF_2	P6	
2	IO_L70N_2	P5	
2	IO_L70P_2	N5	
2	IO_L71N_2	P10	
2	IO_L71P_2	R10	
2	IO_L72N_2	P3	
2	IO_L72P_2	N3	
2	IO_L73N_2	M1	
2	IO_L73P_2	L1	
2	IO_L74N_2	P9	
2	IO_L74P_2	R9	
2	IO_L75N_2	P2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	R4	
2	IO_L76P_2	P4	
2	IO_L77N_2	R8	
2	IO_L77P_2	T8	
2	IO_L78N_2	T3	
2	IO_L78P_2	R3	
2	IO_L79N_2	P1	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L79P_2	N1	NC
2	IO_L80N_2	T11	NC
2	IO_L80P_2	U11	NC
2	IO_L81N_2	R7	NC
2	IO_L81P_2/VREF_2	R6	NC
2	IO_L82N_2	U5	NC
2	IO_L82P_2	T5	NC
2	IO_L83N_2	T10	NC
2	IO_L83P_2	U10	NC
2	IO_L84N_2	U4	NC
2	IO_L84P_2	T4	NC
2	IO_L91N_2	T2	
2	IO_L91P_2	R1	
2	IO_L92N_2	U7	
2	IO_L92P_2	T7	
2	IO_L93N_2	T6	
2	IO_L93P_2/VREF_2	U6	
2	IO_L94N_2	U1	
2	IO_L94P_2	U2	
2	IO_L95N_2	U9	
2	IO_L95P_2	U8	
2	IO_L96N_2	U3	
2	IO_L96P_2	V4	
3	IO_L96N_3	V6	
3	IO_L96P_3	W6	
3	IO_L95N_3	V5	
3	IO_L95P_3	W5	
3	IO_L94N_3	V7	
3	IO_L94P_3	W7	
3	IO_L93N_3/VREF_3	V10	
3	IO_L93P_3	W10	
3	IO_L92N_3	V1	
3	IO_L92P_3	V2	
3	IO_L91N_3	W3	
3	IO_L91P_3	Y3	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L84N_3	V9	NC
3	IO_L84P_3	V8	NC
3	IO_L83N_3	W4	NC
3	IO_L83P_3	Y4	NC
3	IO_L82N_3	W11	NC
3	IO_L82P_3	V11	NC
3	IO_L81N_3/VREF_3	W8	NC
3	IO_L81P_3	Y8	NC
3	IO_L80N_3	W2	NC
3	IO_L80P_3	Y1	NC
3	IO_L79N_3	AA3	NC
3	IO_L79P_3	AB3	NC
3	IO_L78N_3	Y6	
3	IO_L78P_3	AA6	
3	IO_L77N_3	AA4	
3	IO_L77P_3	AB4	
3	IO_L76N_3	Y7	
3	IO_L76P_3	AA8	
3	IO_L75N_3/VREF_3	Y10	
3	IO_L75P_3	AA10	
3	IO_L74N_3	AA1	
3	IO_L74P_3	AB1	
3	IO_L73N_3	AA5	
3	IO_L73P_3	AB5	
3	IO_L72N_3	AA9	
3	IO_L72P_3	Y9	
3	IO_L71N_3	AA2	
3	IO_L71P_3	AB2	
3	IO_L70N_3	AB6	
3	IO_L70P_3	AC6	
3	IO_L69N_3/VREF_3	AD1	
3	IO_L69P_3	AC1	
3	IO_L68N_3	AC3	
3	IO_L68P_3	AD3	
3	IO_L67N_3	AC4	
3	IO_L67P_3	AD4	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L54N_3	AB7	
3	IO_L54P_3	AC7	
3	IO_L53N_3	AC2	
3	IO_L53P_3	AD2	
3	IO_L52N_3	AC8	
3	IO_L52P_3	AB8	
3	IO_L51N_3/VREF_3	AB10	
3	IO_L51P_3	AC10	
3	IO_L50N_3	AD5	
3	IO_L50P_3	AE5	
3	IO_L49N_3	AE4	
3	IO_L49P_3	AF4	
3	IO_L48N_3	AB9	
3	IO_L48P_3	AC9	
3	IO_L47N_3	AE2	
3	IO_L47P_3	AF1	
3	IO_L46N_3	AD6	
3	IO_L46P_3	AE6	
3	IO_L45N_3/VREF_3	AD9	
3	IO_L45P_3	AE9	
3	IO_L44N_3	AF2	
3	IO_L44P_3	AG2	
3	IO_L43N_3	AF3	
3	IO_L43P_3	AG3	
3	IO_L30N_3	AD7	
3	IO_L30P_3	AE7	
3	IO_L29N_3	AF5	
3	IO_L29P_3	AG5	
3	IO_L28N_3	AE8	
3	IO_L28P_3	AD8	
3	IO_L27N_3/VREF_3	AF8	
3	IO_L27P_3	AF9	
3	IO_L26N_3	AH1	
3	IO_L26P_3	AJ1	
3	IO_L25N_3	AG4	
3	IO_L25P_3	AH5	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L24N_3	AF6	
3	IO_L24P_3	AG6	
3	IO_L23N_3	AH3	
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/DOUT	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	
4	IO_L20N_4	AJ10	
4	IO_L20P_4	AJ9	
4	IO_L21N_4	AH9	
4	IO_L21P_4/VREF_4	AH10	
4	IO_L22N_4	AN5	
4	IO_L22P_4	AN4	
4	IO_L23N_4	AE12	
4	IO_L23P_4	AE13	
4	IO_L24N_4	AM9	
4	IO_L24P_4	AL8	
4	IO_L25N_4	AP5	
4	IO_L25P_4	AP4	
4	IO_L26N_4	AG11	
4	IO_L26P_4	AG12	
4	IO_L27N_4	AN7	
4	IO_L27P_4/VREF_4	AN6	
4	IO_L28N_4	AL10	
4	IO_L28P_4	AL9	
4	IO_L29N_4	AF12	
4	IO_L29P_4	AF13	
4	IO_L30N_4	AK10	
4	IO_L30P_4	AK11	
4	IO_L49N_4	AP7	
4	IO_L49P_4	AP6	
4	IO_L50N_4	AH13	
4	IO_L50P_4	AH12	
4	IO_L51N_4	AJ11	
4	IO_L51P_4/VREF_4	AJ12	
4	IO_L52N_4	AP9	
4	IO_L52P_4	AN8	
4	IO_L53N_4	AG13	
4	IO_L53P_4	AG14	
4	IO_L54N_4	AM11	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L54P_4	AL11	
4	IO_L60N_4	AN10	NC
4	IO_L60P_4	AN9	NC
4	IO_L67N_4	AN12	
4	IO_L67P_4	AN11	
4	IO_L68N_4	AE14	
4	IO_L68P_4	AE15	
4	IO_L69N_4	AJ13	
4	IO_L69P_4/VREF_4	AJ14	
4	IO_L70N_4	AL13	
4	IO_L70P_4	AL12	
4	IO_L71N_4	AF14	
4	IO_L71P_4	AF15	
4	IO_L72N_4	AM13	
4	IO_L72P_4	AM12	
4	IO_L73N_4	AP12	
4	IO_L73P_4	AP11	
4	IO_L74N_4	AG15	
4	IO_L74P_4	AG16	
4	IO_L75N_4	AN14	
4	IO_L75P_4/VREF_4	AN13	
4	IO_L76N_4	AP14	
4	IO_L76P_4	AP13	
4	IO_L77N_4	AD16	
4	IO_L77P_4	AD17	
4	IO_L78N_4	AK14	
4	IO_L78P_4	AK13	
4	IO_L79N_4	AN16	NC
4	IO_L79P_4	AP15	NC
4	IO_L80N_4	AE16	NC
4	IO_L80P_4	AE17	NC
4	IO_L81N_4	AH15	NC
4	IO_L81P_4/VREF_4	AJ15	NC
4	IO_L82N_4	AP17	NC
4	IO_L82P_4	AN17	NC
4	IO_L83N_4	AH17	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L83P_4	AH16	NC
4	IO_L84N_4	AL15	NC
4	IO_L84P_4	AL14	NC
4	IO_L91N_4/VREF_4	AL16	
4	IO_L91P_4	AL17	
4	IO_L92N_4	AJ17	
4	IO_L92P_4	AJ16	
4	IO_L93N_4	AM15	
4	IO_L93P_4	AM14	
4	IO_L94N_4/VREF_4	AM16	
4	IO_L94P_4	AM17	
4	IO_L95N_4/GCLK3S	AF17	
4	IO_L95P_4/GCLK2P	AG17	
4	IO_L96N_4/GCLK1S	AK16	
4	IO_L96P_4/GCLK0P	AK17	
5	IO_L96N_5/GCLK7S	AK18	
5	IO_L96P_5/GCLK6P	AK19	
5	IO_L95N_5/GCLK5S	AG18	
5	IO_L95P_5/GCLK4P	AF18	
5	IO_L94N_5	AL18	
5	IO_L94P_5/VREF_5	AL19	
5	IO_L93N_5	AJ19	
5	IO_L93P_5	AJ18	
5	IO_L92N_5	AH19	
5	IO_L92P_5	AH18	
5	IO_L91N_5	AM19	
5	IO_L91P_5/VREF_5	AM20	
5	IO_L84N_5	AL21	NC
5	IO_L84P_5	AL20	NC
5	IO_L83N_5	AM22	NC
5	IO_L83P_5	AM21	NC
5	IO_L82N_5	AN18	NC
5	IO_L82P_5	AP18	NC
5	IO_L81N_5/VREF_5	AP20	NC
5	IO_L81P_5	AN19	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L80N_5	AE18	NC
5	IO_L80P_5	AE19	NC
5	IO_L79N_5	AP22	NC
5	IO_L79P_5	AP21	NC
5	IO_L78N_5	AK22	
5	IO_L78P_5	AK21	
5	IO_L77N_5	AD18	
5	IO_L77P_5	AD19	
5	IO_L76N_5	AN22	
5	IO_L76P_5	AN21	
5	IO_L75N_5/VREF_5	AJ20	
5	IO_L75P_5	AH20	
5	IO_L74N_5	AG19	
5	IO_L74P_5	AG20	
5	IO_L73N_5	AP24	
5	IO_L73P_5	AP23	
5	IO_L72N_5	AL23	
5	IO_L72P_5	AL22	
5	IO_L71N_5	AF20	
5	IO_L71P_5	AF21	
5	IO_L70N_5	AM24	
5	IO_L70P_5	AM23	
5	IO_L69N_5/VREF_5	AJ21	
5	IO_L69P_5	AJ22	
5	IO_L68N_5	AJ24	
5	IO_L68P_5	AJ23	
5	IO_L67N_5	AN24	
5	IO_L67P_5	AN23	
5	IO_L60N_5	AN26	NC
5	IO_L60P_5	AN25	NC
5	IO_L54N_5	AL25	
5	IO_L54P_5	AL24	
5	IO_L53N_5	AE20	
5	IO_L53P_5	AE21	
5	IO_L52N_5	AN27	
5	IO_L52P_5	AP26	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L51N_5/VREF_5	AP29	
5	IO_L51P_5	AP28	
5	IO_L50N_5	AG21	
5	IO_L50P_5	AG22	
5	IO_L49N_5	AN29	
5	IO_L49P_5	AN28	
5	IO_L30N_5	AK24	
5	IO_L30P_5	AK25	
5	IO_L29N_5	AH23	
5	IO_L29P_5	AH22	
5	IO_L28N_5	AP31	
5	IO_L28P_5	AP30	
5	IO_L27N_5/VREF_5	AH24	
5	IO_L27P_5	AH25	
5	IO_L26N_5	AF22	
5	IO_L26P_5	AF23	
5	IO_L25N_5	AM27	
5	IO_L25P_5	AM26	
5	IO_L24N_5	AL27	
5	IO_L24P_5	AL26	
5	IO_L23N_5	AH26	
5	IO_L23P_5	AJ25	
5	IO_L22N_5	AN31	
5	IO_L22P_5	AN30	
5	IO_L21N_5/VREF_5	AK26	
5	IO_L21P_5	AK27	
5	IO_L20N_5	AG23	
5	IO_L20P_5	AF24	
5	IO_L19N_5	AM33	
5	IO_L19P_5	AN32	
5	IO_L06N_5	AJ27	
5	IO_L06P_5	AJ26	
5	IO_L05N_5/VRP_5	AE22	
5	IO_L05P_5/VRN_5	AE23	
5	IO_L04N_5	AM28	
5	IO_L04P_5/VREF_5	AM29	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L03N_5/D4/ALT_VRP_5	AK28	
5	IO_L03P_5/D5/ALT_VRN_5	AL29	
5	IO_L02N_5/D6	AG24	
5	IO_L02P_5/D7	AG25	
5	IO_L01N_5/RDWR_B	AL30	
5	IO_L01P_5/CS_B	AM31	
6	IO_L01P_6	AE24	
6	IO_L01N_6	AD25	
6	IO_L02P_6/VRN_6	AJ30	
6	IO_L02N_6/VRP_6	AH30	
6	IO_L03P_6	AL32	
6	IO_L03N_6/VREF_6	AK32	
6	IO_L04P_6	AF25	
6	IO_L04N_6	AE25	
6	IO_L05P_6	AJ31	
6	IO_L05N_6	AK31	
6	IO_L06P_6	AH29	
6	IO_L06N_6	AG29	
6	IO_L19P_6	AG26	
6	IO_L19N_6	AF26	
6	IO_L20P_6	AL33	
6	IO_L20N_6	AK33	
6	IO_L21P_6	AJ32	
6	IO_L21N_6/VREF_6	AH32	
6	IO_L22P_6	AG28	
6	IO_L22N_6	AF28	
6	IO_L23P_6	AG30	
6	IO_L23N_6	AF30	
6	IO_L24P_6	AF29	
6	IO_L24N_6	AE29	
6	IO_L25P_6	AF27	
6	IO_L25N_6	AE27	
6	IO_L26P_6	AL34	
6	IO_L26N_6	AK34	
6	IO_L27P_6	AE28	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L27N_6/VREF_6	AD28	
6	IO_L28P_6	AE26	
6	IO_L28N_6	AD26	
6	IO_L29P_6	AF31	
6	IO_L29N_6	AG31	
6	IO_L30P_6	AF32	
6	IO_L30N_6	AG32	
6	IO_L43P_6	AC25	
6	IO_L43N_6	AB25	
6	IO_L44P_6	AJ33	
6	IO_L44N_6	AH33	
6	IO_L45P_6	AE31	
6	IO_L45N_6/VREF_6	AD32	
6	IO_L46P_6	AD27	
6	IO_L46N_6	AC27	
6	IO_L47P_6	AJ34	
6	IO_L47N_6	AH34	
6	IO_L48P_6	AE30	
6	IO_L48N_6	AD30	
6	IO_L49P_6	AC26	
6	IO_L49N_6	AB26	
6	IO_L50P_6	AD29	
6	IO_L50N_6	AC29	
6	IO_L51P_6	AF33	
6	IO_L51N_6/VREF_6	AG33	
6	IO_L52P_6	AC28	
6	IO_L52N_6	AB28	
6	IO_L53P_6	AF34	
6	IO_L53N_6	AE33	
6	IO_L54P_6	AB27	
6	IO_L54N_6	AA27	
6	IO_L67P_6	AA25	
6	IO_L67N_6	Y25	
6	IO_L68P_6	AD33	
6	IO_L68N_6	AC33	
6	IO_L69P_6	AC32	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L69N_6/VREF_6	AB32	
6	IO_L70P_6	AA26	
6	IO_L70N_6	Y26	
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	
6	IO_L95P_6	W30	
6	IO_L95N_6	V30	
6	IO_L96P_6	V32	
6	IO_L96N_6	W32	
7	IO_L96P_7	U31	
7	IO_L96N_7	V31	
7	IO_L95P_7	T28	
7	IO_L95N_7	U28	
7	IO_L94P_7	U33	
7	IO_L94N_7	U34	
7	IO_L93P_7/VREF_7	U29	
7	IO_L93N_7	T29	
7	IO_L92P_7	U27	
7	IO_L92N_7	U26	
7	IO_L91P_7	T30	
7	IO_L91N_7	U30	
7	IO_L84P_7	R32	NC
7	IO_L84N_7	T32	NC
7	IO_L83P_7	U25	NC
7	IO_L83N_7	T25	NC
7	IO_L82P_7	R34	NC
7	IO_L82N_7	T33	NC
7	IO_L81P_7/VREF_7	N34	NC
7	IO_L81N_7	P34	NC
7	IO_L80P_7	U24	NC
7	IO_L80N_7	T24	NC
7	IO_L79P_7	R31	NC
7	IO_L79N_7	T31	NC
7	IO_L78P_7	N32	
7	IO_L78N_7	P32	
7	IO_L77P_7	T27	
7	IO_L77N_7	R27	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L76P_7	N33	
7	IO_L76N_7	P33	
7	IO_L75P_7/VREF_7	R29	
7	IO_L75N_7	R28	
7	IO_L74P_7	R26	
7	IO_L74N_7	P26	
7	IO_L73P_7	N31	
7	IO_L73N_7	P31	
7	IO_L72P_7	N30	
7	IO_L72N_7	P30	
7	IO_L71P_7	R25	
7	IO_L71N_7	P25	
7	IO_L70P_7	L34	
7	IO_L70N_7	M34	
7	IO_L69P_7/VREF_7	P29	
7	IO_L69N_7	N29	
7	IO_L68P_7	P27	
7	IO_L68N_7	N27	
7	IO_L67P_7	L32	
7	IO_L67N_7	M32	
7	IO_L54P_7	L31	
7	IO_L54N_7	M31	
7	IO_L53P_7	K29	
7	IO_L53N_7	L30	
7	IO_L52P_7	L33	
7	IO_L52N_7	M33	
7	IO_L51P_7/VREF_7	M29	
7	IO_L51N_7	L29	
7	IO_L50P_7	M28	
7	IO_L50N_7	N28	
7	IO_L49P_7	K30	
7	IO_L49N_7	K31	
7	IO_L48P_7	H32	
7	IO_L48N_7	J32	
7	IO_L47P_7	N26	
7	IO_L47N_7	M26	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L46P_7	J33	
7	IO_L46N_7	K33	
7	IO_L45P_7/VREF_7	H33	
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	
7	IO_L03N_7	F30	
7	IO_L02P_7/VRN_7	K25	
7	IO_L02N_7/VRP_7	J25	
7	IO_L01P_7	D33	
7	IO_L01N_7	E33	
0	VCCO_0	M22	
0	VCCO_0	M21	
0	VCCO_0	M20	
0	VCCO_0	M19	
0	VCCO_0	M18	
0	VCCO_0	L23	
0	VCCO_0	L22	
0	VCCO_0	L21	
0	VCCO_0	L20	
0	VCCO_0	E20	
0	VCCO_0	D28	
0	VCCO_0	A25	
0	VCCO_0	A19	
1	VCCO_1	M17	
1	VCCO_1	M16	
1	VCCO_1	M15	
1	VCCO_1	M14	
1	VCCO_1	M13	
1	VCCO_1	L15	
1	VCCO_1	L14	
1	VCCO_1	L13	
1	VCCO_1	L12	
1	VCCO_1	E15	
1	VCCO_1	D7	
1	VCCO_1	A16	
1	VCCO_1	A10	
2	VCCO_2	U12	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	T12	
2	VCCO_2	T1	
2	VCCO_2	R12	
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	
5	VCCO_5	AP19	
5	VCCO_5	AL28	
5	VCCO_5	AK20	
5	VCCO_5	AD23	
5	VCCO_5	AD22	
5	VCCO_5	AD21	
5	VCCO_5	AD20	
5	VCCO_5	AC22	
5	VCCO_5	AC21	
5	VCCO_5	AC20	
5	VCCO_5	AC19	
5	VCCO_5	AC18	
6	VCCO_6	AH31	
6	VCCO_6	AE34	
6	VCCO_6	AC24	
6	VCCO_6	AB24	
6	VCCO_6	AB23	
6	VCCO_6	AA24	
6	VCCO_6	AA23	
6	VCCO_6	Y30	
6	VCCO_6	Y24	
6	VCCO_6	Y23	
6	VCCO_6	W34	
6	VCCO_6	W23	
6	VCCO_6	V23	
7	VCCO_7	U23	
7	VCCO_7	T34	
7	VCCO_7	T23	
7	VCCO_7	R30	
7	VCCO_7	R24	
7	VCCO_7	R23	
7	VCCO_7	P24	
7	VCCO_7	P23	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	VCCO_7	N24	
7	VCCO_7	N23	
7	VCCO_7	M24	
7	VCCO_7	K34	
7	VCCO_7	G31	
NA	CCLK	AH8	
NA	PROG_B	D30	
NA	DONE	AJ7	
NA	M0	AH27	
NA	M1	AJ28	
NA	M2	AK29	
NA	HSWAP_EN	E29	
NA	TCK	F7	
NA	TDI	C31	
NA	TDO	D5	
NA	TMS	E6	
NA	PWRDWN_B	AK6	
NA	DXN	F28	
NA	DXP	G27	
NA	VBATT	C4	
NA	RSVD	G8	
NA	VCCAUX	AM30	
NA	VCCAUX	AM18	
NA	VCCAUX	AM5	
NA	VCCAUX	V3	
NA	VCCAUX	U32	
NA	VCCAUX	C30	
NA	VCCAUX	C17	
NA	VCCAUX	C5	
NA	VCCINT	AD24	
NA	VCCINT	AD11	
NA	VCCINT	AC23	
NA	VCCINT	AC12	
NA	VCCINT	AB22	
NA	VCCINT	AB21	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	VCCINT	AB20	
NA	VCCINT	AB19	
NA	VCCINT	AB18	
NA	VCCINT	AB17	
NA	VCCINT	AB16	
NA	VCCINT	AB15	
NA	VCCINT	AB14	
NA	VCCINT	AB13	
NA	VCCINT	AA22	
NA	VCCINT	AA13	
NA	VCCINT	Y22	
NA	VCCINT	Y13	
NA	VCCINT	W22	
NA	VCCINT	W13	
NA	VCCINT	V22	
NA	VCCINT	V13	
NA	VCCINT	U22	
NA	VCCINT	U13	
NA	VCCINT	T22	
NA	VCCINT	T13	
NA	VCCINT	R22	
NA	VCCINT	R13	
NA	VCCINT	P22	
NA	VCCINT	P13	
NA	VCCINT	N22	
NA	VCCINT	N21	
NA	VCCINT	N20	
NA	VCCINT	N19	
NA	VCCINT	N18	
NA	VCCINT	N17	
NA	VCCINT	N16	
NA	VCCINT	N15	
NA	VCCINT	N14	
NA	VCCINT	N13	
NA	VCCINT	M23	
NA	VCCINT	M12	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	VCCINT	L24	
NA	VCCINT	L11	
NA	GND	AP33	
NA	GND	AP32	
NA	GND	AP27	
NA	GND	AP8	
NA	GND	AP3	
NA	GND	AP2	
NA	GND	AN34	
NA	GND	AN33	
NA	GND	AN20	
NA	GND	AN15	
NA	GND	AN2	
NA	GND	AN1	
NA	GND	AM34	
NA	GND	AM32	
NA	GND	AM25	
NA	GND	AM10	
NA	GND	AM3	
NA	GND	AM1	
NA	GND	AL31	
NA	GND	AL4	
NA	GND	AK30	
NA	GND	AK23	
NA	GND	AK12	
NA	GND	AK5	
NA	GND	AJ29	
NA	GND	AJ6	
NA	GND	AH28	
NA	GND	AH21	
NA	GND	AH14	
NA	GND	AH7	
NA	GND	AG34	
NA	GND	AG27	
NA	GND	AG8	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	AG1	
NA	GND	AF19	
NA	GND	AF16	
NA	GND	AE32	
NA	GND	AE3	
NA	GND	AC30	
NA	GND	AC5	
NA	GND	AA28	
NA	GND	AA21	
NA	GND	AA20	
NA	GND	AA19	
NA	GND	AA18	
NA	GND	AA17	
NA	GND	AA16	
NA	GND	AA15	
NA	GND	AA14	
NA	GND	AA7	
NA	GND	Y33	
NA	GND	Y21	
NA	GND	Y20	
NA	GND	Y19	
NA	GND	Y18	
NA	GND	Y17	
NA	GND	Y16	
NA	GND	Y15	
NA	GND	Y14	
NA	GND	Y2	
NA	GND	W26	
NA	GND	W21	
NA	GND	W20	
NA	GND	W19	
NA	GND	W18	
NA	GND	W17	
NA	GND	W16	
NA	GND	W15	
NA	GND	W14	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	W9	
NA	GND	V21	
NA	GND	V20	
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	

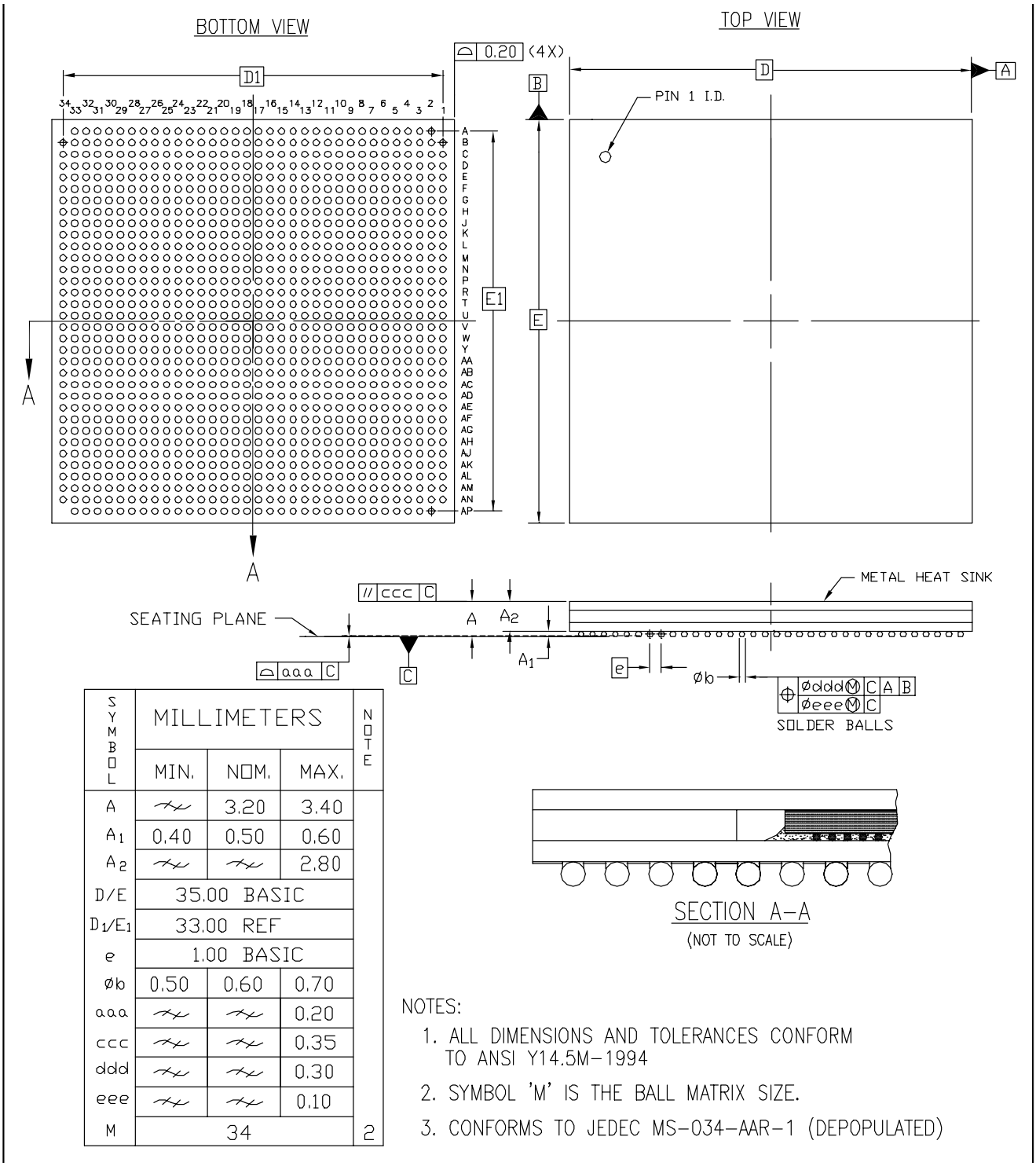
Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, XC2V8000, & XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	
NA	GND	B34	
NA	GND	B33	
NA	GND	B20	
NA	GND	B15	
NA	GND	B2	
NA	GND	B1	
NA	GND	A33	
NA	GND	A32	
NA	GND	A27	
NA	GND	A8	
NA	GND	A3	
NA	GND	A2	

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 8: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2V4000, XC2V6000, XC2V8000, and XC2V10000 Virtex-II devices are available in the FF1517 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V4000 and XC2V6000 devices shown in the No Connect columns. Following this table are the **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L01N_0	B36		
0	IO_L01P_0	C36		
0	IO_L02N_0	J30		
0	IO_L02P_0	J29		
0	IO_L03N_0/VRP_0	D33		
0	IO_L03P_0/VRN_0	D34		
0	IO_L04N_0/VREF_0	C34		
0	IO_L04P_0	C35		
0	IO_L05N_0	H30		
0	IO_L05P_0	G30		
0	IO_L06N_0	D32		
0	IO_L06P_0	E33		
0	IO_L07N_0	A35	NC	
0	IO_L07P_0	A36	NC	
0	IO_L08N_0	K28	NC	
0	IO_L08P_0	J28	NC	
0	IO_L09N_0	E32	NC	
0	IO_L09P_0/VREF_0	F32	NC	
0	IO_L10N_0	B34	NC	
0	IO_L10P_0	B35	NC	
0	IO_L11N_0	H29	NC	
0	IO_L11P_0	H28	NC	
0	IO_L12N_0	F31	NC	
0	IO_L12P_0	G31	NC	
0	IO_L19N_0	C32		
0	IO_L19P_0	C33		
0	IO_L20N_0	M26		
0	IO_L20P_0	M25		
0	IO_L21N_0	E30		
0	IO_L21P_0/VREF_0	E31		
0	IO_L22N_0	A33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L22P_0	A34		
0	IO_L23N_0	K27		
0	IO_L23P_0	K26		
0	IO_L24N_0	F29		
0	IO_L24P_0	F30		
0	IO_L25N_0	B32		
0	IO_L25P_0	B33		
0	IO_L26N_0	L26		
0	IO_L26P_0	L25		
0	IO_L27N_0	G28		
0	IO_L27P_0/VREF_0	G29		
0	IO_L28N_0	C30		
0	IO_L28P_0	C31		
0	IO_L29N_0	J27		
0	IO_L29P_0	J26		
0	IO_L30N_0	D30		
0	IO_L30P_0	D31		
0	IO_L31N_0	A31	NC	
0	IO_L31P_0	A32	NC	
0	IO_L32N_0	H27	NC	
0	IO_L32P_0	H26	NC	
0	IO_L33N_0	F27	NC	
0	IO_L33P_0/VREF_0	F28	NC	
0	IO_L34N_0	B30	NC	
0	IO_L34P_0	B31	NC	
0	IO_L35N_0	M24	NC	
0	IO_L35P_0	M23	NC	
0	IO_L36N_0	D28	NC	
0	IO_L36P_0	D29	NC	
0	IO_L49N_0	C28		
0	IO_L49P_0	C29		
0	IO_L50N_0	K25		
0	IO_L50P_0	L24		
0	IO_L51N_0	E27		
0	IO_L51P_0/VREF_0	E28		
0	IO_L52N_0	A29		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L52P_0	A30		
0	IO_L53N_0	G26		
0	IO_L53P_0	G25		
0	IO_L54N_0	D26		
0	IO_L54P_0	D27		
0	IO_L55N_0	B27		
0	IO_L55P_0	B28		
0	IO_L56N_0	H25		
0	IO_L56P_0	H24		
0	IO_L57N_0	F25		
0	IO_L57P_0/VREF_0	F26		
0	IO_L58N_0	A27		
0	IO_L58P_0	A28		
0	IO_L59N_0	K24		
0	IO_L59P_0	K23		
0	IO_L60N_0	E24		
0	IO_L60P_0	E25		
0	IO_L67N_0	C26		
0	IO_L67P_0	C27		
0	IO_L68N_0	J24		
0	IO_L68P_0	J23		
0	IO_L69N_0	D24		
0	IO_L69P_0/VREF_0	D25		
0	IO_L70N_0	A25		
0	IO_L70P_0	A26		
0	IO_L71N_0	M22		
0	IO_L71P_0	M21		
0	IO_L72N_0	G23		
0	IO_L72P_0	G24		
0	IO_L73N_0	B25		
0	IO_L73P_0	C25		
0	IO_L74N_0	L22		
0	IO_L74P_0	L21		
0	IO_L75N_0	F23		
0	IO_L75P_0/VREF_0	F24		
0	IO_L76N_0	C23		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L76P_0	C24		
0	IO_L77N_0	K22		
0	IO_L77P_0	K21		
0	IO_L78N_0	E22		
0	IO_L78P_0	E23		
0	IO_L79N_0	B23		
0	IO_L79P_0	B24		
0	IO_L80N_0	J22		
0	IO_L80P_0	J21		
0	IO_L81N_0	G21		
0	IO_L81P_0/VREF_0	G22		
0	IO_L82N_0	A23		
0	IO_L82P_0	A24		
0	IO_L83N_0	H22		
0	IO_L83P_0	H21		
0	IO_L84N_0	F21		
0	IO_L84P_0	F22		
0	IO_L91N_0/VREF_0	B21		
0	IO_L91P_0	B22		
0	IO_L92N_0	L20		
0	IO_L92P_0	M20		
0	IO_L93N_0	E21		
0	IO_L93P_0	D22		
0	IO_L94N_0/VREF_0	A21		
0	IO_L94P_0	A22		
0	IO_L95N_0/GCLK7P	H20		
0	IO_L95P_0/GCLK6S	J20		
0	IO_L96N_0/GCLK5P	C21		
0	IO_L96P_0/GCLK4S	D21		
1	IO_L96N_1/GCLK3P	F19		
1	IO_L96P_1/GCLK2S	F20		
1	IO_L95N_1/GCLK1P	H19		
1	IO_L95P_1/GCLK0S	H18		
1	IO_L94N_1	C19		
1	IO_L94P_1/VREF_1	C20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L69N_1/VREF_1	E15		
1	IO_L69P_1	E16		
1	IO_L68N_1	K17		
1	IO_L68P_1	K16		
1	IO_L67N_1	C15		
1	IO_L67P_1	B15		
1	IO_L60N_1	F15		
1	IO_L60P_1	F16		
1	IO_L59N_1	H16		
1	IO_L59P_1	H15		
1	IO_L58N_1	C13		
1	IO_L58P_1	C14		
1	IO_L57N_1/VREF_1	D13		
1	IO_L57P_1	D14		
1	IO_L56N_1	M17		
1	IO_L56P_1	M16		
1	IO_L55N_1	A12		
1	IO_L55P_1	A13		
1	IO_L54N_1	B12		
1	IO_L54P_1	B13		
1	IO_L53N_1	G15		
1	IO_L53P_1	G14		
1	IO_L52N_1	C11		
1	IO_L52P_1	C12		
1	IO_L51N_1/VREF_1	F13		
1	IO_L51P_1	F14		
1	IO_L50N_1	L16		
1	IO_L50P_1	L15		
1	IO_L49N_1	A10		
1	IO_L49P_1	A11		
1	IO_L36N_1	E12	NC	
1	IO_L36P_1	E13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J14	NC	
1	IO_L34N_1	B9	NC	
1	IO_L34P_1	B10	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L09P_2/VREF_2	H7	NC	
2	IO_L10N_2	G3	NC	
2	IO_L10P_2	F3	NC	
2	IO_L11N_2	J8	NC	
2	IO_L11P_2	K8	NC	
2	IO_L12N_2	H5	NC	
2	IO_L12P_2	G5	NC	
2	IO_L19N_2	G1		
2	IO_L19P_2	F1		
2	IO_L20N_2	K9		
2	IO_L20P_2	L10		
2	IO_L21N_2	K7		
2	IO_L21P_2/VREF_2	J7		
2	IO_L22N_2	H2		
2	IO_L22P_2	G2		
2	IO_L23N_2	L9		
2	IO_L23P_2	M9		
2	IO_L24N_2	H4		
2	IO_L24P_2	G4		
2	IO_L25N_2	J3		
2	IO_L25P_2	H3		
2	IO_L26N_2	M10		
2	IO_L26P_2	N10		
2	IO_L27N_2	K6		
2	IO_L27P_2/VREF_2	J6		
2	IO_L28N_2	K5		
2	IO_L28P_2	J5		
2	IO_L29N_2	N11		
2	IO_L29P_2	P11		
2	IO_L30N_2	M7		
2	IO_L30P_2	L7		
2	IO_L31N_2	J1	NC	
2	IO_L31P_2	H1	NC	
2	IO_L32N_2	L8	NC	
2	IO_L32P_2	M8	NC	
2	IO_L33N_2	K4	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L57P_2/VREF_2	P7		
2	IO_L58N_2	R3		
2	IO_L58P_2	P3		
2	IO_L59N_2	T10		
2	IO_L59P_2	U10		
2	IO_L60N_2	P4		
2	IO_L60P_2	N4		
2	IO_L67N_2	T6		
2	IO_L67P_2	R6		
2	IO_L68N_2	T9		
2	IO_L68P_2	U9		
2	IO_L69N_2	T5		
2	IO_L69P_2/VREF_2	R5		
2	IO_L70N_2	R1		
2	IO_L70P_2	P1		
2	IO_L71N_2	V12		
2	IO_L71P_2	W12		
2	IO_L72N_2	T4		
2	IO_L72P_2	R4		
2	IO_L73N_2	T2		
2	IO_L73P_2	R2		
2	IO_L74N_2	V11		
2	IO_L74P_2	W11		
2	IO_L75N_2	U7		
2	IO_L75P_2/VREF_2	T7		
2	IO_L76N_2	U3		
2	IO_L76P_2	T3		
2	IO_L77N_2	V10		
2	IO_L77P_2	W10		
2	IO_L78N_2	V6		
2	IO_L78P_2	U6		
2	IO_L79N_2	U1		
2	IO_L79P_2	T1		
2	IO_L80N_2	V9		
2	IO_L80P_2	W9		
2	IO_L81N_2	V5		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L81P_2/VREF_2	U5		
2	IO_L82N_2	V2		
2	IO_L82P_2	U2		
2	IO_L83N_2	V8		
2	IO_L83P_2	W8		
2	IO_L84N_2	W7		
2	IO_L84P_2	V7		
2	IO_L91N_2	W1		
2	IO_L91P_2	V1		
2	IO_L92N_2	Y11		
2	IO_L92P_2	Y12		
2	IO_L93N_2	W4		
2	IO_L93P_2/VREF_2	V4		
2	IO_L94N_2	W2		
2	IO_L94P_2	W3		
2	IO_L95N_2	Y8		
2	IO_L95P_2	Y9		
2	IO_L96N_2	W5		
2	IO_L96P_2	W6		
3	IO_L96N_3	AB8		
3	IO_L96P_3	AA8		
3	IO_L95N_3	Y3		
3	IO_L95P_3	AA3		
3	IO_L94N_3	Y6		
3	IO_L94P_3	AA6		
3	IO_L93N_3/VREF_3	AB9		
3	IO_L93P_3	AA9		
3	IO_L92N_3	AA1		
3	IO_L92P_3	AB1		
3	IO_L91N_3	Y5		
3	IO_L91P_3	AA5		
3	IO_L84N_3	AB10		
3	IO_L84P_3	AA10		
3	IO_L83N_3	AA2		
3	IO_L83P_3	AB2		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L82N_3	AA4		
3	IO_L82P_3	AB4		
3	IO_L81N_3/VREF_3	AB11		
3	IO_L81P_3	AA11		
3	IO_L80N_3	AC1		
3	IO_L80P_3	AD1		
3	IO_L79N_3	AA7		
3	IO_L79P_3	AB7		
3	IO_L78N_3	AB12		
3	IO_L78P_3	AA12		
3	IO_L77N_3	AC2		
3	IO_L77P_3	AC3		
3	IO_L76N_3	AB5		
3	IO_L76P_3	AC5		
3	IO_L75N_3/VREF_3	AD9		
3	IO_L75P_3	AC9		
3	IO_L74N_3	AD2		
3	IO_L74P_3	AE2		
3	IO_L73N_3	AB6		
3	IO_L73P_3	AC6		
3	IO_L72N_3	AD10		
3	IO_L72P_3	AC10		
3	IO_L71N_3	AD3		
3	IO_L71P_3	AE3		
3	IO_L70N_3	AC7		
3	IO_L70P_3	AD7		
3	IO_L69N_3/VREF_3	AE8		
3	IO_L69P_3	AD8		
3	IO_L68N_3	AE1		
3	IO_L68P_3	AF1		
3	IO_L67N_3	AD4		
3	IO_L67P_3	AE4		
3	IO_L60N_3	AD12		
3	IO_L60P_3	AC12		
3	IO_L59N_3	AF3		
3	IO_L59P_3	AG3		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L58N_3	AD5		
3	IO_L58P_3	AE5		
3	IO_L57N_3/VREF_3	AE11		
3	IO_L57P_3	AD11		
3	IO_L56N_3	AG1		
3	IO_L56P_3	AH1		
3	IO_L55N_3	AD6		
3	IO_L55P_3	AE6		
3	IO_L54N_3	AF10		
3	IO_L54P_3	AE10		
3	IO_L53N_3	AG2		
3	IO_L53P_3	AH2		
3	IO_L52N_3	AF4		
3	IO_L52P_3	AG4		
3	IO_L51N_3/VREF_3	AG8		
3	IO_L51P_3	AF8		
3	IO_L50N_3	AH3		
3	IO_L50P_3	AJ3		
3	IO_L49N_3	AE7		
3	IO_L49P_3	AF7		
3	IO_L48N_3	AG9		
3	IO_L48P_3	AF9		
3	IO_L47N_3	AF6		
3	IO_L47P_3	AG6		
3	IO_L46N_3	AG5		
3	IO_L46P_3	AH5		
3	IO_L45N_3/VREF_3	AF12		
3	IO_L45P_3	AE12		
3	IO_L44N_3	AJ1		
3	IO_L44P_3	AK1		
3	IO_L43N_3	AH4		
3	IO_L43P_3	AJ4		
3	IO_L36N_3	AG11	NC	
3	IO_L36P_3	AF11	NC	
3	IO_L35N_3	AK2	NC	
3	IO_L35P_3	AL2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L34N_3	AH6	NC	
3	IO_L34P_3	AJ6	NC	
3	IO_L33N_3/VREF_3	AJ8	NC	
3	IO_L33P_3	AH8	NC	
3	IO_L32N_3	AL1	NC	
3	IO_L32P_3	AM1	NC	
3	IO_L31N_3	AH7	NC	
3	IO_L31P_3	AJ7	NC	
3	IO_L30N_3	AH10		
3	IO_L30P_3	AG10		
3	IO_L29N_3	AK3		
3	IO_L29P_3	AL3		
3	IO_L28N_3	AK4		
3	IO_L28P_3	AL4		
3	IO_L27N_3/VREF_3	AJ9		
3	IO_L27P_3	AH9		
3	IO_L26N_3	AM2		
3	IO_L26P_3	AN2		
3	IO_L25N_3	AK5		
3	IO_L25P_3	AL5		
3	IO_L24N_3	AK9		
3	IO_L24P_3	AK8		
3	IO_L23N_3	AN1		
3	IO_L23P_3	AP1		
3	IO_L22N_3	AK6		
3	IO_L22P_3	AL6		
3	IO_L21N_3/VREF_3	AH12		
3	IO_L21P_3	AG12		
3	IO_L20N_3	AM3		
3	IO_L20P_3	AN3		
3	IO_L19N_3	AM4		
3	IO_L19P_3	AN4		
3	IO_L12N_3	AJ12	NC	
3	IO_L12P_3	AH11	NC	
3	IO_L11N_3	AP2	NC	
3	IO_L11P_3	AR2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/DOUT	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L08P_4	AL12	NC	
4	IO_L09N_4	AP9	NC	
4	IO_L09P_4/VREF_4	AP8	NC	
4	IO_L10N_4	AV6	NC	
4	IO_L10P_4	AV5	NC	
4	IO_L11N_4	AM11	NC	
4	IO_L11P_4	AM12	NC	
4	IO_L12N_4	AN10	NC	
4	IO_L12P_4	AN9	NC	
4	IO_L19N_4	AU8		
4	IO_L19P_4	AU7		
4	IO_L20N_4	AH14		
4	IO_L20P_4	AH15		
4	IO_L21N_4	AT8		
4	IO_L21P_4/VREF_4	AT7		
4	IO_L22N_4	AW7		
4	IO_L22P_4	AW6		
4	IO_L23N_4	AK13		
4	IO_L23P_4	AK14		
4	IO_L24N_4	AR10		
4	IO_L24P_4	AR9		
4	IO_L25N_4	AV8		
4	IO_L25P_4	AV7		
4	IO_L26N_4	AJ14		
4	IO_L26P_4	AJ15		
4	IO_L27N_4	AP11		
4	IO_L27P_4/VREF_4	AP10		
4	IO_L28N_4	AU10		
4	IO_L28P_4	AU9		
4	IO_L29N_4	AL13		
4	IO_L29P_4	AL14		
4	IO_L30N_4	AN12		
4	IO_L30P_4	AN11		
4	IO_L31N_4	AW9	NC	
4	IO_L31P_4	AW8	NC	
4	IO_L32N_4	AM13	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L32P_4	AM14	NC	
4	IO_L33N_4	AT10	NC	
4	IO_L33P_4/VREF_4	AT9	NC	
4	IO_L34N_4	AV10	NC	
4	IO_L34P_4	AV9	NC	
4	IO_L35N_4	AH16	NC	
4	IO_L35P_4	AH17	NC	
4	IO_L36N_4	AP13	NC	
4	IO_L36P_4	AP12	NC	
4	IO_L49N_4	AU12		
4	IO_L49P_4	AU11		
4	IO_L50N_4	AK15		
4	IO_L50P_4	AJ16		
4	IO_L51N_4	AT12		
4	IO_L51P_4/VREF_4	AT11		
4	IO_L52N_4	AN15		
4	IO_L52P_4	AN14		
4	IO_L53N_4	AR12		
4	IO_L53P_4	AR13		
4	IO_L54N_4	AT14		
4	IO_L54P_4	AT13		
4	IO_L55N_4	AW11		
4	IO_L55P_4	AW10		
4	IO_L56N_4	AM15		
4	IO_L56P_4	AM16		
4	IO_L57N_4	AP15		
4	IO_L57P_4/VREF_4	AP14		
4	IO_L58N_4	AV13		
4	IO_L58P_4	AV12		
4	IO_L59N_4	AK16		
4	IO_L59P_4	AK17		
4	IO_L60N_4	AR16		
4	IO_L60P_4	AR15		
4	IO_L67N_4	AW13		
4	IO_L67P_4	AW12		
4	IO_L68N_4	AL16		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L91P_4	AV18		
4	IO_L92N_4	AH20		
4	IO_L92P_4	AJ20		
4	IO_L93N_4	AR19		
4	IO_L93P_4	AT18		
4	IO_L94N_4/VREF_4	AW19		
4	IO_L94P_4	AW18		
4	IO_L95N_4/GCLK3S	AL20		
4	IO_L95P_4/GCLK2P	AM20		
4	IO_L96N_4/GCLK1S	AU19		
4	IO_L96P_4/GCLK0P	AT19		
5	IO_L96N_5/GCLK7S	AP21		
5	IO_L96P_5/GCLK6P	AP20		
5	IO_L95N_5/GCLK5S	AN21		
5	IO_L95P_5/GCLK4P	AN22		
5	IO_L94N_5	AU21		
5	IO_L94P_5/VREF_5	AU20		
5	IO_L93N_5	AR21		
5	IO_L93P_5	AR20		
5	IO_L92N_5	AM21		
5	IO_L92P_5	AM22		
5	IO_L91N_5	AW22		
5	IO_L91P_5/VREF_5	AW21		
5	IO_L85N_5	AV22	NC	NC
5	IO_L85P_5	AV21	NC	NC
5	IO_L84N_5	AT22		
5	IO_L84P_5	AT21		
5	IO_L83N_5	AL21		
5	IO_L83P_5	AL22		
5	IO_L82N_5	AW24		
5	IO_L82P_5	AW23		
5	IO_L81N_5/VREF_5	AR23		
5	IO_L81P_5	AR22		
5	IO_L80N_5	AK21		
5	IO_L80P_5	AK22		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L79N_5	AV24		
5	IO_L79P_5	AV23		
5	IO_L78N_5	AP23		
5	IO_L78P_5	AP22		
5	IO_L77N_5	AJ21		
5	IO_L77P_5	AJ22		
5	IO_L76N_5	AU24		
5	IO_L76P_5	AU23		
5	IO_L75N_5/VREF_5	AT25		
5	IO_L75P_5	AT24		
5	IO_L74N_5	AH21		
5	IO_L74P_5	AH22		
5	IO_L73N_5	AW26		
5	IO_L73P_5	AW25		
5	IO_L72N_5	AR25		
5	IO_L72P_5	AR24		
5	IO_L71N_5	AN23		
5	IO_L71P_5	AN24		
5	IO_L70N_5	AU25		
5	IO_L70P_5	AV25		
5	IO_L69N_5/VREF_5	AL24		
5	IO_L69P_5	AL23		
5	IO_L68N_5	AK23		
5	IO_L68P_5	AK24		
5	IO_L67N_5	AU27		
5	IO_L67P_5	AU26		
5	IO_L60N_5	AP25		
5	IO_L60P_5	AP24		
5	IO_L59N_5	AM24		
5	IO_L59P_5	AM25		
5	IO_L58N_5	AW28		
5	IO_L58P_5	AW27		
5	IO_L57N_5/VREF_5	AT27		
5	IO_L57P_5	AT26		
5	IO_L56N_5	AH23		
5	IO_L56P_5	AH24		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L55N_5	AV28		
5	IO_L55P_5	AV27		
5	IO_L54N_5	AP27		
5	IO_L54P_5	AP26		
5	IO_L53N_5	AN25		
5	IO_L53P_5	AN26		
5	IO_L52N_5	AU29		
5	IO_L52P_5	AU28		
5	IO_L51N_5/VREF_5	AR28		
5	IO_L51P_5	AR27		
5	IO_L50N_5	AJ24		
5	IO_L50P_5	AJ25		
5	IO_L49N_5	AW30		
5	IO_L49P_5	AW29		
5	IO_L36N_5	AT29	NC	
5	IO_L36P_5	AT28	NC	
5	IO_L35N_5	AK25	NC	
5	IO_L35P_5	AL26	NC	
5	IO_L34N_5	AV31	NC	
5	IO_L34P_5	AV30	NC	
5	IO_L33N_5/VREF_5	AP29	NC	
5	IO_L33P_5	AP28	NC	
5	IO_L32N_5	AK26	NC	
5	IO_L32P_5	AJ26	NC	
5	IO_L31N_5	AW32	NC	
5	IO_L31P_5	AW31	NC	
5	IO_L30N_5	AM27		
5	IO_L30P_5	AM26		
5	IO_L29N_5	AN28		
5	IO_L29P_5	AN29		
5	IO_L28N_5	AU31		
5	IO_L28P_5	AU30		
5	IO_L27N_5/VREF_5	AT31		
5	IO_L27P_5	AT30		
5	IO_L26N_5	AH25		
5	IO_L26P_5	AH26		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L25N_5	AV33		
5	IO_L25P_5	AV32		
5	IO_L24N_5	AR31		
5	IO_L24P_5	AR30		
5	IO_L23N_5	AL27		
5	IO_L23P_5	AL28		
5	IO_L22N_5	AW34		
5	IO_L22P_5	AW33		
5	IO_L21N_5/VREF_5	AN30		
5	IO_L21P_5	AP30		
5	IO_L20N_5	AM28		
5	IO_L20P_5	AM29		
5	IO_L19N_5	AU33		
5	IO_L19P_5	AU32		
5	IO_L12N_5	AT33	NC	
5	IO_L12P_5	AT32	NC	
5	IO_L11N_5	AK27	NC	
5	IO_L11P_5	AK28	NC	
5	IO_L10N_5	AV35	NC	
5	IO_L10P_5	AV34	NC	
5	IO_L09N_5/VREF_5	AP32	NC	
5	IO_L09P_5	AP31	NC	
5	IO_L08N_5	AL29	NC	
5	IO_L08P_5	AK29	NC	
5	IO_L07N_5	AW36	NC	
5	IO_L07P_5	AW35	NC	
5	IO_L06N_5	AR33		
5	IO_L06P_5	AR32		
5	IO_L05N_5/VRP_5	AM30		
5	IO_L05P_5/VRN_5	AL30		
5	IO_L04N_5	AU35		
5	IO_L04P_5/VREF_5	AU34		
5	IO_L03N_5/D4/ALT_VRP_5	AR34		
5	IO_L03P_5/D5/ALT_VRN_5	AT34		
5	IO_L02N_5/D6	AN31		
5	IO_L02P_5/D7	AM31		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L01N_5/RDWR_B	AU36		
5	IO_L01P_5/CS_B	AV36		
6	IO_L01P_6	AJ27		
6	IO_L01N_6	AH27		
6	IO_L02P_6/VRN_6	AT38		
6	IO_L02N_6/VRP_6	AR37		
6	IO_L03P_6	AP36		
6	IO_L03N_6/VREF_6	AR36		
6	IO_L04P_6	AJ28		
6	IO_L04N_6	AH29		
6	IO_L05P_6	AT39		
6	IO_L05N_6	AR39		
6	IO_L06P_6	AN34		
6	IO_L06N_6	AP35		
6	IO_L07P_6	AH28	NC	
6	IO_L07N_6	AG28	NC	
6	IO_L08P_6	AR38	NC	
6	IO_L08N_6	AP38	NC	
6	IO_L09P_6	AM34	NC	
6	IO_L09N_6/VREF_6	AM33	NC	
6	IO_L10P_6	AL32	NC	
6	IO_L10N_6	AK32	NC	
6	IO_L11P_6	AP37	NC	
6	IO_L11N_6	AN37	NC	
6	IO_L12P_6	AM35	NC	
6	IO_L12N_6	AN35	NC	
6	IO_L19P_6	AK31		
6	IO_L19N_6	AJ30		
6	IO_L20P_6	AP39		
6	IO_L20N_6	AN39		
6	IO_L21P_6	AK33		
6	IO_L21N_6/VREF_6	AL33		
6	IO_L22P_6	AJ31		
6	IO_L22N_6	AH31		
6	IO_L23P_6	AN38		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L23N_6	AM38		
6	IO_L24P_6	AM36		
6	IO_L24N_6	AN36		
6	IO_L25P_6	AH30		
6	IO_L25N_6	AG30		
6	IO_L26P_6	AM37		
6	IO_L26N_6	AL37		
6	IO_L27P_6	AK34		
6	IO_L27N_6/VREF_6	AL34		
6	IO_L28P_6	AG29		
6	IO_L28N_6	AF29		
6	IO_L29P_6	AL35		
6	IO_L29N_6	AK35		
6	IO_L30P_6	AH33		
6	IO_L30N_6	AJ33		
6	IO_L31P_6	AJ32	NC	
6	IO_L31N_6	AH32	NC	
6	IO_L32P_6	AM39	NC	
6	IO_L32N_6	AL39	NC	
6	IO_L33P_6	AK36	NC	
6	IO_L33N_6/VREF_6	AL36	NC	
6	IO_L34P_6	AF28	NC	
6	IO_L34N_6	AE28	NC	
6	IO_L35P_6	AL38	NC	
6	IO_L35N_6	AK38	NC	
6	IO_L36P_6	AH34	NC	
6	IO_L36N_6	AJ34	NC	
6	IO_L43P_6	AG31		
6	IO_L43N_6	AF31		
6	IO_L44P_6	AK37		
6	IO_L44N_6	AJ37		
6	IO_L45P_6	AH36		
6	IO_L45N_6/VREF_6	AJ36		
6	IO_L46P_6	AF30		
6	IO_L46N_6	AE30		
6	IO_L47P_6	AK39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L47N_6	AJ39		
6	IO_L48P_6	AG35		
6	IO_L48N_6	AH35		
6	IO_L49P_6	AG32		
6	IO_L49N_6	AF32		
6	IO_L50P_6	AH37		
6	IO_L50N_6	AG37		
6	IO_L51P_6	AD29		
6	IO_L51N_6/VREF_6	AE29		
6	IO_L52P_6	AD28		
6	IO_L52N_6	AC28		
6	IO_L53P_6	AH38		
6	IO_L53N_6	AG38		
6	IO_L54P_6	AF34		
6	IO_L54N_6	AG34		
6	IO_L55P_6	AE32		
6	IO_L55N_6	AD32		
6	IO_L56P_6	AH39		
6	IO_L56N_6	AG39		
6	IO_L57P_6	AE33		
6	IO_L57N_6/VREF_6	AF33		
6	IO_L58P_6	AD30		
6	IO_L58N_6	AC30		
6	IO_L59P_6	AF37		
6	IO_L59N_6	AE37		
6	IO_L60P_6	AF36		
6	IO_L60N_6	AG36		
6	IO_L67P_6	AD31		
6	IO_L67N_6	AC31		
6	IO_L68P_6	AE34		
6	IO_L68N_6	AD34		
6	IO_L69P_6	AD35		
6	IO_L69N_6/VREF_6	AE35		
6	IO_L70P_6	AB28		
6	IO_L70N_6	AA28		
6	IO_L71P_6	AF39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L71N_6	AE39		
6	IO_L72P_6	AD36		
6	IO_L72N_6	AE36		
6	IO_L73P_6	AB29		
6	IO_L73N_6	AA29		
6	IO_L74P_6	AE38		
6	IO_L74N_6	AD38		
6	IO_L75P_6	AC33		
6	IO_L75N_6/VREF_6	AD33		
6	IO_L76P_6	AB30		
6	IO_L76N_6	AA30		
6	IO_L77P_6	AD37		
6	IO_L77N_6	AC37		
6	IO_L78P_6	AB34		
6	IO_L78N_6	AC34		
6	IO_L79P_6	AB31		
6	IO_L79N_6	AA31		
6	IO_L80P_6	AD39		
6	IO_L80N_6	AC39		
6	IO_L81P_6	AB35		
6	IO_L81N_6/VREF_6	AC35		
6	IO_L82P_6	AB32		
6	IO_L82N_6	AA32		
6	IO_L83P_6	AC38		
6	IO_L83N_6	AB38		
6	IO_L84P_6	AA33		
6	IO_L84N_6	AB33		
6	IO_L91P_6	Y28		
6	IO_L91N_6	Y29		
6	IO_L92P_6	AB39		
6	IO_L92N_6	AA39		
6	IO_L93P_6	AA36		
6	IO_L93N_6/VREF_6	AB36		
6	IO_L94P_6	Y31		
6	IO_L94N_6	Y32		
6	IO_L95P_6	AA37		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L95N_6	AA38		
6	IO_L96P_6	AA35		
6	IO_L96N_6	AA34		
7	IO_L96P_7	W34		
7	IO_L96N_7	Y34		
7	IO_L95P_7	W32		
7	IO_L95N_7	V32		
7	IO_L94P_7	W37		
7	IO_L94N_7	Y37		
7	IO_L93P_7/VREF_7	W35		
7	IO_L93N_7	Y35		
7	IO_L92P_7	W31		
7	IO_L92N_7	V31		
7	IO_L91P_7	V39		
7	IO_L91N_7	W39		
7	IO_L84P_7	V36		
7	IO_L84N_7	W36		
7	IO_L83P_7	W30		
7	IO_L83N_7	V30		
7	IO_L82P_7	V38		
7	IO_L82N_7	W38		
7	IO_L81P_7/VREF_7	V33		
7	IO_L81N_7	W33		
7	IO_L80P_7	W29		
7	IO_L80N_7	V29		
7	IO_L79P_7	T39		
7	IO_L79N_7	U39		
7	IO_L78P_7	U35		
7	IO_L78N_7	V35		
7	IO_L77P_7	W28		
7	IO_L77N_7	V28		
7	IO_L76P_7	U37		
7	IO_L76N_7	U38		
7	IO_L75P_7/VREF_7	U34		
7	IO_L75N_7	V34		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L74P_7	U31		
7	IO_L74N_7	T31		
7	IO_L73P_7	R38		
7	IO_L73N_7	T38		
7	IO_L72P_7	T33		
7	IO_L72N_7	U33		
7	IO_L71P_7	U30		
7	IO_L71N_7	T30		
7	IO_L70P_7	R37		
7	IO_L70N_7	T37		
7	IO_L69P_7/VREF_7	R36		
7	IO_L69N_7	T36		
7	IO_L68P_7	T32		
7	IO_L68N_7	R32		
7	IO_L67P_7	P39		
7	IO_L67N_7	R39		
7	IO_L60P_7	R35		
7	IO_L60N_7	T35		
7	IO_L59P_7	U28		
7	IO_L59N_7	T28		
7	IO_L58P_7	N37		
7	IO_L58N_7	P37		
7	IO_L57P_7/VREF_7	R34		
7	IO_L57N_7	T34		
7	IO_L56P_7	T29		
7	IO_L56N_7	R29		
7	IO_L55P_7	M39		
7	IO_L55N_7	N39		
7	IO_L54P_7	N36		
7	IO_L54N_7	P36		
7	IO_L53P_7	R30		
7	IO_L53N_7	P30		
7	IO_L52P_7	M38		
7	IO_L52N_7	N38		
7	IO_L51P_7/VREF_7	P33		
7	IO_L51N_7	R33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L50P_7	P32		
7	IO_L50N_7	N32		
7	IO_L49P_7	L37		
7	IO_L49N_7	M37		
7	IO_L48P_7	N34		
7	IO_L48N_7	P34		
7	IO_L47P_7	P31		
7	IO_L47N_7	N31		
7	IO_L46P_7	M35		
7	IO_L46N_7	N35		
7	IO_L45P_7/VREF_7	L36		
7	IO_L45N_7	M36		
7	IO_L44P_7	R28		
7	IO_L44N_7	P28		
7	IO_L43P_7	K39		
7	IO_L43N_7	L39		
7	IO_L36P_7	L34	NC	
7	IO_L36N_7	M34	NC	
7	IO_L35P_7	P29	NC	
7	IO_L35N_7	N29	NC	
7	IO_L34P_7	J38	NC	
7	IO_L34N_7	K38	NC	
7	IO_L33P_7/VREF_7	L33	NC	
7	IO_L33N_7	M33	NC	
7	IO_L32P_7	M32	NC	
7	IO_L32N_7	L32	NC	
7	IO_L31P_7	H39	NC	
7	IO_L31N_7	J39	NC	
7	IO_L30P_7	J36		
7	IO_L30N_7	K36		
7	IO_L29P_7	N30		
7	IO_L29N_7	M30		
7	IO_L28P_7	J37		
7	IO_L28N_7	K37		
7	IO_L27P_7/VREF_7	J35		
7	IO_L27N_7	K35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L26P_7	M31		
7	IO_L26N_7	L31		
7	IO_L25P_7	G38		
7	IO_L25N_7	H38		
7	IO_L24P_7	J34		
7	IO_L24N_7	K34		
7	IO_L23P_7	K32		
7	IO_L23N_7	K31		
7	IO_L22P_7	F39		
7	IO_L22N_7	G39		
7	IO_L21P_7/VREF_7	G36		
7	IO_L21N_7	H36		
7	IO_L20P_7	N28		
7	IO_L20N_7	M28		
7	IO_L19P_7	G37		
7	IO_L19N_7	H37		
7	IO_L12P_7	J33	NC	
7	IO_L12N_7	K33	NC	
7	IO_L11P_7	M29	NC	
7	IO_L11N_7	L28	NC	
7	IO_L10P_7	E38	NC	
7	IO_L10N_7	F38	NC	
7	IO_L09P_7/VREF_7	G35	NC	
7	IO_L09N_7	H35	NC	
7	IO_L08P_7	L30	NC	
7	IO_L08N_7	K29	NC	
7	IO_L07P_7	D39	NC	
7	IO_L07N_7	E39	NC	
7	IO_L06P_7	G34		
7	IO_L06N_7	H34		
7	IO_L05P_7	J32		
7	IO_L05N_7	H33		
7	IO_L04P_7	F36		
7	IO_L04N_7	F37		
7	IO_L03P_7/VREF_7	E36		
7	IO_L03N_7	F35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L02P_7/VRN_7	M27		
7	IO_L02N_7/VRP_7	L27		
7	IO_L01P_7	D38		
7	IO_L01N_7	E37		
0	VCCO_0	P25		
0	VCCO_0	P24		
0	VCCO_0	P23		
0	VCCO_0	P22		
0	VCCO_0	P21		
0	VCCO_0	N26		
0	VCCO_0	N25		
0	VCCO_0	N24		
0	VCCO_0	N23		
0	VCCO_0	N22		
0	VCCO_0	N21		
0	VCCO_0	L23		
0	VCCO_0	J25		
0	VCCO_0	G27		
0	VCCO_0	E29		
0	VCCO_0	C22		
0	VCCO_0	B26		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	P16		
1	VCCO_1	P15		
1	VCCO_1	N19		
1	VCCO_1	N18		
1	VCCO_1	N17		
1	VCCO_1	N16		
1	VCCO_1	N15		
1	VCCO_1	N14		
1	VCCO_1	L17		
1	VCCO_1	J15		
1	VCCO_1	G13		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	VCCO_1	E11		
1	VCCO_1	C18		
1	VCCO_1	B14		
2	VCCO_2	W14		
2	VCCO_2	W13		
2	VCCO_2	V14		
2	VCCO_2	V13		
2	VCCO_2	V3		
2	VCCO_2	U14		
2	VCCO_2	U13		
2	VCCO_2	U11		
2	VCCO_2	T14		
2	VCCO_2	T13		
2	VCCO_2	R14		
2	VCCO_2	R13		
2	VCCO_2	R9		
2	VCCO_2	P13		
2	VCCO_2	P2		
2	VCCO_2	N7		
2	VCCO_2	L5		
3	VCCO_3	AJ5		
3	VCCO_3	AG7		
3	VCCO_3	AF13		
3	VCCO_3	AF2		
3	VCCO_3	AE14		
3	VCCO_3	AE13		
3	VCCO_3	AE9		
3	VCCO_3	AD14		
3	VCCO_3	AD13		
3	VCCO_3	AC14		
3	VCCO_3	AC13		
3	VCCO_3	AC11		
3	VCCO_3	AB14		
3	VCCO_3	AB13		
3	VCCO_3	AB3		
3	VCCO_3	AA14		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	VCCO_3	AA13		
4	VCCO_4	AV14		
4	VCCO_4	AU18		
4	VCCO_4	AR11		
4	VCCO_4	AN13		
4	VCCO_4	AL15		
4	VCCO_4	AJ17		
4	VCCO_4	AG19		
4	VCCO_4	AG18		
4	VCCO_4	AG17		
4	VCCO_4	AG16		
4	VCCO_4	AG15		
4	VCCO_4	AG14		
4	VCCO_4	AF19		
4	VCCO_4	AF18		
4	VCCO_4	AF17		
4	VCCO_4	AF16		
4	VCCO_4	AF15		
5	VCCO_5	AV26		
5	VCCO_5	AU22		
5	VCCO_5	AR29		
5	VCCO_5	AN27		
5	VCCO_5	AL25		
5	VCCO_5	AJ23		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AG24		
5	VCCO_5	AG23		
5	VCCO_5	AG22		
5	VCCO_5	AG21		
5	VCCO_5	AF25		
5	VCCO_5	AF24		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
6	VCCO_6	AJ35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	DONE	AP7		
NA	M0	AN32		
NA	M1	AP33		
NA	M2	AT35		
NA	HSWAP_EN	E34		
NA	TCK	G8		
NA	TDI	D35		
NA	TDO	E6		
NA	TMS	F7		
NA	PWRDWN_B	AN8		
NA	DXN	G32		
NA	DXP	F33		
NA	VBATT	D5		
NA	RSVD	H9		
NA	VCCAUX	AV20		
NA	VCCAUX	AT37		
NA	VCCAUX	AT3		
NA	VCCAUX	Y38		
NA	VCCAUX	Y2		
NA	VCCAUX	D37		
NA	VCCAUX	D3		
NA	VCCAUX	B20		
NA	VCCINT	AG27		
NA	VCCINT	AG20		
NA	VCCINT	AG13		
NA	VCCINT	AF26		
NA	VCCINT	AF20		
NA	VCCINT	AF14		
NA	VCCINT	AE25		
NA	VCCINT	AE24		
NA	VCCINT	AE23		
NA	VCCINT	AE22		
NA	VCCINT	AE21		
NA	VCCINT	AE20		
NA	VCCINT	AE19		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	AE18		
NA	VCCINT	AE17		
NA	VCCINT	AE16		
NA	VCCINT	AE15		
NA	VCCINT	AD25		
NA	VCCINT	AD24		
NA	VCCINT	AD16		
NA	VCCINT	AD15		
NA	VCCINT	AC25		
NA	VCCINT	AC15		
NA	VCCINT	AB25		
NA	VCCINT	AB15		
NA	VCCINT	AA25		
NA	VCCINT	AA15		
NA	VCCINT	Y27		
NA	VCCINT	Y26		
NA	VCCINT	Y25		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	W25		
NA	VCCINT	W15		
NA	VCCINT	V25		
NA	VCCINT	V15		
NA	VCCINT	U25		
NA	VCCINT	U15		
NA	VCCINT	T25		
NA	VCCINT	T24		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	R25		
NA	VCCINT	R24		
NA	VCCINT	R23		
NA	VCCINT	R22		
NA	VCCINT	R21		
NA	VCCINT	R20		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	R19		
NA	VCCINT	R18		
NA	VCCINT	R17		
NA	VCCINT	R16		
NA	VCCINT	R15		
NA	VCCINT	P26		
NA	VCCINT	P20		
NA	VCCINT	P14		
NA	VCCINT	N27		
NA	VCCINT	N20		
NA	VCCINT	N13		
NA	GND	AW38		
NA	GND	AW37		
NA	GND	AW20		
NA	GND	AW3		
NA	GND	AW2		
NA	GND	AV39		
NA	GND	AV38		
NA	GND	AV37		
NA	GND	AV29		
NA	GND	AV11		
NA	GND	AV3		
NA	GND	AV2		
NA	GND	AV1		
NA	GND	AU39		
NA	GND	AU38		
NA	GND	AU37		
NA	GND	AU3		
NA	GND	AU2		
NA	GND	AU1		
NA	GND	AT36		
NA	GND	AT23		
NA	GND	AT20		
NA	GND	AT17		
NA	GND	AT4		
NA	GND	AR35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AC20		
NA	GND	AC19		
NA	GND	AC18		
NA	GND	AC17		
NA	GND	AC16		
NA	GND	AC8		
NA	GND	AC4		
NA	GND	AB24		
NA	GND	AB23		
NA	GND	AB22		
NA	GND	AB21		
NA	GND	AB20		
NA	GND	AB19		
NA	GND	AB18		
NA	GND	AB17		
NA	GND	AB16		
NA	GND	AA24		
NA	GND	AA23		
NA	GND	AA22		
NA	GND	AA21		
NA	GND	AA20		
NA	GND	AA19		
NA	GND	AA18		
NA	GND	AA17		
NA	GND	AA16		
NA	GND	Y39		
NA	GND	Y36		
NA	GND	Y33		
NA	GND	Y30		
NA	GND	Y24		
NA	GND	Y23		
NA	GND	Y22		
NA	GND	Y21		
NA	GND	Y20		
NA	GND	Y19		
NA	GND	Y18		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		

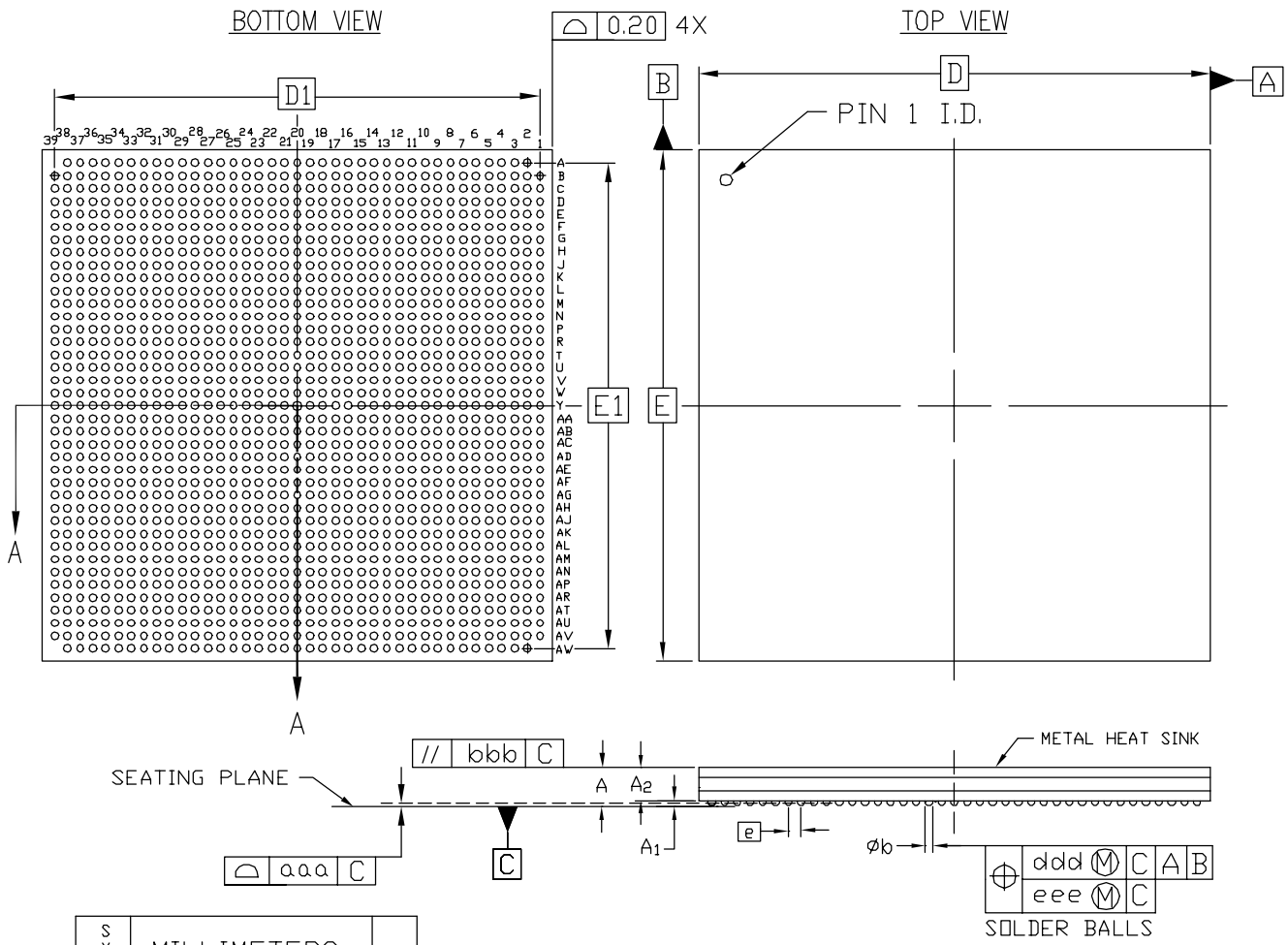
Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	U4		
NA	GND	T23		
NA	GND	T22		
NA	GND	T21		
NA	GND	T20		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	P35		
NA	GND	P5		
NA	GND	L38		
NA	GND	L29		
NA	GND	L11		
NA	GND	L2		
NA	GND	K30		
NA	GND	K20		
NA	GND	K10		
NA	GND	J31		
NA	GND	J9		
NA	GND	H32		
NA	GND	H23		
NA	GND	H17		
NA	GND	H8		
NA	GND	G33		
NA	GND	G20		
NA	GND	G7		
NA	GND	F34		
NA	GND	F6		
NA	GND	E35		
NA	GND	E26		
NA	GND	E14		
NA	GND	E5		
NA	GND	D36		
NA	GND	D23		
NA	GND	D20		
NA	GND	D17		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	40.00 BASIC			
D_1/E_1	38.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		39		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 9: **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**

BF957 Flip-Chip BGA Package

As shown in Table 14, XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000 Virtex-II devices are available in the BF957 package. Pins in each of these devices are the same, except for the pin differences in the XC2V2000 device shown in the No Connect column. Following this table are the **BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)**.

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L01N_0	H23	
0	IO_L01P_0	H22	
0	IO_L02N_0	G24	
0	IO_L02P_0	E25	
0	IO_L03N_0/VRP_0	B29	
0	IO_L03P_0/VRN_0	C27	
0	IO_L04N_0/VREF_0	F24	
0	IO_L04P_0	F23	
0	IO_L05N_0	D26	
0	IO_L05P_0	D25	
0	IO_L06N_0	A28	
0	IO_L06P_0	A27	
0	IO_L19N_0	J22	
0	IO_L19P_0	J21	
0	IO_L20N_0	G23	
0	IO_L20P_0	G22	
0	IO_L21N_0	B27	
0	IO_L21P_0/VREF_0	B26	
0	IO_L22N_0	K20	
0	IO_L22P_0	K19	
0	IO_L23N_0	C26	
0	IO_L23P_0	C24	
0	IO_L24N_0	D24	
0	IO_L24P_0	D23	
0	IO_L25N_0	E24	NC
0	IO_L25P_0	E23	NC
0	IO_L26N_0	G21	NC
0	IO_L26P_0	G20	NC
0	IO_L27N_0	A26	NC
0	IO_L27P_0/VREF_0	A25	NC
0	IO_L29N_0	H21	NC
0	IO_L29P_0	H20	NC
0	IO_L30N_0	B25	NC

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L30P_0	B23	NC
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L91P_0	J18	
0	IO_L92N_0	F17	
0	IO_L92P_0	F16	
0	IO_L93N_0	B18	
0	IO_L93P_0	B17	
0	IO_L94N_0/VREF_0	J17	
0	IO_L94P_0	J16	
0	IO_L95N_0/GCLK7P	E17	
0	IO_L95P_0/GCLK6S	E16	
0	IO_L96N_0/GCLK5P	A18	
0	IO_L96P_0/GCLK4S	A17	
1	IO_L96N_1/GCLK3P	C16	
1	IO_L96P_1/GCLK2S	C15	
1	IO_L95N_1/GCLK1P	H16	
1	IO_L95P_1/GCLK0S	H15	
1	IO_L94N_1	A15	
1	IO_L94P_1/VREF_1	A14	
1	IO_L93N_1	F15	
1	IO_L93P_1	F14	
1	IO_L92N_1	G15	
1	IO_L92P_1	G14	
1	IO_L91N_1	B15	
1	IO_L91P_1/VREF_1	B14	
1	IO_L78N_1	D15	
1	IO_L78P_1	E15	
1	IO_L77N_1	J15	
1	IO_L77P_1	K14	
1	IO_L76N_1	D14	
1	IO_L76P_1	D13	
1	IO_L75N_1/VREF_1	E14	
1	IO_L75P_1	E13	
1	IO_L74N_1	A13	
1	IO_L74P_1	A12	
1	IO_L73N_1	F13	
1	IO_L73P_1	F12	
1	IO_L72N_1	J14	
1	IO_L72P_1	J13	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L71N_1	B13	
1	IO_L71P_1	B12	
1	IO_L70N_1	C13	
1	IO_L70P_1	C12	
1	IO_L69N_1/VREF_1	H13	
1	IO_L69P_1	H12	
1	IO_L68N_1	D12	
1	IO_L68P_1	D11	
1	IO_L67N_1	B11	
1	IO_L67P_1	B10	
1	IO_L54N_1	E12	
1	IO_L54P_1	E11	
1	IO_L53N_1	A11	
1	IO_L53P_1	A10	
1	IO_L52N_1	G12	
1	IO_L52P_1	G11	
1	IO_L51N_1/VREF_1	K13	
1	IO_L51P_1	K12	
1	IO_L50N_1	C11	
1	IO_L50P_1	C10	
1	IO_L49N_1	B9	
1	IO_L49P_1	B7	
1	IO_L30N_1	F11	NC
1	IO_L30P_1	F9	NC
1	IO_L29N_1	A9	NC
1	IO_L29P_1	A8	NC
1	IO_L27N_1/VREF_1	D9	NC
1	IO_L27P_1	D8	NC
1	IO_L26N_1	J12	NC
1	IO_L26P_1	J11	NC
1	IO_L25N_1	C9	NC
1	IO_L25P_1	C8	NC
1	IO_L24N_1	E10	
1	IO_L24P_1	E9	
1	IO_L23N_1	H11	
1	IO_L23P_1	H10	
1	IO_L22N_1	A7	
1	IO_L22P_1	A6	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L21N_1/VREF_1	A5	
1	IO_L21P_1	A4	
1	IO_L20N_1	G10	
1	IO_L20P_1	G9	
1	IO_L19N_1	B6	
1	IO_L19P_1	C5	
1	IO_L06N_1	C6	
1	IO_L06P_1	D6	
1	IO_L05N_1	H9	
1	IO_L05P_1	G8	
1	IO_L04N_1	D7	
1	IO_L04P_1/VREF_1	E6	
1	IO_L03N_1/VRP_1	E8	
1	IO_L03P_1/VRN_1	E7	
1	IO_L02N_1	F8	
1	IO_L02P_1	F7	
1	IO_L01N_1	B5	
1	IO_L01P_1	B3	
2	IO_L01N_2	F5	
2	IO_L01P_2	G4	
2	IO_L02N_2/VRP_2	G6	
2	IO_L02P_2/VRN_2	H6	
2	IO_L03N_2	D3	
2	IO_L03P_2/VREF_2	E4	
2	IO_L04N_2	K10	
2	IO_L04P_2	K9	
2	IO_L05N_2	D2	
2	IO_L05P_2	E3	
2	IO_L06N_2	F4	
2	IO_L06P_2	F3	
2	IO_L19N_2	L10	
2	IO_L19P_2	M10	
2	IO_L20N_2	H7	
2	IO_L20P_2	J8	
2	IO_L21N_2	D1	
2	IO_L21P_2/VREF_2	E1	
2	IO_L22N_2	G5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L22P_2	H5	
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L69P_2/VREF_2	M4	
2	IO_L70N_2	K1	
2	IO_L70P_2	L1	
2	IO_L71N_2	N9	
2	IO_L71P_2	P9	
2	IO_L72N_2	N5	
2	IO_L72P_2	P5	
2	IO_L73N_2	M3	
2	IO_L73P_2	N3	
2	IO_L74N_2	R8	
2	IO_L74P_2	R9	
2	IO_L75N_2	M2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	M1	
2	IO_L76P_2	N1	
2	IO_L77N_2	P7	
2	IO_L77P_2	R7	
2	IO_L78N_2	N4	
2	IO_L78P_2	P4	
2	IO_L91N_2	T8	
2	IO_L91P_2	T9	
2	IO_L92N_2	P6	
2	IO_L92P_2	R6	
2	IO_L93N_2	P2	
2	IO_L93P_2/VREF_2	R2	
2	IO_L94N_2	R5	
2	IO_L94P_2	T5	
2	IO_L95N_2	P1	
2	IO_L95P_2	R1	
2	IO_L96N_2	R4	
2	IO_L96P_2	R3	
3	IO_L96N_3	T6	
3	IO_L96P_3	U5	
3	IO_L95N_3	U6	
3	IO_L95P_3	V6	
3	IO_L94N_3	T3	
3	IO_L94P_3	U3	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L93N_3/VREF_3	U1	
3	IO_L93P_3	V1	
3	IO_L92N_3	U8	
3	IO_L92P_3	W8	
3	IO_L91N_3	U2	
3	IO_L91P_3	V2	
3	IO_L78N_3	U7	
3	IO_L78P_3	V7	
3	IO_L77N_3	U4	
3	IO_L77P_3	V4	
3	IO_L76N_3	W1	
3	IO_L76P_3	Y1	
3	IO_L75N_3/VREF_3	V5	
3	IO_L75P_3	W5	
3	IO_L74N_3	W2	
3	IO_L74P_3	Y2	
3	IO_L73N_3	W6	
3	IO_L73P_3	Y6	
3	IO_L72N_3	Y5	
3	IO_L72P_3	AA5	
3	IO_L71N_3	W3	
3	IO_L71P_3	Y3	
3	IO_L70N_3	W4	
3	IO_L70P_3	Y4	
3	IO_L69N_3/VREF_3	U9	
3	IO_L69P_3	V9	
3	IO_L68N_3	AA1	
3	IO_L68P_3	AB1	
3	IO_L67N_3	Y7	
3	IO_L67P_3	AA7	
3	IO_L54N_3	AA6	
3	IO_L54P_3	AC6	
3	IO_L53N_3	AA2	
3	IO_L53P_3	AB2	
3	IO_L52N_3	AA4	
3	IO_L52P_3	AC4	
3	IO_L51N_3/VREF_3	V10	
3	IO_L51P_3	W10	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L50N_3	AA3	
3	IO_L50P_3	AB3	
3	IO_L49N_3	AB5	
3	IO_L49P_3	AC5	
3	IO_L48N_3	W9	
3	IO_L48P_3	Y9	
3	IO_L47N_3	AC1	
3	IO_L47P_3	AD1	
3	IO_L46N_3	AC3	
3	IO_L46P_3	AD3	
3	IO_L45N_3/VREF_3	Y8	
3	IO_L45P_3	AA8	
3	IO_L44N_3	AC2	
3	IO_L44P_3	AE2	
3	IO_L43N_3	AB7	
3	IO_L43P_3	AC7	
3	IO_L27N_3/VREF_3	Y10	NC
3	IO_L27P_3	AA10	NC
3	IO_L25N_3	AE1	NC
3	IO_L25P_3	AF1	NC
3	IO_L24N_3	AF2	
3	IO_L24P_3	AG2	
3	IO_L23N_3	AA9	
3	IO_L23P_3	AB9	
3	IO_L22N_3	AD4	
3	IO_L22P_3	AE4	
3	IO_L21N_3/VREF_3	AD5	
3	IO_L21P_3	AE5	
3	IO_L20N_3	AB8	
3	IO_L20P_3	AC8	
3	IO_L19N_3	AG1	
3	IO_L19P_3	AH1	
3	IO_L06N_3	AF4	
3	IO_L06P_3	AG4	
3	IO_L05N_3	AB10	
3	IO_L05P_3	AB11	
3	IO_L04N_3	AF3	
3	IO_L04P_3	AG3	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L03N_3/VREF_3	AD6	
3	IO_L03P_3	AD7	
3	IO_L02N_3/VRP_3	AE6	
3	IO_L02P_3/VRN_3	AF5	
3	IO_L01N_3	AH2	
3	IO_L01P_3	AH3	
4	IO_L01N_4/DOUT	AD9	
4	IO_L01P_4/INIT_B	AD10	
4	IO_L02N_4/D0	AF7	
4	IO_L02P_4/D1	AG7	
4	IO_L03N_4/D2/ALT_VRP_4	AK3	
4	IO_L03P_4/D3/ALT_VRN_4	AJ5	
4	IO_L04N_4/VREF_4	AE8	
4	IO_L04P_4	AF8	
4	IO_L05N_4/VRP_4	AK4	
4	IO_L05P_4/VRN_4	AK5	
4	IO_L06N_4	AH6	
4	IO_L06P_4	AH7	
4	IO_L19N_4	AC10	
4	IO_L19P_4	AC11	
4	IO_L20N_4	AE9	
4	IO_L20P_4	AE10	
4	IO_L21N_4	AL4	
4	IO_L21P_4/VREF_4	AL5	
4	IO_L22N_4	AB12	
4	IO_L22P_4	AB13	
4	IO_L23N_4	AJ6	
4	IO_L23P_4	AJ8	
4	IO_L24N_4	AK6	
4	IO_L24P_4	AK7	
4	IO_L25N_4	AG8	NC
4	IO_L25P_4	AG9	NC
4	IO_L26N_4	AF9	NC
4	IO_L26P_4	AF11	NC
4	IO_L27N_4	AH8	NC
4	IO_L27P_4/VREF_4	AH9	NC
4	IO_L28N_4	AD11	NC

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L28P_4	AD12	NC
4	IO_L29N_4	AL6	NC
4	IO_L29P_4	AL7	NC
4	IO_L30N_4	AJ9	NC
4	IO_L30P_4	AJ10	NC
4	IO_L49N_4	AE11	
4	IO_L49P_4	AE12	
4	IO_L50N_4	AG10	
4	IO_L50P_4	AG11	
4	IO_L51N_4	AL8	
4	IO_L51P_4/VREF_4	AL9	
4	IO_L52N_4	AF12	
4	IO_L52P_4	AF13	
4	IO_L53N_4	AK9	
4	IO_L53P_4	AK10	
4	IO_L54N_4	AH11	
4	IO_L54P_4	AH12	
4	IO_L67N_4	AC12	
4	IO_L67P_4	AC13	
4	IO_L68N_4	AG12	
4	IO_L68P_4	AG13	
4	IO_L69N_4	AL10	
4	IO_L69P_4/VREF_4	AL11	
4	IO_L70N_4	AD13	
4	IO_L70P_4	AD15	
4	IO_L71N_4	AJ11	
4	IO_L71P_4	AJ12	
4	IO_L72N_4	AK11	
4	IO_L72P_4	AK12	
4	IO_L73N_4	AE14	
4	IO_L73P_4	AE15	
4	IO_L74N_4	AF14	
4	IO_L74P_4	AF15	
4	IO_L75N_4	AL12	
4	IO_L75P_4/VREF_4	AL13	
4	IO_L76N_4	AB14	
4	IO_L76P_4	AC14	
4	IO_L77N_4	AH13	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L77P_4	AH14	
4	IO_L78N_4	AJ13	
4	IO_L78P_4	AK13	
4	IO_L91N_4/VREF_4	AC15	
4	IO_L91P_4	AC16	
4	IO_L92N_4	AG14	
4	IO_L92P_4	AG15	
4	IO_L93N_4	AK14	
4	IO_L93P_4	AK15	
4	IO_L94N_4/VREF_4	AF16	
4	IO_L94P_4	AG16	
4	IO_L95N_4/GCLK3S	AL14	
4	IO_L95P_4/GCLK2P	AL15	
4	IO_L96N_4/GCLK1S	AH15	
4	IO_L96P_4/GCLK0P	AJ15	
5	IO_L96N_5/GCLK7S	AJ16	
5	IO_L96P_5/GCLK6P	AH17	
5	IO_L95N_5/GCLK5S	AD16	
5	IO_L95P_5/GCLK4P	AD17	
5	IO_L94N_5	AL17	
5	IO_L94P_5/VREF_5	AL18	
5	IO_L93N_5	AG17	
5	IO_L93P_5	AF17	
5	IO_L92N_5	AE17	
5	IO_L92P_5	AE18	
5	IO_L91N_5	AK17	
5	IO_L91P_5/VREF_5	AJ17	
5	IO_L78N_5	AK18	
5	IO_L78P_5	AK19	
5	IO_L77N_5	AC17	
5	IO_L77P_5	AB18	
5	IO_L76N_5	AH18	
5	IO_L76P_5	AH19	
5	IO_L75N_5/VREF_5	AL19	
5	IO_L75P_5	AL20	
5	IO_L74N_5	AC18	
5	IO_L74P_5	AC19	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L73N_5	AJ19	
5	IO_L73P_5	AJ20	
5	IO_L72N_5	AG18	
5	IO_L72P_5	AG19	
5	IO_L71N_5	AF18	
5	IO_L71P_5	AF19	
5	IO_L70N_5	AK20	
5	IO_L70P_5	AK21	
5	IO_L69N_5/VREF_5	AH20	
5	IO_L69P_5	AH21	
5	IO_L68N_5	AD19	
5	IO_L68P_5	AD20	
5	IO_L67N_5	AL21	
5	IO_L67P_5	AL22	
5	IO_L54N_5	AG20	
5	IO_L54P_5	AG21	
5	IO_L53N_5	AB19	
5	IO_L53P_5	AB20	
5	IO_L52N_5	AJ21	
5	IO_L52P_5	AJ22	
5	IO_L51N_5/VREF_5	AF20	
5	IO_L51P_5	AF21	
5	IO_L50N_5	AE20	
5	IO_L50P_5	AE21	
5	IO_L49N_5	AK22	
5	IO_L49P_5	AK23	
5	IO_L30N_5	AJ23	NC
5	IO_L30P_5	AJ24	NC
5	IO_L29N_5	AC20	NC
5	IO_L29P_5	AC21	NC
5	IO_L28N_5	AL23	NC
5	IO_L28P_5	AL24	NC
5	IO_L27N_5/VREF_5	AL25	NC
5	IO_L27P_5	AL26	NC
5	IO_L26N_5	AD21	NC
5	IO_L26P_5	AD22	NC
5	IO_L25N_5	AH23	NC
5	IO_L25P_5	AH24	NC

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	IO_L24N_5	AG22	
5	IO_L24P_5	AG23	
5	IO_L23N_5	AE22	
5	IO_L23P_5	AE23	
5	IO_L22N_5	AK25	
5	IO_L22P_5	AK26	
5	IO_L21N_5/VREF_5	AH25	
5	IO_L21P_5	AG25	
5	IO_L20N_5	AB21	
5	IO_L20P_5	AC22	
5	IO_L19N_5	AL27	
5	IO_L19P_5	AL28	
5	IO_L06N_5	AK27	
5	IO_L06P_5	AJ27	
5	IO_L05N_5/VRP_5	AD23	
5	IO_L05P_5/VRN_5	AE24	
5	IO_L04N_5	AJ26	
5	IO_L04P_5/VREF_5	AH26	
5	IO_L03N_5/D4/ALT_VRP_5	AF23	
5	IO_L03P_5/D5/ALT_VRN_5	AF24	
5	IO_L02N_5/D6	AG24	
5	IO_L02P_5/D7	AF25	
5	IO_L01N_5/RDWR_B	AK28	
5	IO_L01P_5/CS_B	AK29	
6	IO_L01P_6	AF27	
6	IO_L01N_6	AF28	
6	IO_L02P_6/VRN_6	AE26	
6	IO_L02N_6/VRP_6	AE27	
6	IO_L03P_6	AH29	
6	IO_L03N_6/VREF_6	AH30	
6	IO_L04P_6	AB22	
6	IO_L04N_6	AB23	
6	IO_L05P_6	AG28	
6	IO_L05N_6	AG29	
6	IO_L06P_6	AH31	
6	IO_L06N_6	AG31	
6	IO_L19P_6	AA22	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L19N_6	Y22	
6	IO_L20P_6	AD25	
6	IO_L20N_6	AC24	
6	IO_L21P_6	AG30	
6	IO_L21N_6/VREF_6	AF30	
6	IO_L22P_6	AD26	
6	IO_L22N_6	AC26	
6	IO_L23P_6	AF29	
6	IO_L23N_6	AD29	
6	IO_L24P_6	AE28	
6	IO_L24N_6	AD28	
6	IO_L25P_6	AB24	NC
6	IO_L25N_6	AA24	NC
6	IO_L27P_6	AC25	NC
6	IO_L27N_6/VREF_6	AB25	NC
6	IO_L43P_6	AF31	
6	IO_L43N_6	AE31	
6	IO_L44P_6	AA23	
6	IO_L44N_6	Y23	
6	IO_L45P_6	AE30	
6	IO_L45N_6/VREF_6	AC30	
6	IO_L46P_6	AC28	
6	IO_L46N_6	AA28	
6	IO_L47P_6	AD27	
6	IO_L47N_6	AC27	
6	IO_L48P_6	AA25	
6	IO_L48N_6	Y25	
6	IO_L49P_6	AC29	
6	IO_L49N_6	AB29	
6	IO_L50P_6	AB27	
6	IO_L50N_6	AA27	
6	IO_L51P_6	AA26	
6	IO_L51N_6/VREF_6	Y26	
6	IO_L52P_6	AD31	
6	IO_L52N_6	AC31	
6	IO_L53P_6	W22	
6	IO_L53N_6	V22	
6	IO_L54P_6	Y27	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L54N_6	W27	
6	IO_L67P_6	AB30	
6	IO_L67N_6	AA30	
6	IO_L68P_6	W26	
6	IO_L68N_6	V26	
6	IO_L69P_6	AB31	
6	IO_L69N_6/VREF_6	AA31	
6	IO_L70P_6	AA29	
6	IO_L70N_6	Y29	
6	IO_L71P_6	Y24	
6	IO_L71N_6	W24	
6	IO_L72P_6	V25	
6	IO_L72N_6	U25	
6	IO_L73P_6	Y28	
6	IO_L73N_6	W28	
6	IO_L74P_6	W23	
6	IO_L74N_6	V23	
6	IO_L75P_6	Y30	
6	IO_L75N_6/VREF_6	W30	
6	IO_L76P_6	Y31	
6	IO_L76N_6	W31	
6	IO_L77P_6	V27	
6	IO_L77N_6	U27	
6	IO_L78P_6	W29	
6	IO_L78N_6	U29	
6	IO_L91P_6	U23	
6	IO_L91N_6	T23	
6	IO_L92P_6	U26	
6	IO_L92N_6	T26	
6	IO_L93P_6	V28	
6	IO_L93N_6/VREF_6	U28	
6	IO_L94P_6	U24	
6	IO_L94N_6	T24	
6	IO_L95P_6	V30	
6	IO_L95N_6	U30	
6	IO_L96P_6	V31	
6	IO_L96N_6	U31	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L96P_7	T27	
7	IO_L96N_7	R27	
7	IO_L95P_7	R24	
7	IO_L95N_7	N24	
7	IO_L94P_7	T29	
7	IO_L94N_7	R29	
7	IO_L93P_7/VREF_7	R31	
7	IO_L93N_7	P31	
7	IO_L92P_7	R26	
7	IO_L92N_7	P26	
7	IO_L91P_7	R30	
7	IO_L91N_7	P30	
7	IO_L78P_7	R25	
7	IO_L78N_7	P25	
7	IO_L77P_7	R28	
7	IO_L77N_7	P28	
7	IO_L76P_7	N31	
7	IO_L76N_7	M31	
7	IO_L75P_7/VREF_7	R23	
7	IO_L75N_7	P23	
7	IO_L74P_7	N30	
7	IO_L74N_7	M30	
7	IO_L73P_7	P27	
7	IO_L73N_7	N27	
7	IO_L72P_7	P22	
7	IO_L72N_7	N22	
7	IO_L71P_7	N29	
7	IO_L71N_7	M29	
7	IO_L70P_7	N28	
7	IO_L70N_7	M28	
7	IO_L69P_7/VREF_7	N26	
7	IO_L69N_7	M26	
7	IO_L68P_7	L31	
7	IO_L68N_7	K31	
7	IO_L67P_7	M27	
7	IO_L67N_7	L27	
7	IO_L54P_7	N23	
7	IO_L54N_7	M23	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L53P_7	L30	
7	IO_L53N_7	K30	
7	IO_L52P_7	L28	
7	IO_L52N_7	J28	
7	IO_L51P_7/VREF_7	M24	
7	IO_L51N_7	L24	
7	IO_L50P_7	L29	
7	IO_L50N_7	K29	
7	IO_L49P_7	M25	
7	IO_L49N_7	L25	
7	IO_L48P_7	L26	
7	IO_L48N_7	J26	
7	IO_L47P_7	J31	
7	IO_L47N_7	H31	
7	IO_L46P_7	J29	
7	IO_L46N_7	H29	
7	IO_L45P_7/VREF_7	M22	
7	IO_L45N_7	L22	
7	IO_L44P_7	J30	
7	IO_L44N_7	G30	
7	IO_L43P_7	K27	
7	IO_L43N_7	J27	
7	IO_L27P_7/VREF_7	L23	NC
7	IO_L27N_7	K23	NC
7	IO_L25P_7	G31	NC
7	IO_L25N_7	F31	NC
7	IO_L24P_7	F30	
7	IO_L24N_7	E30	
7	IO_L23P_7	K25	
7	IO_L23N_7	J25	
7	IO_L22P_7	H28	
7	IO_L22N_7	G28	
7	IO_L21P_7/VREF_7	H27	
7	IO_L21N_7	G27	
7	IO_L20P_7	K24	
7	IO_L20N_7	J24	
7	IO_L19P_7	E31	
7	IO_L19N_7	D31	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L06P_7	F28	
7	IO_L06N_7	E28	
7	IO_L05P_7	K22	
7	IO_L05N_7	K21	
7	IO_L04P_7	F29	
7	IO_L04N_7	E29	
7	IO_L03P_7/VREF_7	H26	
7	IO_L03N_7	H25	
7	IO_L02P_7/VRN_7	G26	
7	IO_L02N_7/VRP_7	F27	
7	IO_L01P_7	D30	
7	IO_L01N_7	D29	
0	VCCO_0	C18	
0	VCCO_0	C25	
0	VCCO_0	F22	
0	VCCO_0	H18	
0	VCCO_0	L17	
0	VCCO_0	L18	
0	VCCO_0	L19	
0	VCCO_0	L20	
0	VCCO_0	M17	
0	VCCO_0	M18	
0	VCCO_0	M19	
1	VCCO_1	C7	
1	VCCO_1	C14	
1	VCCO_1	F10	
1	VCCO_1	H14	
1	VCCO_1	L12	
1	VCCO_1	L13	
1	VCCO_1	L14	
1	VCCO_1	L15	
1	VCCO_1	M13	
1	VCCO_1	M14	
1	VCCO_1	M15	
2	VCCO_2	G3	
2	VCCO_2	K6	
2	VCCO_2	M11	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	VCCO_2	N11	
2	VCCO_2	N12	
2	VCCO_2	P3	
2	VCCO_2	P8	
2	VCCO_2	P11	
2	VCCO_2	P12	
2	VCCO_2	R11	
2	VCCO_2	R12	
3	VCCO_3	U11	
3	VCCO_3	U12	
3	VCCO_3	V3	
3	VCCO_3	V8	
3	VCCO_3	V11	
3	VCCO_3	V12	
3	VCCO_3	W11	
3	VCCO_3	W12	
3	VCCO_3	Y11	
3	VCCO_3	AB6	
3	VCCO_3	AE3	
4	VCCO_4	Y13	
4	VCCO_4	Y14	
4	VCCO_4	Y15	
4	VCCO_4	AA12	
4	VCCO_4	AA13	
4	VCCO_4	AA14	
4	VCCO_4	AA15	
4	VCCO_4	AD14	
4	VCCO_4	AF10	
4	VCCO_4	AJ7	
4	VCCO_4	AJ14	
5	VCCO_5	Y17	
5	VCCO_5	Y18	
5	VCCO_5	Y19	
5	VCCO_5	AA17	
5	VCCO_5	AA18	
5	VCCO_5	AA19	
5	VCCO_5	AA20	
5	VCCO_5	AD18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	VCCO_5	AF22	
5	VCCO_5	AJ18	
5	VCCO_5	AJ25	
6	VCCO_6	U20	
6	VCCO_6	U21	
6	VCCO_6	V20	
6	VCCO_6	V21	
6	VCCO_6	V24	
6	VCCO_6	V29	
6	VCCO_6	W20	
6	VCCO_6	W21	
6	VCCO_6	Y21	
6	VCCO_6	AB26	
6	VCCO_6	AE29	
7	VCCO_7	G29	
7	VCCO_7	K26	
7	VCCO_7	M21	
7	VCCO_7	N20	
7	VCCO_7	N21	
7	VCCO_7	P20	
7	VCCO_7	P21	
7	VCCO_7	P24	
7	VCCO_7	P29	
7	VCCO_7	R20	
7	VCCO_7	R21	
NA	CCLK	AJ4	
NA	PROG_B	D27	
NA	DONE	AG6	
NA	M0	AH27	
NA	M1	AJ28	
NA	M2	AG26	
NA	HSWAP_EN	E26	
NA	TCK	K11	
NA	TDI	C28	
NA	TDO	C4	
NA	TMS	J10	
NA	PWRDWN_B	AH5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	DXN	F25	
NA	DXP	B28	
NA	VBATT	D5	
NA	RSVD	B4	
NA	VCCAUX	B16	
NA	VCCAUX	C2	
NA	VCCAUX	C30	
NA	VCCAUX	T2	
NA	VCCAUX	T30	
NA	VCCAUX	AJ2	
NA	VCCAUX	AJ30	
NA	VCCAUX	AK16	
NA	VCCINT	K15	
NA	VCCINT	K17	
NA	VCCINT	L11	
NA	VCCINT	L16	
NA	VCCINT	L21	
NA	VCCINT	M12	
NA	VCCINT	M16	
NA	VCCINT	M20	
NA	VCCINT	N13	
NA	VCCINT	N14	
NA	VCCINT	N15	
NA	VCCINT	N16	
NA	VCCINT	N17	
NA	VCCINT	N18	
NA	VCCINT	N19	
NA	VCCINT	P13	
NA	VCCINT	P19	
NA	VCCINT	R10	
NA	VCCINT	R13	
NA	VCCINT	R19	
NA	VCCINT	R22	
NA	VCCINT	T11	
NA	VCCINT	T12	
NA	VCCINT	T13	
NA	VCCINT	T19	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCINT	T20	
NA	VCCINT	T21	
NA	VCCINT	U10	
NA	VCCINT	U13	
NA	VCCINT	U19	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V19	
NA	VCCINT	W13	
NA	VCCINT	W14	
NA	VCCINT	W15	
NA	VCCINT	W16	
NA	VCCINT	W17	
NA	VCCINT	W18	
NA	VCCINT	W19	
NA	VCCINT	Y12	
NA	VCCINT	Y16	
NA	VCCINT	Y20	
NA	VCCINT	AA11	
NA	VCCINT	AA16	
NA	VCCINT	AA21	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	GND	A2	
NA	GND	A3	
NA	GND	A16	
NA	GND	A29	
NA	GND	A30	
NA	GND	B1	
NA	GND	B2	
NA	GND	B8	
NA	GND	B24	
NA	GND	B30	
NA	GND	B31	
NA	GND	C1	
NA	GND	C3	
NA	GND	C29	
NA	GND	C31	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D4	
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	

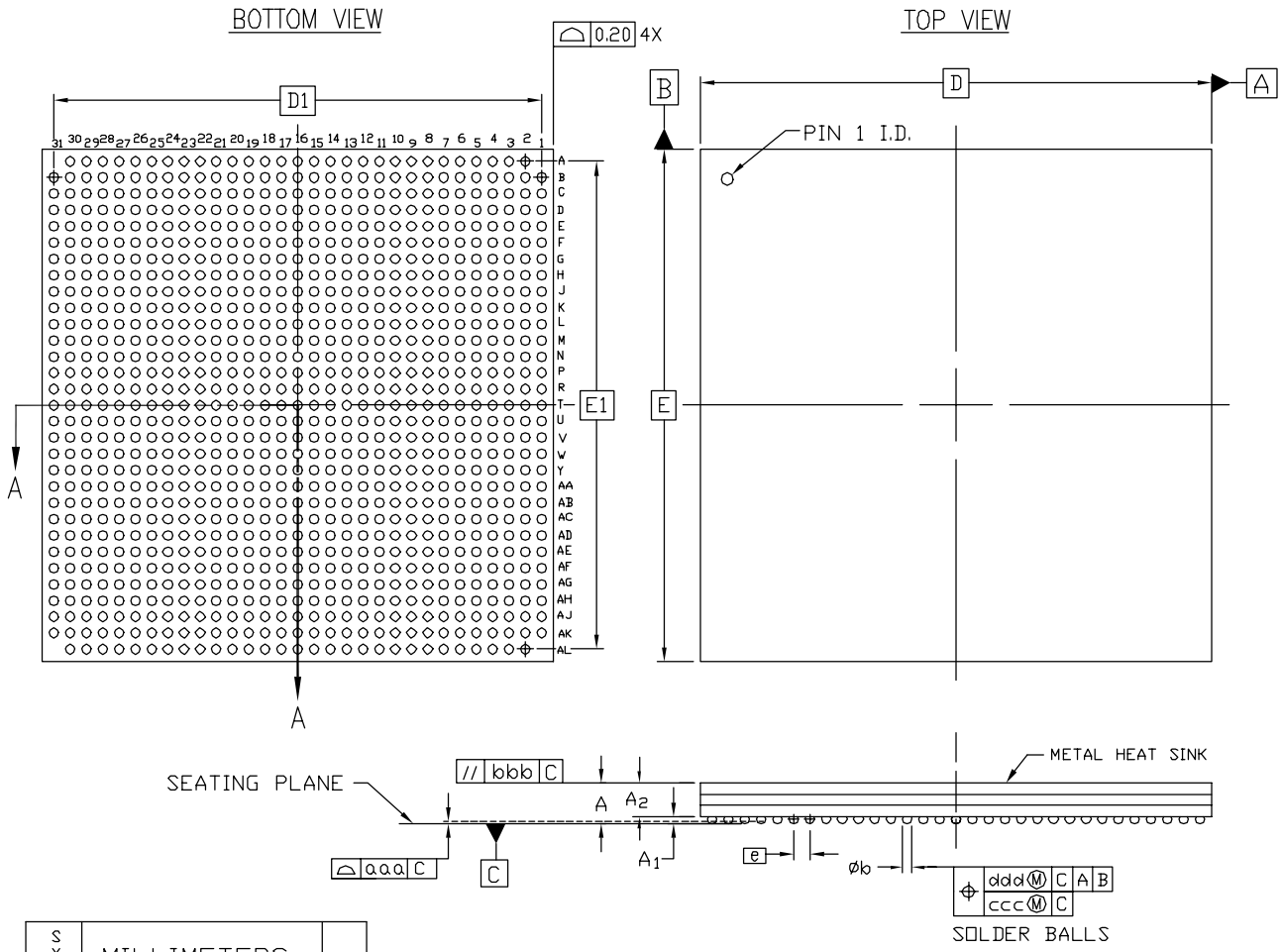
Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T10	
NA	GND	T14	
NA	GND	T15	
NA	GND	T16	
NA	GND	T17	
NA	GND	T18	
NA	GND	T22	
NA	GND	T25	
NA	GND	T28	
NA	GND	T31	
NA	GND	U14	
NA	GND	U15	
NA	GND	U16	
NA	GND	U17	
NA	GND	U18	
NA	GND	V14	
NA	GND	V15	
NA	GND	V16	
NA	GND	V17	
NA	GND	V18	
NA	GND	W7	
NA	GND	W25	
NA	GND	AB4	
NA	GND	AB16	
NA	GND	AB28	
NA	GND	AC9	
NA	GND	AC23	
NA	GND	AD2	
NA	GND	AD8	
NA	GND	AD24	
NA	GND	AD30	
NA	GND	AE7	
NA	GND	AE13	
NA	GND	AE16	
NA	GND	AE19	
NA	GND	AE25	
NA	GND	AF6	
NA	GND	AF26	

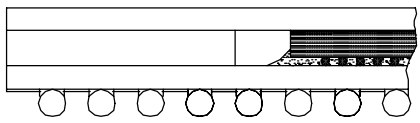
Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	AG5	
NA	GND	AG27	
NA	GND	AH4	
NA	GND	AH10	
NA	GND	AH16	
NA	GND	AH22	
NA	GND	AH28	
NA	GND	AJ1	
NA	GND	AJ3	
NA	GND	AJ29	
NA	GND	AJ31	
NA	GND	AK1	
NA	GND	AK2	
NA	GND	AK8	
NA	GND	AK24	
NA	GND	AK30	
NA	GND	AK31	
NA	GND	AL2	
NA	GND	AL3	
NA	GND	AL16	
NA	GND	AL29	
NA	GND	AL30	

BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.25	3.50	
A_1	0.50	0.60	0.70	
A_2			2.80	
A_3	0.20			
D/E	40.00 BSC			
D_1/E_1	38.10 REF.			
e	1.27 BSC			
øb	0.60	0.75	0.90	
aaa			0.20	
bbb			0.25	
ccc			0.15	
ddd			0.30	
M	31			



SECTION A–A
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–BAU–1 (DEPOPULATED)

Figure 10: **BF957 Flip-Chip BGA Package Specifications**

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5 on page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6 on page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11 on page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12 on page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). DXN and DXP pin information was added for the CS144 package (Table 5) and the FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8 on page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- DS031-1, Virtex-II 1.5V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS031-2, Virtex-II 1.5V FPGAs: **Functional Description (Module 2)**
- DS031-3, Virtex-II 1.5V FPGAs: **DC and Switching Characteristics (Module 3)**
- DS031-4, Virtex-II 1.5V FPGAs: Pinout Tables (Module 4)