MFG(AA)160 MFY(AA)160
Thyristor/Diode Modules(Non-isolated Type)

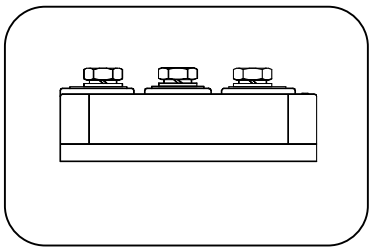
Features:

- **n** Non-Isolated. Mounting base as common
- **n** Pressure contact technology with Increased power cycling capability
- **n** Low on-state voltage drop

Typical Applications

- **n** Welding Power Supply
- **n** Various DC Power supplies
- **n** DC supply for PWM inverter

$I_{T(AV)}$	160 A
V_{DRM}/V_{RRM}	200~600 V
I_{TSM}	5.60 A×10^3
I^2t	160 A^2 S*10^3



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, T_c=110°C	140			160	A
$I_{T(RMS)}$	RMS on-state current		140			251	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+200V respectively	140	200		600	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	140			12	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=60%V_{RRM}	140			5.60	KA
I^2t	I^2T for fusing coordination					160	A^2s*10^3
V_{TO}	Threshold voltage		140			0.80	V
r_T	On-state slop resistance					1.15	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=480A	25			1.43	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	140			800	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t_r ≤0.5μs Repetitive	140			100	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		150	mA
V_{GT}	Gate trigger voltage			1.0		2.5	V
I_H	Holding current			20		200	mA
V_{GD}	Non-trigger gate voltage	At 67%V_{DRM}	140	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled				0.150	°C /W
Rth(c-h)	Thermal resistance case to heatsink	Single side cooled				0.04	°C /W
F_m	Thermal connection torque(M8)				12		N·m
	Mounting torque(M6)				6		N·m
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				680		g
Outline	404F4						

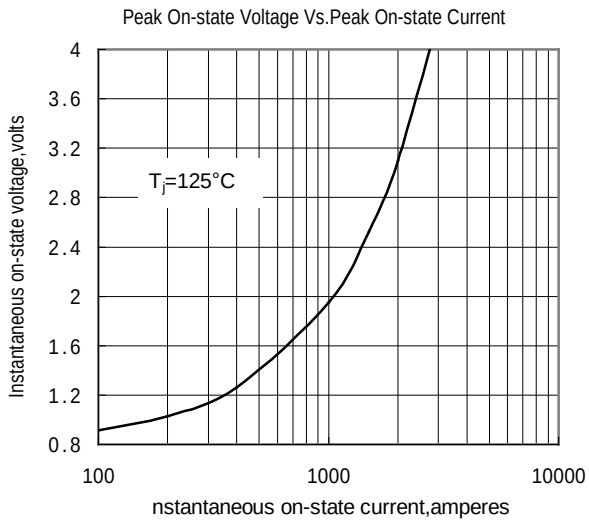


Fig.1

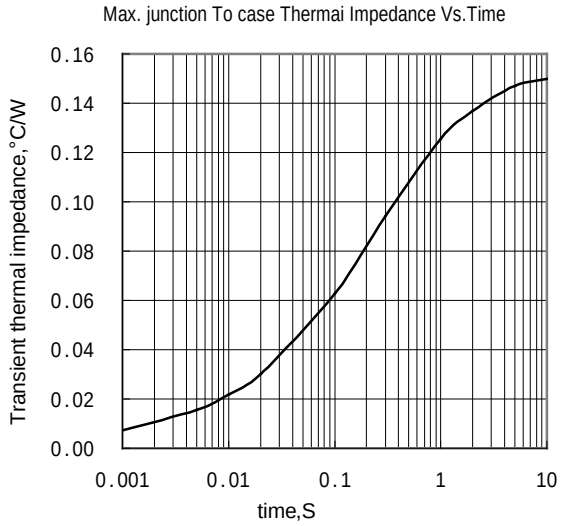


Fig.2

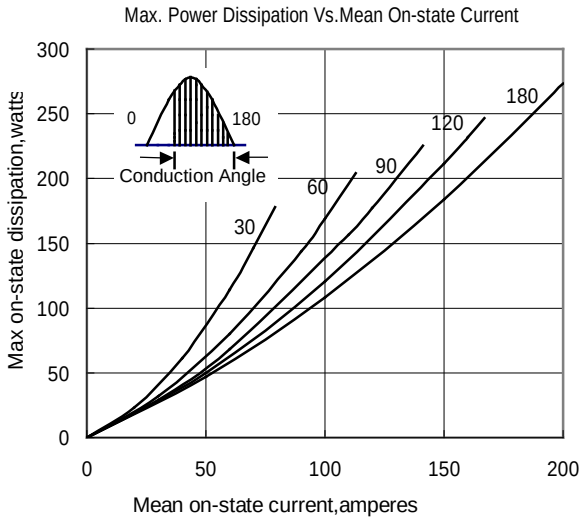


Fig.3

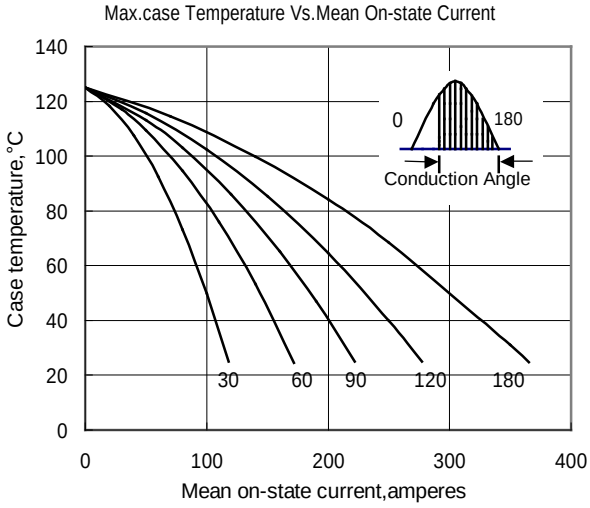


Fig.4

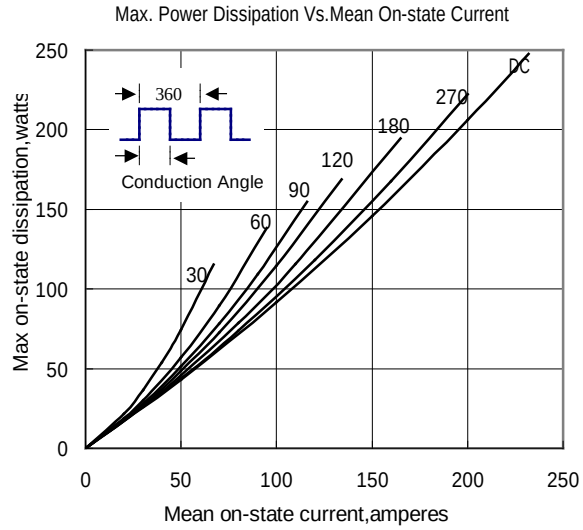


Fig.5

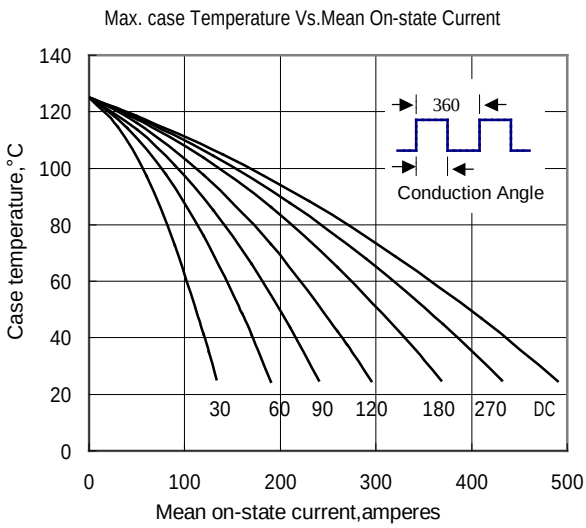


Fig.6

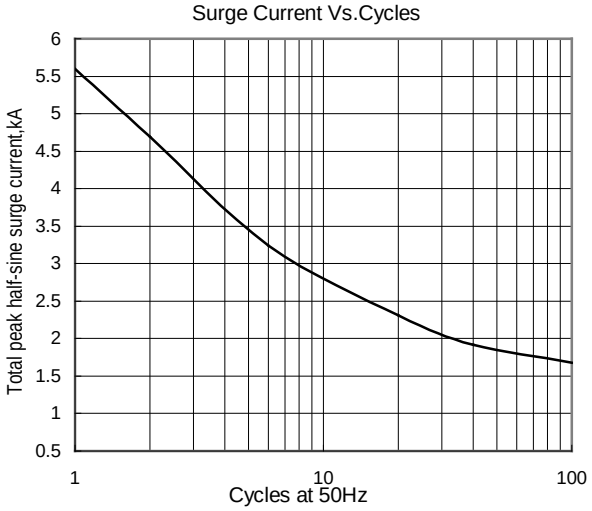


Fig.7

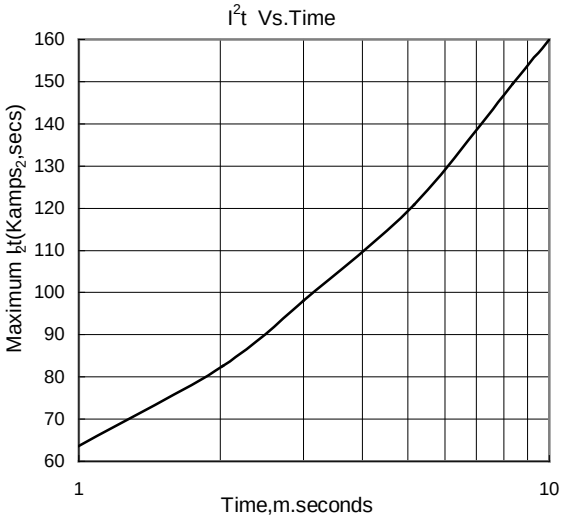


Fig.8

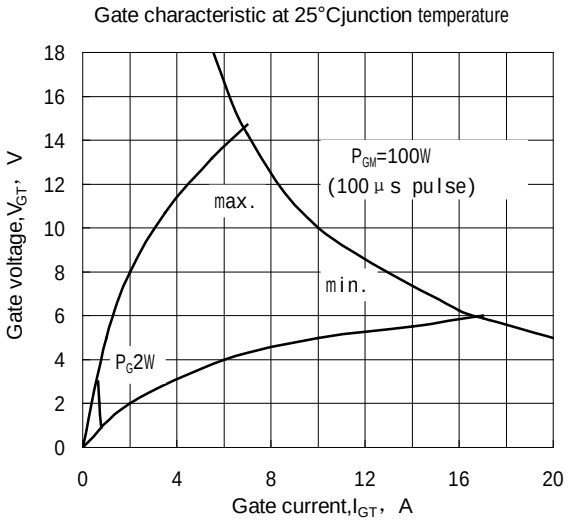


Fig.9

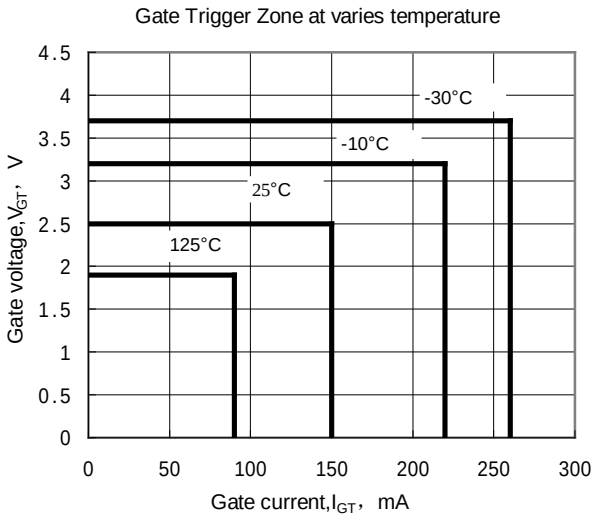
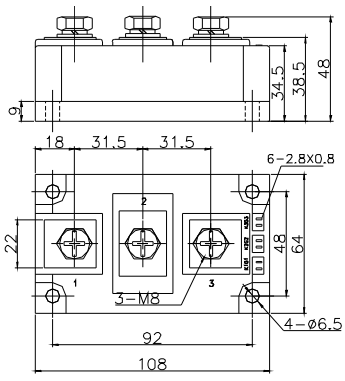


Fig.10

Outline:



404F4