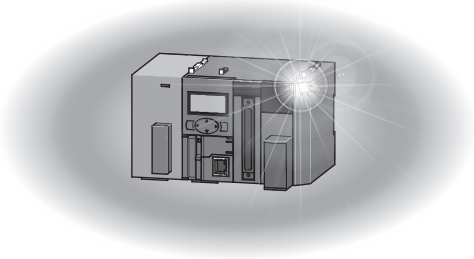
MITSUBISHI ELECTRIC

Programmable Controller

MELSEC *L* series

MELSEC-L Flexible High-Speed I/O Control Module User's Manual

-LD40PD01
-Flexible High-Speed I/O Control Module Configuration tool (SW1DNN-FLEXIOP-E)



SAFETY PRECAUTIONS

(Read these precautions before using this product.)

Before using this product, please read this manual and the relevant manuals carefully and pay full attention to safety to handle the product correctly.

The precautions given in this manual are concerned with this product only. For the safety precautions of the programmable controller system, refer to the user's manual for the CPU module used.

In this manual, the safety precautions are classified into two levels: "⚠ WARNING" and "⚠ CAUTION".

⚠ **WARNING**	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
⚠ **CAUTION**	Indicates that incorrect handling may cause hazardous conditions, resulting in minor or moderate injury or property damage.

Under some circumstances, failure to observe the precautions given under "⚠ CAUTION" may lead to serious consequences.

Observe the precautions of both levels because they are important for personal and system safety.

Make sure that the end users read this manual and then keep the manual in a safe place for future reference.

[Design Precautions]

⚠ WARNING

- In an output circuit, when a load current exceeding the rated current or an overcurrent caused by a load short-circuit flows for a long time, it may cause smoke and fire. To prevent this, configure an external safety circuit, such as a fuse.
- Do not write any data to the "system area" and "write-protect area" (R) of the buffer memory in the intelligent function module. Also, do not use any "use prohibited" signals as an output signal from the programmable controller CPU to the intelligent function module. Doing so may cause malfunction of the programmable controller system.
- Outputs may remain on or off due to a failure of a transistor for external output. Configure an external circuit for monitoring output signals that could cause a serious accident.
- When changing data and operating status of the running module from an external device such as a personal computer connected, configure an interlock circuit external to the programmable controller to ensure that the entire system always operates safely.
  In addition, before performing online operations, determine corrective actions to be taken between the external device and the module in case of a communication failure due to poor contact of cables.

[Design Precautions]

⚠ CAUTION

- Do not install the control lines or communication cables together with the main circuit lines or power cables. Keep a distance of 150mm or more between them. Failure to do so may result in malfunction due to noise.
- During control of an inductive load such as a lamp, heater, or solenoid valve, a large current (approximately ten times greater than normal) may flow when the output is turned from off to on. Therefore, use a module that has a sufficient current rating.

[Installation Precautions]

⚠WARNING

- Shut off the external power supply (all phases) used in the system before mounting or removing a module. Failure to do so may result in electric shock or cause the module to fail or malfunction.

[Installation Precautions]

⚠CAUTION

- Use the programmable controller in an environment that meets the general specifications in the Safety Guidelines provided with the CPU module or head module. Failure to do so may result in electric shock, fire, malfunction, or damage to or deterioration of the product.
- To interconnect modules, engage the respective connectors and securely lock the module joint levers until they click. Incorrect interconnection may cause malfunction, failure, or drop of the module.
- Do not directly touch any conductive parts and electronic components of the module. Doing so can cause malfunction or failure of the module.

[Wiring Precautions]

⚠WARNING

- Shut off the external power supply (all phases) used in the system before wiring. Failure to do so may result in electric shock or cause the module to fail or malfunction.
- When connecting a differential output terminal to a differential receiver of a drive unit, connect the high-speed output common terminal to the differential receiver common terminal of the drive unit. Failure to do so may cause the module to fail or malfunction because of the potential difference that occurs between the high-speed output common terminal and the differential receiver common terminal.

[Wiring Precautions]

⚠CAUTION

- Individually ground the FG and LG terminals of the programmable controller with a ground resistance of 100 ohms or less. Failure to do so may result in electric shock or malfunction.
- Check the rated voltage and terminal layout before wiring to the module, and connect the cables correctly. Connecting a power supply with a different voltage rating or incorrect wiring may cause a fire or failure.
- Connectors for external devices must be crimped with the tool specified by the manufacturer or must be correctly soldered. Incomplete connections may cause short circuit, fire, or malfunction.
- Place the cables in a duct or clamp them. If not, dangling cable may swing or inadvertently be pulled, resulting in damage to the module or cables or malfunction due to poor contact.
- Tighten the connector screws within the specified torque range. Undertightening can cause drop of the screw, short circuit, fire, or malfunction. Overtightening can damage the screw and/or module, resulting in drop, short circuit, fire, or malfunction.
- Prevent foreign matter such as dust or wire chips from entering the module. Such foreign matter can cause a fire, failure, or malfunction.
- A protective film is attached to the top of the module to prevent foreign matter, such as wire chips, from entering the module during wiring. Do not remove the film during wiring. Remove it for heat dissipation before system operation.
- Ground the shield cable on the encoder side (relay box). Always ground the FG and LG terminals to the protective ground conductor. Failure to do so may cause malfunction.
- Mitsubishi programmable controllers must be installed in control panels. Connect the main power supply to the power supply module in the control panel through a relay terminal block. Wiring and replacement of a power supply module must be performed by qualified maintenance personnel with knowledge of protection against electric shock. For wiring methods, refer to the MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection).

[Startup and Maintenance Precautions]

⚠WARNING

- Do not touch any terminal while power is on. Doing so will cause electric shock or malfunction.
- Shut off the external power supply (all phases) used in the system before cleaning the module or retightening the connector screws. Failure to do so may result in electric shock.

[Startup and Maintenance Precautions]

⚠CAUTION

- Do not disassemble or modify the module. Doing so may cause failure, malfunction, injury, or a fire.
- Shut off the external power supply (all phases) used in the system before mounting or removing a module. Failure to do so may cause the module to fail or malfunction.
- After the first use of the product (module and display unit), do not connect/disconnect the product more than 50 times (in accordance with IEC 61131-2). Exceeding the limit may cause malfunction.
- Tighten the connector screws within the specified torque range. Undertightening can cause drop of the component or wire, short circuit, or malfunction. Overtightening can damage the screw and/or module, resulting in drop, short circuit, or malfunction.
- Before handling the module, touch a conducting object such as a grounded metal to discharge the static electricity from the human body. Failure to do so may cause the module to fail or malfunction.
- When performing online operations of the running module from an external device such as a personal computer connected, read the relevant manuals carefully and ensure that the operation is safe before proceeding.
- Before changing any setting of the module, read the relevant manuals carefully, ensure the safety, and change the operating status of the CPU module to STOP.
  Especially when operating the module in the network system, ensure the safety thoroughly because controlled machines are likely to be moved inadvertently. Improper operation may damage machines or cause accidents.

[Disposal Precautions]

⚠CAUTION

- When disposing of this product, treat it as industrial waste.

CONDITIONS OF USE FOR THE PRODUCT

(1) Mitsubishi programmable controller ("the PRODUCT") shall be used in conditions;
i) where any problem, fault or failure occurring in the PRODUCT, if any, shall not lead to any major or serious accident; and
ii) where the backup and fail-safe function are systematically or automatically provided outside of the PRODUCT for the case of any problem, fault or failure occurring in the PRODUCT.

(2) The PRODUCT has been designed and manufactured for the purpose of being used in general industries.
MITSUBISHI SHALL HAVE NO RESPONSIBILITY OR LIABILITY (INCLUDING, BUT NOT LIMITED TO ANY AND ALL RESPONSIBILITY OR LIABILITY BASED ON CONTRACT, WARRANTY, TORT, PRODUCT LIABILITY) FOR ANY INJURY OR DEATH TO PERSONS OR LOSS OR DAMAGE TO PROPERTY CAUSED BY the PRODUCT THAT ARE OPERATED OR USED IN APPLICATION NOT INTENDED OR EXCLUDED BY INSTRUCTIONS, PRECAUTIONS, OR WARNING CONTAINED IN MITSUBISHI'S USER, INSTRUCTION AND/OR SAFETY MANUALS, TECHNICAL BULLETINS AND GUIDELINES FOR the PRODUCT.
("Prohibited Application")
Prohibited Applications include, but not limited to, the use of the PRODUCT in;

- Nuclear Power Plants and any other power plants operated by Power companies, and/or any other cases in which the public could be affected if any problem or fault occurs in the PRODUCT.
- Railway companies or Public service purposes, and/or any other cases in which establishment of a special quality assurance system is required by the Purchaser or End User.
- Aircraft or Aerospace, Medical applications, Train equipment, transport equipment such as Elevator and Escalator, Incineration and Fuel devices, Vehicles, Manned transportation, Equipment for Recreation and Amusement, and Safety devices, handling of Nuclear or Hazardous Materials or Chemicals, Mining and Drilling, and/or other applications where there is a significant risk of injury to the public or property.

Notwithstanding the above, restrictions Mitsubishi may in its sole discretion, authorize use of the PRODUCT in one or more of the Prohibited Applications, provided that the usage of the PRODUCT is limited only for the specific applications agreed to by Mitsubishi and provided further that no special quality assurance or fail-safe, redundant or other safety features which exceed the general specifications of the PRODUCTs are required. For details, please contact the Mitsubishi representative in your region.

INTRODUCTION

Thank you for purchasing the Mitsubishi Electric MELSEC-L series programmable controllers. This manual describes the functions and programming of a flexible high-speed I/O control module.

Before using this product, please read this manual and the relevant manuals carefully and develop familiarity with the functions and performance of the MELSEC-L series programmable controller to handle the product correctly.
When applying the program examples introduced in this manual to an actual system, ensure the applicability and confirm that it will not cause system control problems.

Relevant product

LD40PD01

Point

Unless otherwise specified, this manual describes the program examples in which the I/O numbers of X/Y00 to X/Y1F are assigned for a flexible high-speed I/O control module. For I/O number assignment, refer to the following.

MELSEC-L CPU Module User's Manual (Function Explanation, Program Fundamentals)

COMPLIANCE WITH EMC AND LOW VOLTAGE DIRECTIVES

Method of ensuring compliance

To ensure that Mitsubishi programmable controllers maintain EMC and Low Voltage Directives when incorporated into other machinery or equipment, certain measures may be necessary. Please refer to one of the following manuals.

- MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection)
- MELSEC-L CC-Link IE Field Network Head Module User's Manual
- Safety Guidelines (This manual is included with the CPU module or head module.)

The CE mark on the side of the programmable controller indicates compliance with EMC and Low Voltage Directives.

Additional measures

To ensure that this product maintains EMC and Low Voltage Directives, please refer to the following.

Page 37 External wiring precautions

MEMO

CONTENTS

RELEVANT MANUALS

CPU module user's manual

Manual name [Manual number]	Description
MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection) [SH-080890ENG]	Specifications of the CPU modules, power supply modules, display unit, branch module, extension module, SD memory cards, and batteries, information on how to establish a system, maintenance and inspection, and troubleshooting
MELSEC-L CPU Module User's Manual (Function Explanation, Program Fundamentals) [SH-080889ENG]	Functions and devices of the CPU module, and programming

Head module user's manual

Manual name [Manual number]	Description
MELSEC-L CC-Link IE Field Network Head Module User's Manual [SH-080919ENG]	Specifications, procedures before operation, system configuration, installation, wiring, settings, and troubleshooting of the head module
MELSEC-L SSCNETⅢ/H Head Module User's Manual [SH-081152ENG]	Specifications, procedures before operation, system configuration, installation, wiring, settings, and troubleshooting of the head module

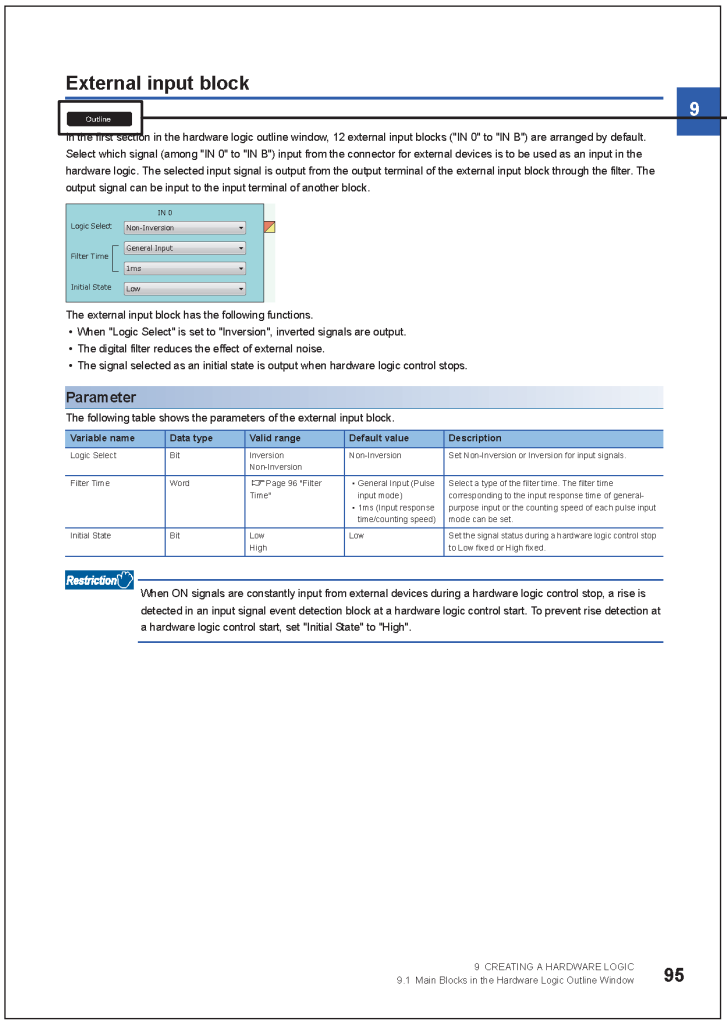
Operating manual

Manual name [Manual number]	Description
GX Works2 Version 1 Operating Manual (Common) [SH-080779ENG]	System configuration, parameter settings, and online operations of GX Works2, which are common to Simple projects and Structured projects
GX LogViewer Version 1 Operating Manual [SH-080915ENG]	System configuration, functions, and operating methods of GX LogViewer

MANUAL PAGE ORGANIZATION

Pages describing the hardware logic are organized as shown below.

The following illustration is for explanation purpose only, and should not be referred to as an actual documentation.



External input block

Outline

9

In the first section in the hardware logic outline window, 12 external input blocks ("IN 0" to "IN B") are arranged by default. Select which signal (among "IN 0" to "IN B") input from the connector for external devices is to be used as an input in the hardware logic. The selected input signal is output from the output terminal of the external input block through the filter. The output signal can be input to the input terminal of another block.

IN 0
Logic Select: Non-Inversion
Filter Time: General Input / 1ms
Initial State: Low

The external input block has the following functions.

- When "Logic Select" is set to "Inversion", inverted signals are output.
- The digital filter reduces the effect of external noise.
- The signal selected as an initial state is output when hardware logic control stops.

Parameter

The following table shows the parameters of the external input block.

Variable name	Data type	Valid range	Default value	Description
Logic Select	Bit	Inversion Non-Inversion	Non-Inversion	Set Non-Inversion or Inversion for input signals.
Filter Time	Word	Page 96 "Filter Time"	• General Input (Pulse input mode) • 1ms (Input response time/counting speed)	Select a type of the filter time. The filter time corresponding to the input response time of general-purpose input or the counting speed of each pulse input mode can be set.
Initial State	Bit	Low High	Low	Set the signal status during a hardware logic control stop to Low fixed or High fixed.

Restriction

When ON signals are constantly input from external devices during a hardware logic control stop, a rise is detected in an input signal event detection block at a hardware logic control start. To prevent rise detection at a hardware logic control start, set "Initial State" to "High".

9 CREATING A HARDWARE LOGIC
9.1 Main Blocks in the Hardware Logic Outline Window
95

An icon displayed here indicates the window where the terminal or block is used.

The meaning of each icon is as follows.

Icon	Description
Outline	The "Outline" icon indicates that the terminal or block is the one for the hardware logic outline window.
Multi function	The "Multi function" icon indicates that the terminal or block is the one for multi function counter block detail windows.

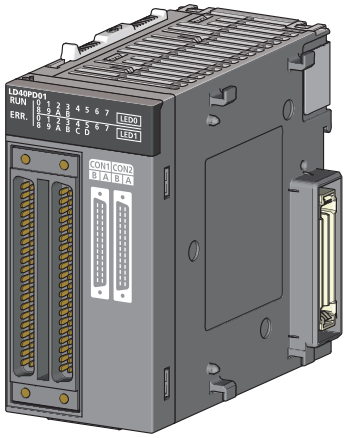
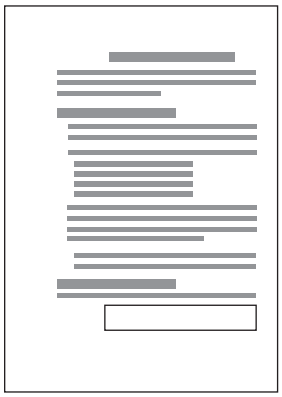
TERMS

Unless otherwise specified, this manual uses the following terms.

Term	Description
Buffer memory	A memory in an intelligent function module, where data (such as setting values and monitoring values) exchanged with a CPU module are stored
Configuration tool	The abbreviation for the configuration tool for flexible high-speed I/O control modules (SW1DNN-FLEXIOP-E)
Display unit	A liquid LCD to be attached to the CPU module
Execution memory	The memory in a flexible high-speed I/O control module where the hardware logic is written
External wiring	Wiring between a flexible high-speed I/O control module and external devices
Flash ROM	A non-volatile memory to which the hardware logic can be written. Although the number of writes to a flash ROM is limited, the written hardware logic is not deleted even after the power off and automatically read at the power-on.
Flexible high-speed I/O control module	The abbreviation for the MELSEC-L series flexible high-speed I/O control module LD40PD01
GX LogViewer	The software for visually displaying execution results of the simulation function
GX Works2	The product name of the software package for the MELSEC programmable controllers
Hardware logic	A control logic that users create graphically combining inputs, outputs, logical operation circuits, and counters with the configuration tool
Head module	The Abbreviation for the LJ72GF15-T2 CC-Link IE Field Network head module
Link	To connect blocks or terminals on the configuration tool
Programming tool	Another name for GX Works2

PACKING LIST

The following items are included in the package of this product. Before use, check that all the items are included.

Flexible high-speed I/O control module	
 Module	 Before Using the Product

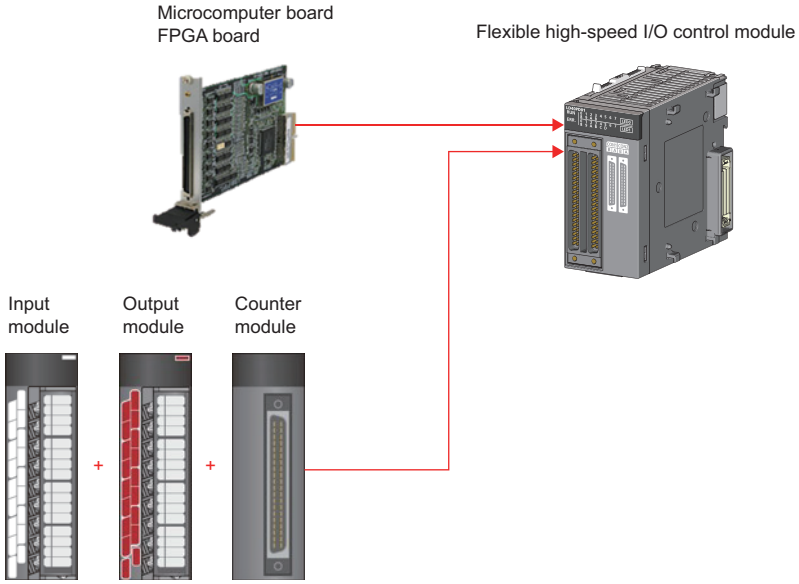
1 FLEXIBLE HIGH-SPEED I/O CONTROL MODULE

For the flexible high-speed I/O control module, users can easily create a high-speed, complicated hardware logic independent from the CPU module by graphically combining input/outputs, logical operation circuits, and counters with the configuration tool.

1.1 Features

Controls that have been performed using a microcomputer board or an FPGA board or combining several modules can be performed only with the flexible high-speed I/O control module.

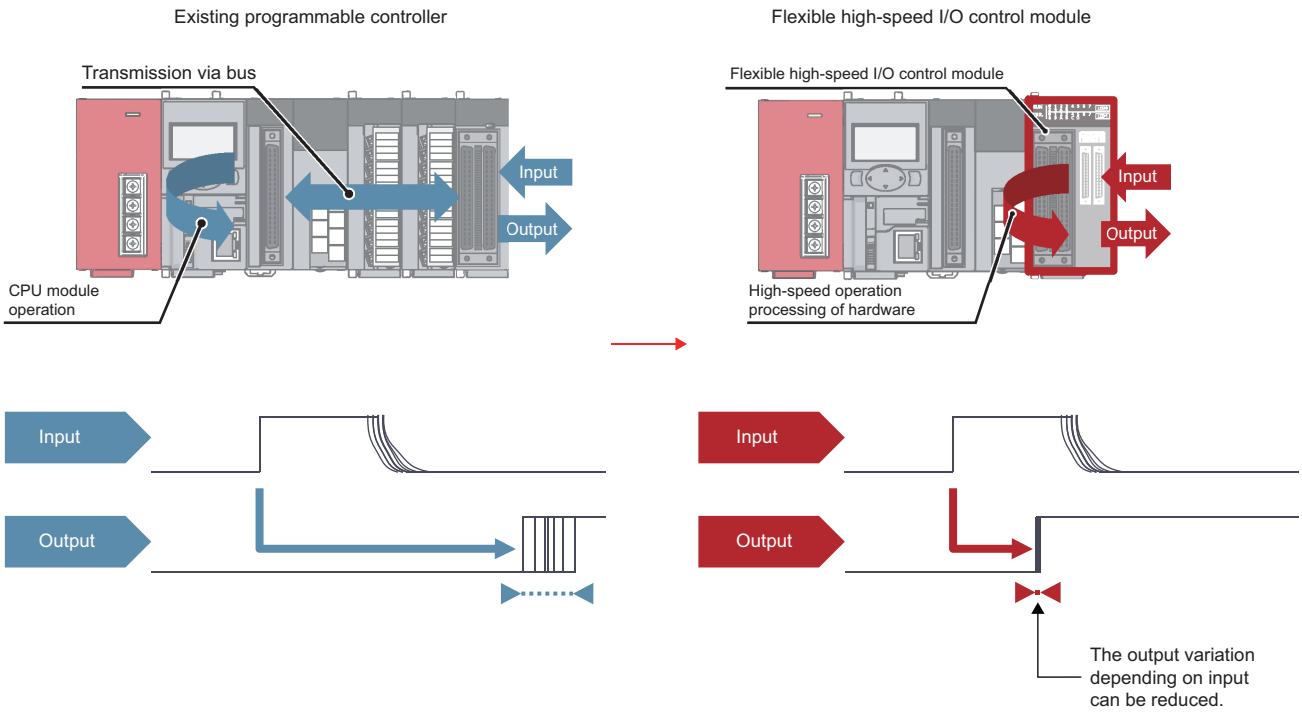
- High-speed, high-response control with μs orders
- Controls with stable response time
- Logic controls that requires rapidity
- Measurement control with sensor inputs
- Controls triggered by external inputs



By using this module instead of a microcomputer board or an FPGA board, which cannot be supplied steadily and constantly due to their high introduction cost and design cost, users can configure a system only with a programmable controller, reducing man-hours and the total system cost.

High-speed, stable I/O response

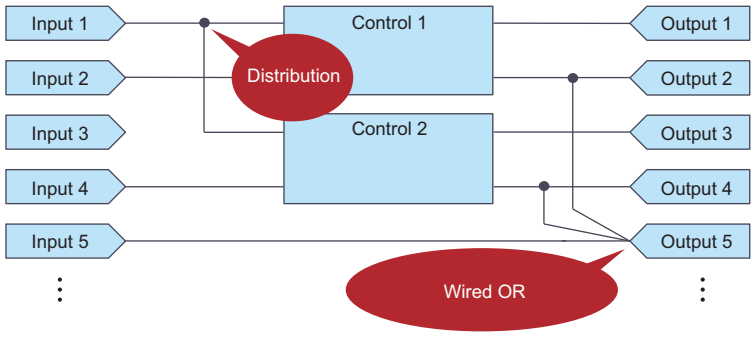
Because the hardware logic inside the module performs controls without relying on the operation processing time and the bus transmission time of the CPU module, high-speed, stable I/O responses can be performed. As a result, variations of outputs to inputs can be reduced.



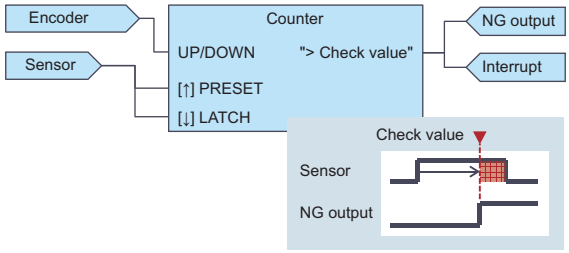
Flexible controls

I/O signals can be flexibly assigned.

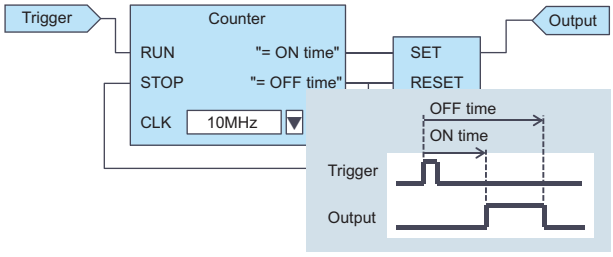
I/Os can be flexibly controlled with high-accuracy counters and timers.



● Length measurement monitor



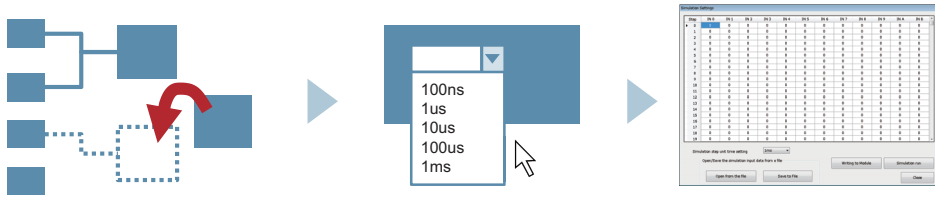
● One-shot pulse output control



Easy designing - select and connect

User can easily create a hardware logic with intuitive actions of "selecting" and "connecting".

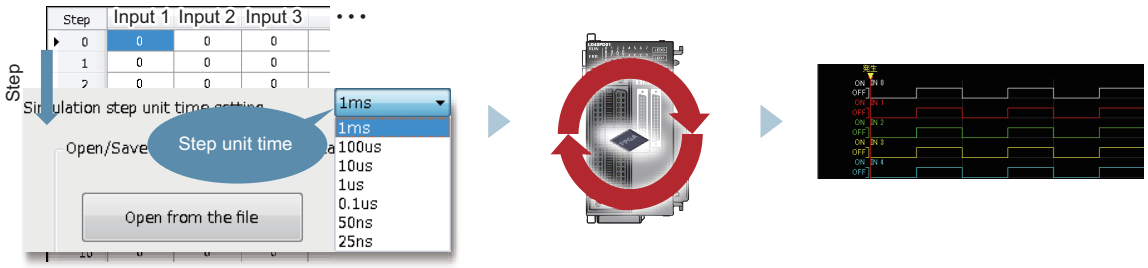
Selecting → Connecting → Setting parameters → Debugging



Simulation function

The operation of a created hardware logic can be checked using simulation data instead of external input signals.

Simulation data → Execute the simulation with the module. → Check the result with GX LogViewer.

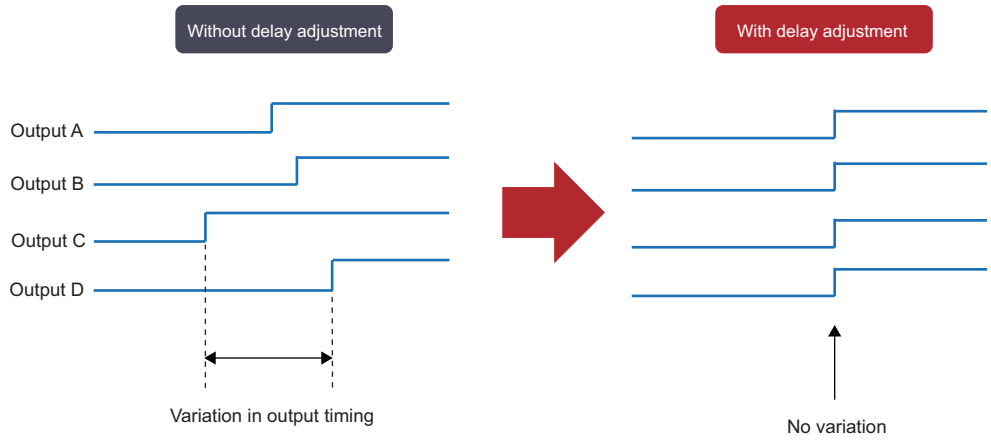


Filter for eliminating noise

A filter for reducing external noise has been implemented for external inputs. This filter eliminates chattering of input pulses.

Delay adjustment of output timing

The delay adjustment function has been implemented for external outputs. The delay adjustment function adjusts the output timing.



The timing variation due to electronic components can be adjusted.

Interrupt function

When a signal that triggers an interrupt is detected, the flexible high-speed I/O control module will send an interrupt request to the CPU module.

The flexible high-speed I/O control module enables a flexible, high-speed interrupt control with this function.

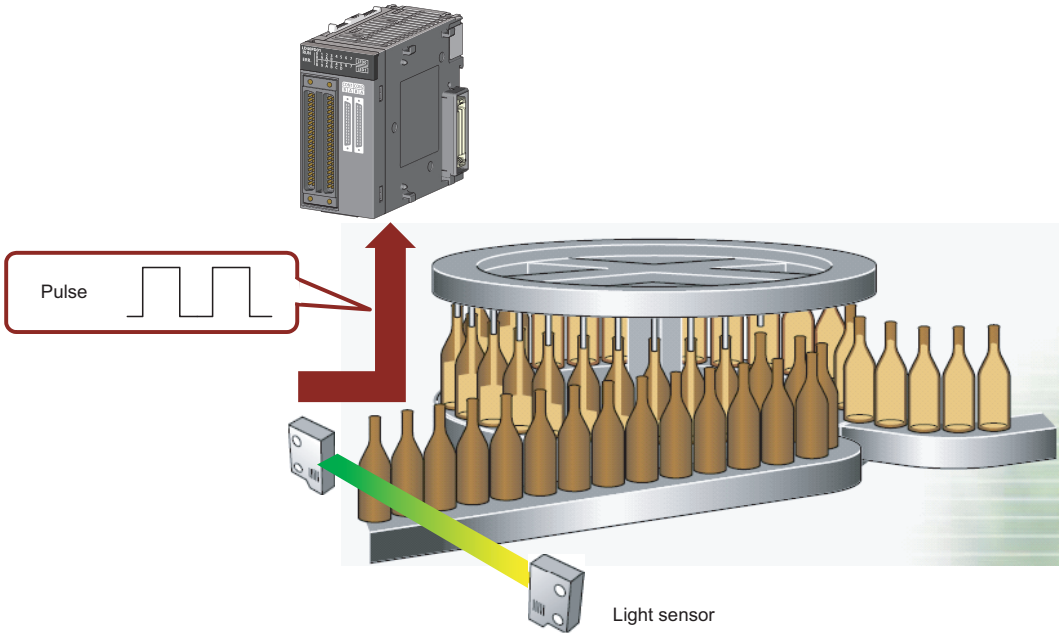
1.2 Application Example

The flexible high-speed I/O control module realizes the following applications.

Pulse measurement

Pulses can be measured with a measurement resolution of 25ns. Pulse widths (ON width and OFF width) of pulse signals can be measured with a high degree of accuracy. This measurement can be applied to variable pulse measurement applications, such as the workpiece length measurement and control of transportation and machining speeds in each carrier device and machining equipment.

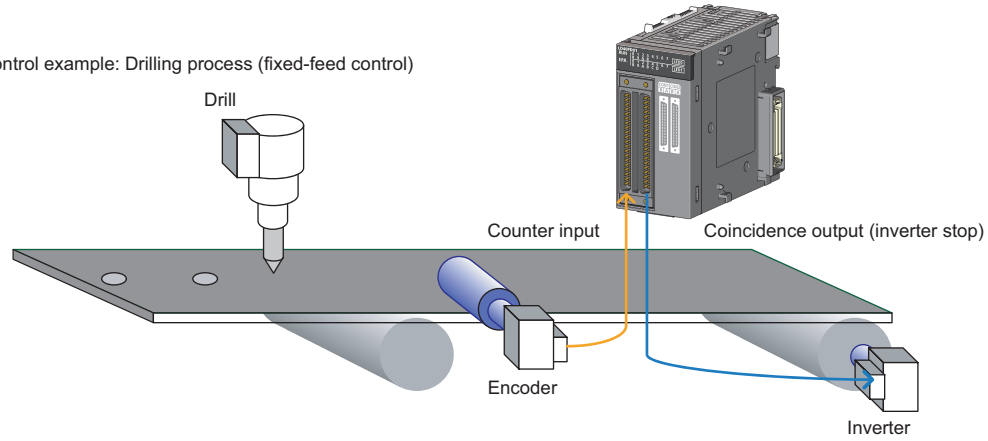
Example: Filling process (container type identification control)



Coincidence output

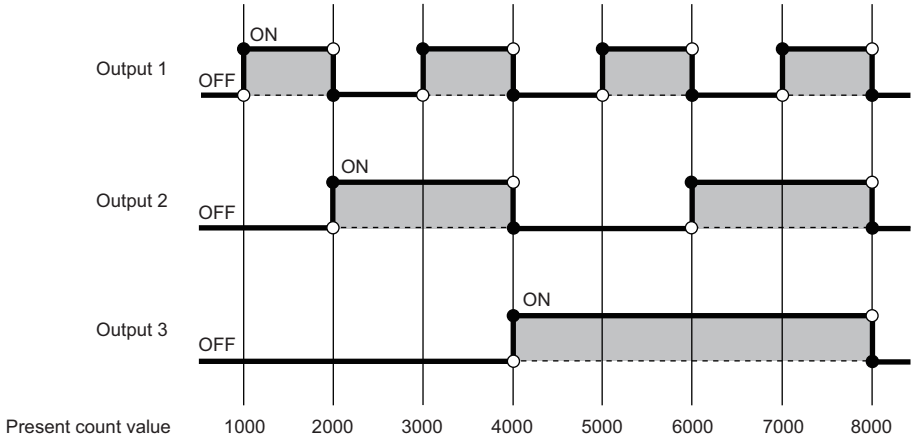
The coincidence output enables a desired fixed-feed control comparing a preset compare value and an input count value.

Control example: Drilling process (fixed-feed control)



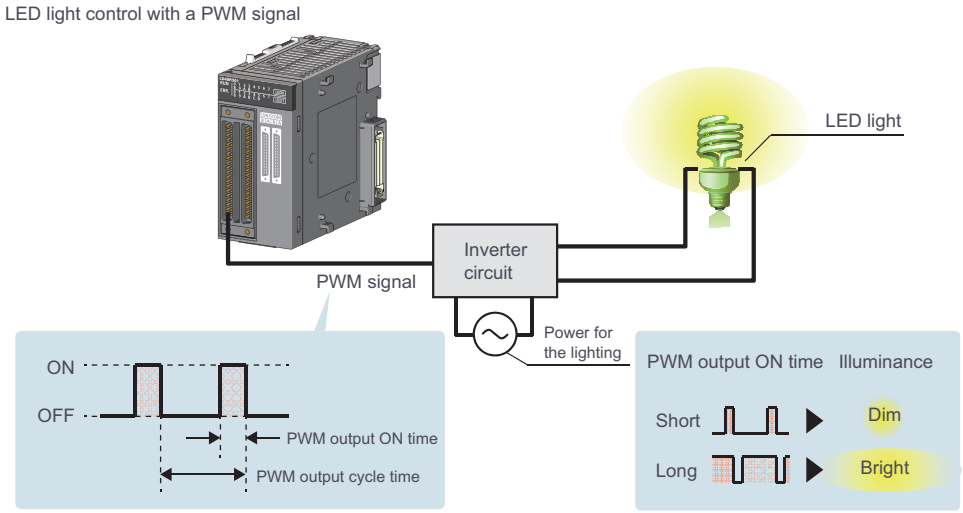
Cam switch output

According to an input count current value, outputs can be turned on or off at preset points without a program. ON/OFF controls can be performed with greater accuracy without being affected by scan time.



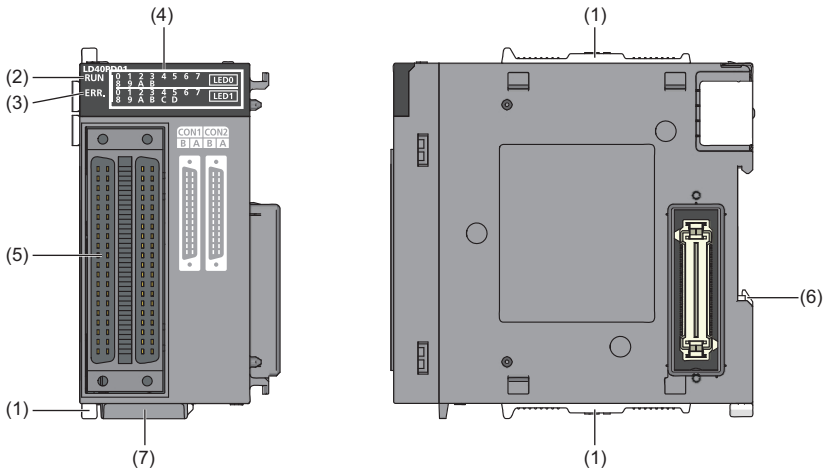
PWM output

PWM of 2MHz at a maximum can be output. The duty ratio can be changed in increments of 25ns, enabling a smooth output control. With PWM outputs, a dimming control with duty ratio changes can be performed.



2 PART NAMES

This chapter lists the part names of the flexible high-speed I/O control module.



No.	Name	Description
(1)	Module joint lever	A lever for connecting two modules
(2)	RUN LED	This LED indicates the operating status. On: Normal operation Flashing: During simulation Off: When 5V power off or a watchdog timer error has occurred
(3)	ERR. LED	This LED indicates the error status. On: An error has occurred. Off: Normal operation
(4)	Indicator LED	This LED indicates the I/O status of external I/O terminals.
	LED0 (Upper section)	This LED indicates the input status of each external input terminal. • On: A voltage has been applied. • Off: No voltage has been applied. 0 to B indicate external input terminals (IN 0 to IN B).
	LED1 (Lower section)	This LED indicates the output status of each external output terminal.*1 • On: A signal output is on. • Off: A signal output is off. 0 to D indicate the following external output terminals. • 0 to 7: OUT 0 to OUT 7 • 8 to D: OUT 0_DIF to OUT 5_DIF
(5)	Connector for external devices (40 pins)	A connector used to connect encoders and control devices. For the terminal layout, refer to the following. ☞ Page 43 Interface with external devices
(6)	DIN rail hook	A hook used to mount the module to a DIN rail
(7)	Serial number marking	Displays the serial number printed on the rating plate.

*1 For differential output terminals, the LED indicates the ON/OFF status of each differential output+ signal.

MEMO

3 SPECIFICATIONS

This chapter describes general specifications, performance specifications, functions, I/O signals, and buffer memory areas.

3.1 General Specifications

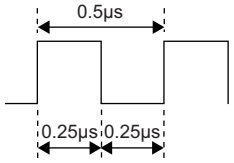
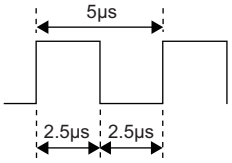
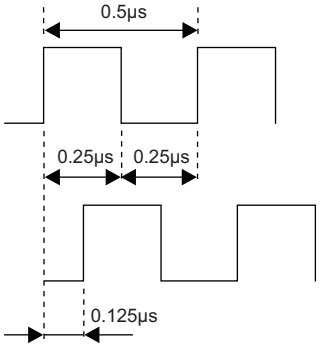
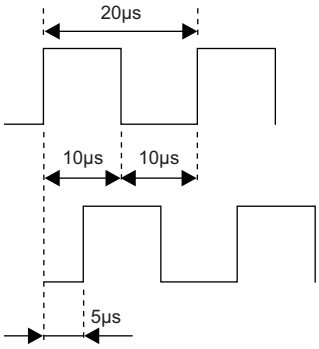
For the general specifications of the flexible high-speed I/O control module, refer to the following.

Safety Guidelines, provided with the CPU module or head module

3.2 Performance Specifications

The following table lists the performance specifications of the flexible high-speed I/O control module.

Item				Specifications	
				Differential	DC
Number of input points				12 points (common for 5VDC/24VDC/differential)	
Number of output points				6 points	8 points (5 to 24VDC, 0.1A/point)
Number of interrupts				8 points	
Input response time				1μs or less	
Output response time				1μs or less	
Pulse input speed				Max. 8Mpps (2MHz)	Max. 200kpps (200kHz)
Pulse output speed				Max. 8Mpps (2MHz)	Max. 200kpps (200kHz)
Main block[*1]	External input block	Logic Select		Inverted, not inverted	
		Filter Time		General-purpose input:	0μs, 10μs, 50μs, 0.1ms, 0.2ms, 0.4ms, 0.6ms, 1ms, 5ms
				Pulse input:	10kpps, 100kpps, 200kpps, 500kpps, 1000kpps, 2000kpps, 4000kpps, 8000kpps
		Initial State		Low, High	
	Y device terminal			Outputs the ON/OFF states of General command 0 to General command F (Y10 to Y1F) as signals.	
	OUT terminal			Outputs the same signal as the one to be output from the external output block.	
	Parallel encoder block	Input Data Type		Pure binary, Gray code, BCD	
		Data Length		1 bit to 12 bits	
	SSI encoder block	Input Data Type		Pure binary, Gray code	
		Data Length		1 bit to 32 bits	
	Multi function counter block	Terminal		Input terminal, latch input terminal, event input terminal, output terminal, event output terminal, cam switch output terminal	
		Input signal event detection block		Combination of rise, fall, Low, and High	
		Latch event detection block		Rise, fall	
		Counter timer block	Type	Addition, subtraction, linear counter mode, ring counter mode, addition mode, preset counter function, latch counter function, internal clock function	
			Internal clock	25ns, 50ns, 0.1μs, 1μs, 10μs, 100μs, 1ms	
			Counting range	32-bit signed binary (-2147483648 to 2147483647) 32-bit unsigned binary (0 to 4294967295) 16-bit signed binary (-32768 to 32767) 16-bit unsigned binary (0 to 65535)	
		Compare block	Compare Value	Same as the counting range	
			Compare Mode	16-bit counter: =, >, <, ≥, ≤, <> 32-bit counter: =, >, <, ≥, ≤, <>	
		Cam switch block	Refreshing cycle	0.1μs	
			Number of steps	Up to 16 steps	
		Set/reset block		Uses the signal input to the Set terminal as a trigger to output the High fixed signal. Uses the signal input to the Reset terminal as a trigger to output the Low fixed signal.	
	Logical operation block	Logical operation type		AND, OR, XOR	
	External output block	Logic Select		Inverted, not inverted	
		Delay Time		None, 12.5ns × (1 to 64), 25ns × (1 to 64), 50ns × (1 to 64), 0.1μs × (1 to 64), 1μs × (1 to 64), 10μs × (1 to 64), 100μs × (1 to 64), 1ms × (1 to 64)	
		Error-time Output Mode		OFF, ON, HOLD	
	SI device terminal			Interrupt to a CPU module	

Item				Specifications	
				Differential	DC
Main functions that can be performed with the combination of main blocks	Pulse count	Count input signal	Phase	1-phase input (1 multiple/2 multiples), 2-phase input (1 multiple/2 multiples/4 multiples), CW/CCW	
		Counting speed	1 multiple	10kpps/100kpps/200kpps/ 500kpps/ 1Mpps/2Mpps	10kpps/100kpps/200kpps
			2 multiples	10kpps/100kpps/200kpps/500kpps/ 1Mpps/2Mpps/4Mpps	
			4 multiples	10kpps/100kpps/200kpps/500kpps/ 1Mpps/2Mpps/4Mpps/8Mpps	
		Counting range		Same as the counter timer block	
		Type		Addition, subtraction, linear counter mode, ring counter mode, addition mode, preset counter function, latch counter function	
		Minimum count pulse width (duty ratio: 50%)		1-phase input (1 multiple/2 multiples), CW/CCW 	1-phase input (1 multiple/2 multiples), CW/CCW 
				2-phase input (1 multiple/2 multiples/4 multiples) 	2-phase input (1 multiple/2 multiples/4 multiples) 
	Coincidence detection	Comparison range		32-bit signed binary value, 32-bit unsigned binary value, 16-bit signed binary value, 16-bit unsigned binary value	
		Comparison method		Setting value < count value, setting value = count value, setting value > count value	
		Interrupt		Coincidence detection interrupt function	
	Cam switch	Number of steps		Up to 16 steps/1 block	
	Highly-accurate pulse output			The ON/OFF timing can be adjusted in increments of 25ns at a minimum using trigger input as the starting point.	
	PWM output	Output frequency range		Max. 2MHz	Max. 200kHz
		Duty ratio		Any value (Can be set in increments of 25ns at a minimum.)	
	Ratio setting	Ratio setting range		Number of output pulses = (1 to 2147483647)/(1 to 2147483647) × Number of input pulses Note that a value obtained by dividing (1 to 2147483647) by (1 to 2147483647) should not exceed 1.	
	Pulse measurement	Measurement item		Pulse width (ON width, OFF width, from a rising edge to the next rising edge, from a falling edge to the next falling edge)	
		Measurement resolution		25ns	
	Electrical interface conversion			24VDC/5VDC/differential	
Processing time of the main hardware logic				Logical operation: Min. 87.5ns, Coincidence output: Min. 137.5ns, Cam switch: Min. 262.5ns	
Number of writes to a flash ROM				Up to 10000 times	
Internal current consumption (5VDC)				0.66A	
Applicable wire size		40-pin connector		0.088mm² to 0.3mm² (28 to 22 AWG) (When the A6CON1 or A6CON4 is used) 0.088mm² to 0.24mm² (28 to 24 AWG) (When the A6CON2 is used)	
External wiring connector (sold separately)				A6CON1, A6CON2, A6CON4	
Number of occupied I/O points				32 points (I/O assignment: Intelligent, 32 points)	

Item		Specifications	
		Differential	DC
Number of occupied modules		2	
External dimensions	Height	90mm	
	Width	45mm	
	Depth	95mm	
Weight		0.18kg	

*1 The basic blocks supplied by the configuration tool

Number of parameter settings

Set the parameters of the auto refresh setting for the flexible high-speed I/O control module so that the number of the set parameters including the number of the parameters for other intelligent function modules will not exceed the maximum number of parameters that can be set for the CPU module.

For the maximum number of parameters that can be set for the CPU module (maximum number of parameter settings), refer to the following.

MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection)

MELSEC-L CC-Link IE Field Network Head Module User's Manual

Number of parameters for the flexible high-speed I/O control module

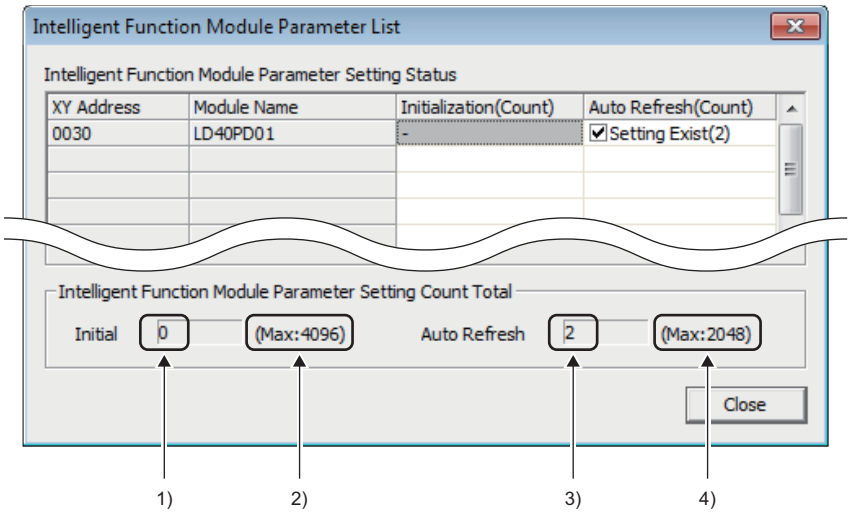
The following table lists the number of parameters that can be set per flexible high-speed I/O control module.

Target module	Initial setting	Auto refresh setting
LD40PD01	0	2 (maximum number of settings)

Check method

The number of parameter settings that are set for the intelligent function module and the maximum number of parameter settings can be checked with the following operation.

[Project window] ⇨ [Intelligent Function Module] ⇨ Right-click ⇨ [Intelligent Function Module Parameter List]



No.	Description
1)	Total number of initial setting parameters selected in the window
2)	Maximum number of initial setting parameter settings
3)	Total number of auto refresh setting parameters selected in the window
4)	Maximum number of auto refresh setting parameter settings

3.3 Function List

The following table lists the functions of the flexible high-speed I/O control module.

Item	Description	Reference
Hardware logic control function	Users can create the hardware logic to perform a desired control with the configuration tool.	☞ Page 103 CREATING A HARDWARE LOGIC
Error history function	The errors that occurred in the flexible high-speed I/O control module are stored in the buffer memory as error history. Up to 16 errors can be stored.	☞ Page 58 Error History Function
Module error collection function	The errors that occurred in the flexible high-speed I/O control module are collected in the CPU module.	☞ Page 61 Module Error Collection Function
Error clear function	When an error has occurred, the error can be cleared from the system monitor.	☞ Page 62 Error Clear Function

3.4 List of I/O Signals

The following table lists the I/O signals of the flexible high-speed I/O control module to the CPU module.
For details on the I/O signals, refer to the following.
☞ Page 240 Details of I/O Signals

Input (Signal direction: CPU module ← Flexible high-speed I/O control module)		Output (Signal direction: CPU module → Flexible high-speed I/O control module)	
Device No.	**Signal name**	**Device No.**	**Signal name**
X0	Module ready	Y0	Use prohibited
X1	Use prohibited	Y1	Use prohibited
X2	Use prohibited	Y2	Use prohibited
X3	Operating condition settings batch-reset complete flag	Y3	Operating condition settings batch-reset command
X4	Hardware logic control flag	Y4	Hardware logic control start request
X5	Use prohibited	Y5	Hardware logic control stop request
X6	Use prohibited	Y6	Hardware logic control stop signal at disconnection
X7	Hardware logic control stop flag at disconnection	Y7	Hardware logic control stop flag clear request at disconnection
X8	Use prohibited	Y8	Use prohibited
X9	Use prohibited	Y9	Use prohibited
XA	Use prohibited	YA	Use prohibited
XB	Use prohibited	YB	Use prohibited
XC	Use prohibited	YC	Use prohibited
XD	Use prohibited	YD	Use prohibited
XE	Use prohibited	YE	Use prohibited
XF	Error flag	YF	Error clear request
X10	IN 0	Y10	General command 0
X11	IN 1	Y11	General command 1
X12	IN 2	Y12	General command 2
X13	IN 3	Y13	General command 3
X14	IN 4	Y14	General command 4
X15	IN 5	Y15	General command 5
X16	IN 6	Y16	General command 6
X17	IN 7	Y17	General command 7
X18	IN 8	Y18	General command 8
X19	IN 9	Y19	General command 9
X1A	IN A	Y1A	General command A
X1B	IN B	Y1B	General command B
X1C	Use prohibited	Y1C	General command C
X1D	Use prohibited	Y1D	General command D
X1E	Use prohibited	Y1E	General command E
X1F	Use prohibited	Y1F	General command F

Point

- The I/O numbers (X/Y) listed above are shown on the assumption that the start I/O number of the flexible high-speed I/O control module is set to 0.
- The use prohibited signals listed above are used by the system and are not available for users. If a user uses these signals (turning off and on), the performance of the flexible high-speed I/O control module is not guaranteed.

3.5 List of Buffer Memory Addresses

The following table lists the buffer memory addresses of the flexible high-speed I/O control module.
For details on the buffer memory areas, refer to the following.
☞ Page 247 Details of Buffer Memory Areas

Point

Do not write any data to the system area and write-protect area of the buffer memory. If data is written to these areas, a malfunction may occur.

Address (decimal)	Address (hexadecimal)	Name				Default value*1	Read/write*2
0 to 99	0H to 63H	System area				—	—
100	64H	Latest error code				0	R
101	65H	System area				—	—
102	66H	Cumulative number of write accesses to a flash ROM				0	R
103	67H						
104 to 109	68H to 6DH	System area				—	—
110, 111	6EH, 6FH	SSI receive data monitor 0				0	R
112, 113	70H, 71H	System area				—	—
114, 115	72H, 73H	SSI receive data monitor 1				0	R
116 to 999	74H to 3E7H	System area				—	—
1000 to 1029	3E8H to 405H	Hardware logic area (High speed area)				0	R/W
1030 to 1099	406H to 44BH	Hardware logic area (Low speed area)				0	R/W
1100 to 7999	44CH to 1F3FH	System area				—	—
8000	1F40H	Latest address of error history				0	R
8001	1F41H	System area				—	—
8002	1F42H	Clear setting of error history				0	R/W
8003 to 8009	1F43H to 1F49H	System area				—	—
8010	1F4AH	Error history No. 1	Error code			0	R
8011	1F4BH		Error time	First two digits of the year	Last two digits of the year		
8012	1F4CH			Month	Day		
8013	1F4DH			Hour	Minute		
8014	1F4EH			Second	Day of the week		
8015 to 8019	1F4FH to 1F53H	System area				—	—
8020 to 8024	1F54H to 1F58H	Error history No. 2	Same with error history No. 1			0	R
8025 to 8029	1F59H to 1F5DH	System area				—	—
8030 to 8034	1F5EH to 1F62H	Error history No. 3	Same with error history No. 1			0	R
8035 to 8039	1F63H to 1F67H	System area				—	—
8040 to 8044	1F68H to 1F6CH	Error history No. 4	Same with error history No. 1			0	R
8045 to 8049	1F6DH to 1F71H	System area				—	—
8050 to 8054	1F72H to 1F76H	Error history No. 5	Same with error history No. 1			0	R
8055 to 8059	1F77H to 1F7BH	System area				—	—
8060 to 8064	1F7CH to 1F80H	Error history No. 6	Same with error history No. 1			0	R
8065 to 8069	1F81H to 1F85H	System area				—	—
8070 to 8074	1F86H to 1F8AH	Error history No. 7	Same with error history No. 1			0	R
8075 to 8079	1F8BH to 1F8FH	System area				—	—
8080 to 8084	1F90H to 1F94H	Error history No. 8	Same with error history No. 1			0	R
8085 to 8089	1F95H to 1F99H	System area				—	—
8090 to 8094	1F9AH to 1F9EH	Error history No. 9	Same with error history No. 1			0	R
8095 to 8099	1F9FH to 1FA3H	System area				—	—
8100 to 8104	1FA4H to 1FA8H	Error history No. 10	Same with error history No. 1			0	R

Address (decimal)	Address (hexadecimal)	Name		Default value*1	Read/write*2
8105 to 8109	1FA9H to 1FADH	System area		—	—
8110 to 8114	1FAEH to 1FB2H	Error history No. 11	Same with error history No. 1	0	R
8115 to 8119	1FB3H to 1FB7H	System area		—	—
8120 to 8124	1FB8H to 1FBCH	Error history No. 12	Same with error history No. 1	0	R
8125 to 8129	1FBDH to 1FC1H	System area		—	—
8130 to 8134	1FC2H to 1FC6H	Error history No. 13	Same with error history No. 1	0	R
8135 to 8139	1FC7H to 1FCBH	System area		—	—
8140 to 8144	1FCCH to 1FD0H	Error history No. 14	Same with error history No. 1	0	R
8145 to 8149	1FD1H to 1FD5H	System area		—	—
8150 to 8154	1FD6H to 1FDAH	Error history No. 15	Same with error history No. 1	0	R
8155 to 8159	1FDBH to 1FDFH	System area		—	—
8160 to 8164	1FE0H to 1FE4H	Error history No. 16	Same with error history No. 1	0	R
8165 to 8169	1FE5H to 1FE9H	System area		—	—
8170	1FEAH	RUN LED status monitor		0	R
8171	1FEBH	ERR LED status monitor		0	R
8172 to 32767	1FECH to 7FFFH	System area		—	—

*1 The default value to be set after the power is turned on or the CPU module is reset

*2 Whether a value can be read/written from/to a program or not is indicated.
R: Readable
W: Writable

4 PROCEDURES BEFORE OPERATION

This chapter describes the procedures before operation.

1. Installing the module

Install the flexible high-speed I/O control module with a desired configuration.

☞ Page 34 Overall Configuration

2. External wiring

Wire external devices to the flexible high-speed I/O control module.

☞ Page 37 External Wiring

3. Creating a hardware logic

Create a hardware logic with the configuration tool.

☞ Page 63 FUNCTIONS OF THE CONFIGURATION TOOL

4. Programming and debugging

Create and check a program.

☞ Page 207 DISPLAY UNIT

MEMO

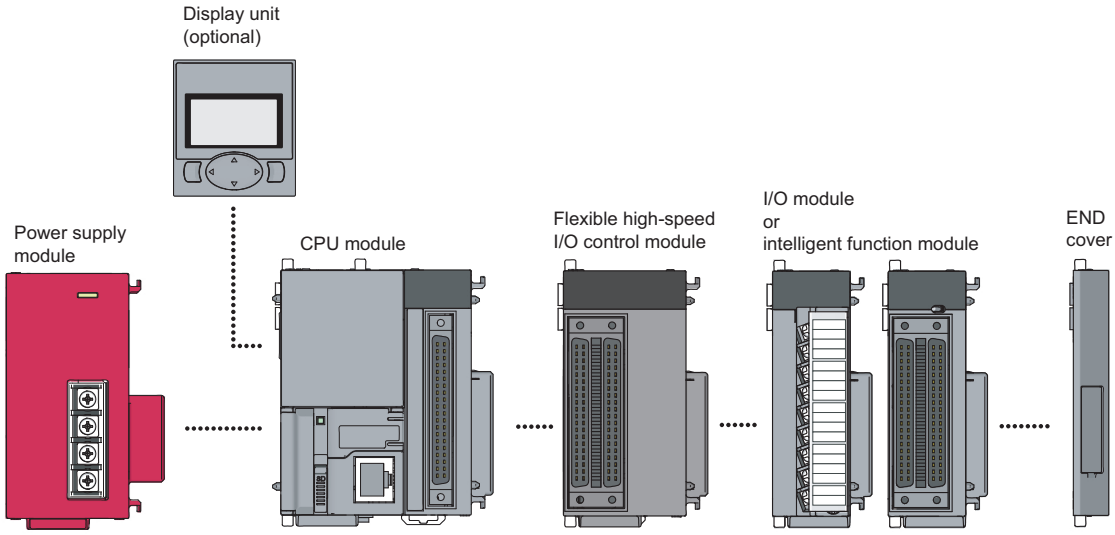
5 SYSTEM CONFIGURATION

This chapter describes the overall system configuration, number of connectable modules, and compatible software versions of the flexible high-speed I/O control module.

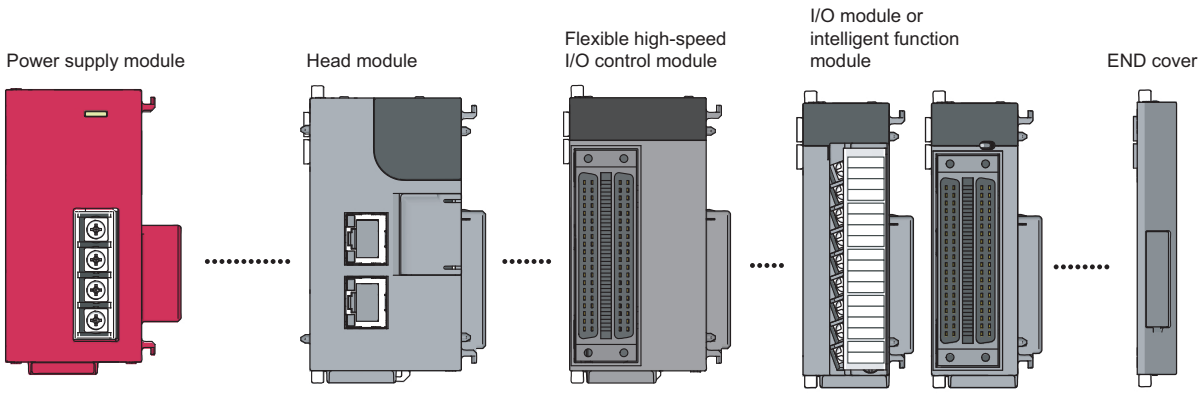
5.1 Overall Configuration

The following figure shows a system configuration example of when the flexible high-speed I/O control module is used.

When connected to the CPU module



When connected to the head module



5.2 Applicable System

Number of connectable modules

For the number of connectable modules, refer to the following.

MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection)
MELSEC-L CC-Link IE Field Network Head Module User's Manual

Compatible software version

The following table lists compatible software versions.

Software	Version
GX Works2	Version 1.535H or later
GX LogViewer	Version 1.46Y or later
Configuration tool	Version 1.000A or later

5.3 Restrictions When the Flexible High-Speed I/O Control Module Is Connected to the Head Module

This section describes the restrictions when the flexible high-speed I/O control module is connected to the head module.

- The intelligent function module interrupt cannot be used.

6 INSTALLATION AND EXTERNAL WIRING

This chapter describes the installation and external wiring of the flexible high-speed I/O control module.

6.1 Installation Environment and Installation Position

For precautions for the installation environment and installation position, refer to the following.

MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection)
MELSEC-L CC-Link IE Field Network Head Module User's Manual

6.2 External Wiring

This section describes wiring of encoders and controllers to the flexible high-speed I/O control module.

External wiring precautions

To obtain the maximum performance from the functions of the flexible high-speed I/O control module and improve the system reliability, an external wiring with high durability against noise is required.
This section describes the precautions for wiring of encoders and controllers.

Wiring

- Different terminals are prepared depending on the voltage of the signal to be input. Connecting to a terminal with an incorrect voltage may cause a malfunction of the module or failure of the connected devices.
- In 1-phase pulse input, always connect a pulse input cable on the phase A side.
- Install a fuse for each external terminal to prevent the external devices or module from being burnt out or damaged if a load shorts in an output circuit. The following fuses have been tested by Mitsubishi.

Fuse model name	Rated current	Contact
312.750	0.75A	Littelfuse www.littelfuse.com
216.800	0.8A	

Connector for external devices

- Connectors for external devices must be soldered or crimped properly. A poor soldering or crimping may result in a malfunction.
- Securely connect the connectors for external devices to the connectors of the flexible high-speed I/O control module, and securely tighten the two screws.
- When disconnecting a cable from the flexible high-speed I/O control module, do not pull the cable holding the cable part. Remove a cable supporting the connector part of the cable by hand. Pulling the cable being connected to the flexible high-speed I/O control module can cause a malfunction. In addition, a damage of the flexible high-speed I/O control module or cables can result.

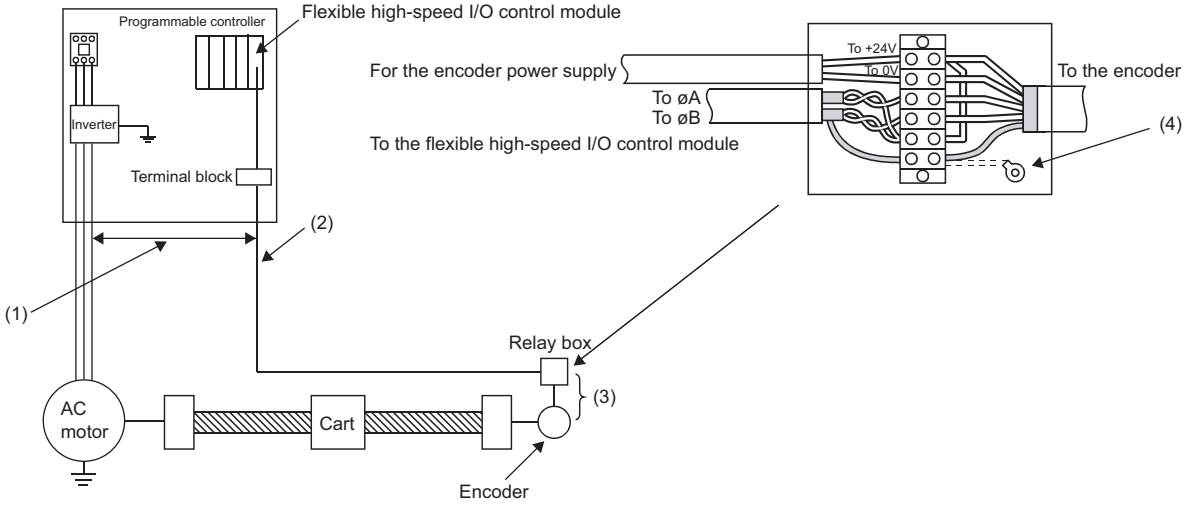
Measures to reduce noise

The flexible high-speed I/O control module may malfunction if pulse-like noise is input. Thus, take the following measures to reduce noise:

- Always use a shielded twisted pair cable.
- Arrange a shielded twisted pair cable keeping a distance of 150mm or more from the power cable, I/O cables, or other cables that cause much noise. Wire the shielded twisted pair cable in the minimum distance to the extent possible.
- Ground a shield wire on the encoder side (relay box). Always ground the FG and LG terminals to the protective ground conductor.
- Do not wire terminals that are not to be used. Doing so may result in malfunction due to noise.

Wiring example for measures to reduce noise

The following figure shows a wiring example of when the measures to reduce noise are reflected to the actual system.



(1) Keep a distance of 150mm or more from the I/O cables of high voltage devices including a relay and an inverter regardless of whether the devices are inside and outside the panel.

(2) For metal pipes, do not use solenoid valves and inductive loads together in a single pipe. When the distance from high voltage cables cannot be kept because of duct wiring or other factors, use shield wires such as CVVS for the high voltage cables.

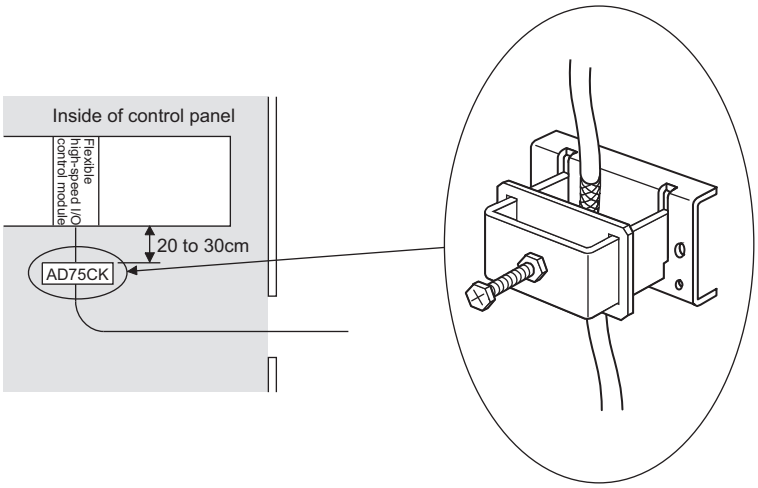
(3) Keep the minimum distance between an encoder and a relay box. When the distance between the flexible high-speed I/O control module and an encoder is long, a voltage drop may occur. Check that the voltage while the encoder is operating and the voltage while the encoder has stopped are within the rated voltage range of the encoder using a measuring instrument such as a tester on the terminal block of the relay box. When a voltage drop is large, use a thicker wire or use the 24DCV encoder that consumes less current.

(4) Connect the shield wires of the encoder and the shield wires of the shielded twisted pair cable inside the relay box. When the shield wires of the encoder in use have not been grounded in the encoder, ground them inside the relay box as shown above.

Compliance with the EMC and Low Voltage Directives

Take the following measures for compliance with the EMC and Low Voltage Directives.

- Always attach a ferrite core on the DC power supply cable to be connected to the flexible high-speed I/O control module and the one to be connected to a controller. Using the ESD-SR-250 ferrite core manufactured by NEC TOKIN Corporation is recommended.
- Install a DC power and the module in the same control panel.
- Use a shielded cable for the DC power when the DC power supply cable is extended out of the control panel.
- The length of the cables to be connected to the output section and external devices must be 2m or shorter for open collector output or 10m or shorter for differential output.
- Keep the length of the cables between the input section and the external devices to 30m or less.
- Use a shielded twisted pair cable and ground the shielded part of the cable to the control panel with the AD75CK cable clamp manufactured by Mitsubishi.



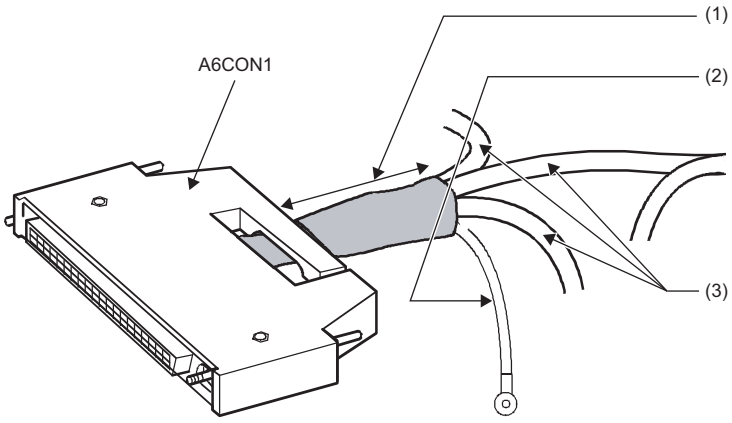
For details on the AD75CK, refer to the following.

📖 AD75CK-type Cable Clamping Instruction Manual

- Take the following measures to reduce noise when wiring connectors for external devices.

■Wiring to use a shielded cable

The following figure shows a wiring example for measures to reduce noise using the A6CON1.

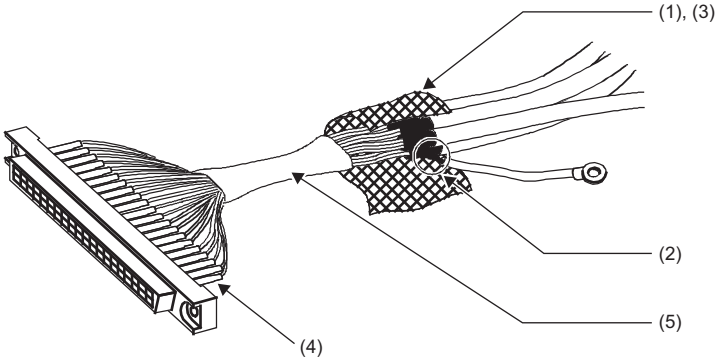


(1) Shorten the distance between the connector and shielded cable as far as possible.

(2) Ground a FG cable of 2㎟ or thicker in the minimum distance. Securely ground the cable in the control panel on the module side.

(3) Shielded cables

■Example of noise reduction measures taken to shielded cables



(1) Remove the jacket of each shielded cable.

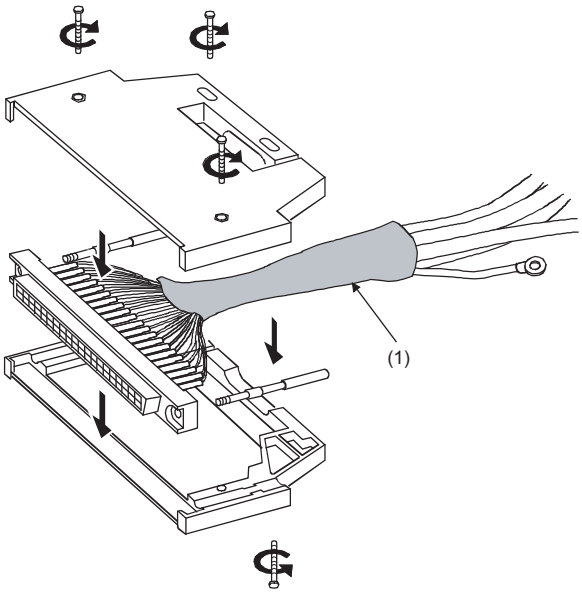
(2) Take out a shield from a shielded cable and solder it on the FG wire.

(3) Connect a shield of each shielded cable with a conductive tape.

(4) Cover a connector pin with a heat-shrinkable insulation tube to protect signal wires. If signal wires are bared, the module may be affected by static electricity and malfunction.

(5) Cover the signal wires with an insulating tape.

■Assembling the A6CON1



(1) Cover the cables on which a conductive tape has been applied with a heat-shrinkable tube.

Connector for external devices

Precautions

- Tighten the connector screws within the specified tightening torque range.

Screw	Tightening torque range
Connector screw (M2.6)	0.20 to 0.29N·m

- Use copper wires having temperature rating of 75℃ or more for the connectors.
- Use UL listed connectors if necessary for UL compliance.

Applicable connectors

Prepare connectors for external devices to be used with the flexible high-speed I/O control module by users.
The following table lists the applicable connectors, and the reference product of a crimping tool.

■40-pin connector

Type	Model	Applicable wire size
Soldering type connector (Straight type)	A6CON1*1	0.088 to 0.3mm^2 (28 to 22 AWG) (Stranded wire)
Crimping type connector (Straight type)	A6CON2	0.088 to 0.24mm^2 (28 to 24 AWG) (Stranded wire)
Soldering type connector (Dual purpose (straight/oblique) type)	A6CON4*1	0.088 to 0.3mm^2 (28 to 22 AWG) (Stranded wire)

*1 When using 40 connectors, use wires whose sheath outside diameter is 1.3mm or less.
Select the wire applicable to the current value to be used.

Point

The A6CON3 (IDC type connector (Straight type)) cannot be used.

■40-pin connector crimping tool

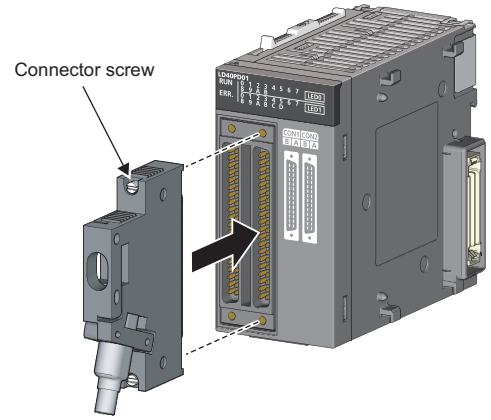
Type	Model	Contact
Crimping tool	FCN-363T-T005/H	FUJITSU COMPONENT LIMITED www.fcl.fujitsu.com/en

For how to wire connectors and how to use the crimping tool, contact FUJITSU COMPONENT LIMITED.

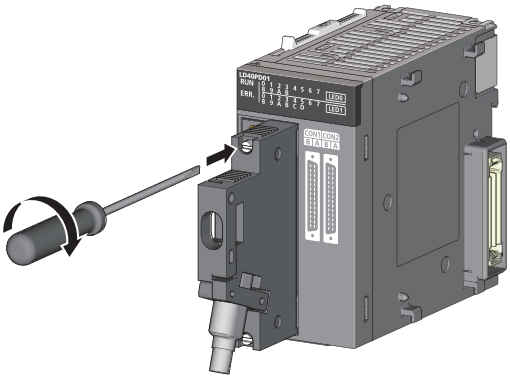
Wiring method

For the wiring method, refer to the following.
MELSEC-L CPU Module User's Manual (Hardware Design, Maintenance and Inspection)

Connection procedure

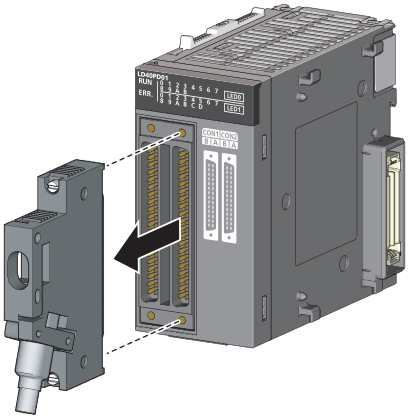


1. Plug the connector into a slot on the flexible high-speed I/O control module.



2. Tighten the two connector screws (M2.6).

Removal procedure



1. Loosen the two connector screws and pull out the connector from the module.

Interface with external devices

The following table shows the interface of the flexible high-speed I/O control module with external devices.

Electrical specifications of external I/O signals

■External input signal

The following table shows the input specifications of the flexible high-speed I/O control module.

Signal name	Operation	Input voltage (Guaranteed value)	Operating current	Response time*1
24VDC input	On	21.6 to 26.4V	4 to 6mA	1μs
	Off	5V or less	1.0mA or less	
5VDC input	On	4.5 to 5.5V	4 to 8mA	1μs
	Off	2V or less	1.0mA or less	
Differential input	—	Equivalent to AM26C32	—	1μs

*1 When the filter time has been set to 0μs

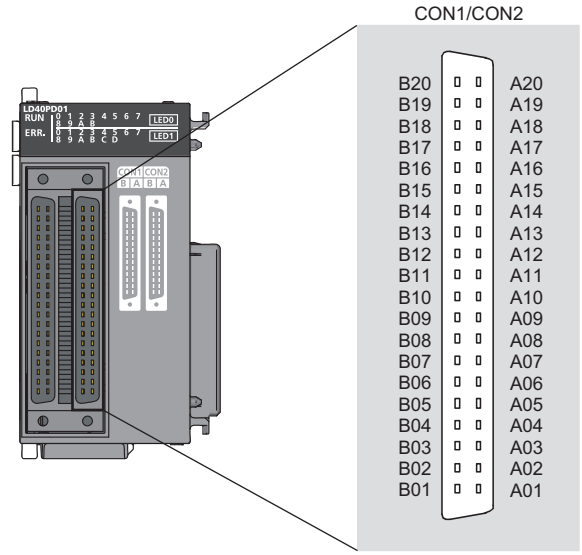
■External output signal

The following table shows the output specifications of the flexible high-speed I/O control module.

Signal name	Item		Description
DC output	Operating load voltage		4.75 to 30VDC
	Maximum load current		0.1A/point
	Maximum voltage drop at ON		0.5V
	Response time	OFF→ON	1μs or less (Rated load, resistive load)
		ON→OFF	1μs or less (Rated load, resistive load)
Differential output	Operating load voltage		Equivalent to AM26C31
	Maximum load current		
	Maximum voltage drop at ON		
	Response time		1μs or less

Signal layout of a connector for external devices

The following shows the signal layout of a connector for external devices of the flexible high-speed I/O control module.



Pin No.	CON1		CON2	
	B	A	B	A
20	NC	NC	NC	NC
19	IN 0_24V	IN 0_5V	IN 6_24V	IN 6_5V
18	IN 0_DIF	IN 0_COM	IN 6_DIF	IN 6_COM
17	IN 1_24V	IN 1_5V	IN 7_24V	IN 7_5V
16	IN 1_DIF	IN 1_COM	IN 7_DIF	IN 7_COM
15	IN 2_24V	IN 2_5V	IN 8_24V	IN 8_5V
14	IN 2_DIF	IN 2_COM	IN 8_DIF	IN 8_COM
13	IN 3_24V	IN 3_5V	IN 9_24V	IN 9_5V
12	IN 3_DIF	IN 3_COM	IN 9_DIF	IN 9_COM
11	IN 4_24V	IN 4_5V	IN A_24V	IN A_5V
10	IN 4_DIF	IN 4_COM	IN A_DIF	IN A_COM
9	IN 5_24V	IN 5_5V	IN B_24V	IN B_5V
8	IN 5_DIF	IN 5_COM	IN B_DIF	IN B_COM
7	OUT 0	OUT 1	OUT 4	OUT 5
6	OUT 2	OUT 3	OUT 6	OUT 7
5	OUT 0-3_COM	OUT_DIF_GND	OUT 4-7_COM	OUT_DIF_GND
4	OUT 0_DIF+	OUT 0_DIF-	OUT 3_DIF+	OUT 3_DIF-
3	OUT 1_DIF+	OUT 1_DIF-	OUT 4_DIF+	OUT 4_DIF-
2	OUT 2_DIF+	OUT 2_DIF-	OUT 5_DIF+	OUT 5_DIF-
1	NC	NC	NC	NC

■List of input signals

The following table lists the input signals of the flexible high-speed I/O control module.

Pin No.	CON1		CON2		Description
	Symbol	Signal name	Symbol	Signal name	
B20	NC	NC	NC	NC	Empty pin
A20	NC	NC	NC	NC	
B19	IN 0_24V	High-speed input 0 24VDC	IN 6_24V	High-speed input 6 24VDC	Inputs the + (plus) side. (common for 5VDC/ 24VDC/differential)
A19	IN 0_5V	High-speed input 0 5VDC	IN 6_5V	High-speed input 6 5VDC	
B18	IN 0_DIF	High-speed input 0 differential	IN 6_DIF	High-speed input 6 differential	
A18	IN 0_COM	High-speed input 0 common	IN 6_COM	High-speed input 6 common	Inputs the - (minus) side.
B17	IN 1_24V	High-speed input 1 24VDC	IN 7_24V	High-speed input 7 24VDC	Inputs the + (plus) side. (common for 5VDC/ 24VDC/differential)
A17	IN 1_5V	High-speed input 1 5VDC	IN 7_5V	High-speed input 7 5VDC	
B16	IN 1_DIF	High-speed input 1 differential	IN 7_DIF	High-speed input 7 differential	
A16	IN 1_COM	High-speed input 1 common	IN 7_COM	High-speed input 7 common	Inputs the - (minus) side.
B15	IN 2_24V	High-speed input 2 24VDC	IN 8_24V	High-speed input 8 24VDC	Inputs the + (plus) side. (common for 5VDC/ 24VDC/differential)
A15	IN 2_5V	High-speed input 2 5VDC	IN 8_5V	High-speed input 8 5VDC	
B14	IN 2_DIF	High-speed input 2 differential	IN 8_DIF	High-speed input 8 differential	
A14	IN 2_COM	High-speed input 2 common	IN 8_COM	High-speed input 8 common	Inputs the - (minus) side.
B13	IN 3_24V	High-speed input 3 24VDC	IN 9_24V	High-speed input 9 24VDC	Inputs the + (plus) side. (common for 5VDC/ 24VDC/differential)
A13	IN 3_5V	High-speed input 3 5VDC	IN 9_5V	High-speed input 9 5VDC	
B12	IN 3_DIF	High-speed input 3 differential	IN 9_DIF	High-speed input 9 differential	
A12	IN 3_COM	High-speed input 3 common	IN 9_COM	High-speed input 9 common	Inputs the - (minus) side.
B11	IN 4_24V	High-speed input 4 24VDC	IN A_24V	High-speed input A 24VDC	Inputs the + (plus) side. (common for 5VDC/ 24VDC/differential)
A11	IN 4_5V	High-speed input 4 5VDC	IN A_5V	High-speed input A 5VDC	
B10	IN 4_DIF	High-speed input 4 differential	IN A_DIF	High-speed input A differential	
A10	IN 4_COM	High-speed input 4 common	IN A_COM	High-speed input A common	Inputs the - (minus) side.
B9	IN 5_24V	High-speed input 5 24VDC	IN B_24V	High-speed input B 24VDC	Inputs the + (plus) side. (common for 5VDC/ 24VDC/differential)
A9	IN 5_5V	High-speed input 5 5VDC	IN B_5V	High-speed input B 5VDC	
B8	IN 5_DIF	High-speed input 5 differential	IN B_DIF	High-speed input B differential	
A8	IN 5_COM	High-speed input 5 common	IN B_COM	High-speed input B common	Inputs the - (minus) side.

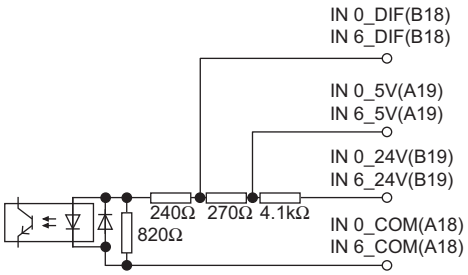
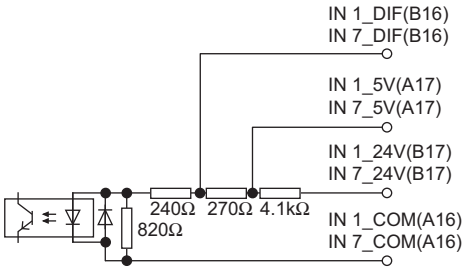
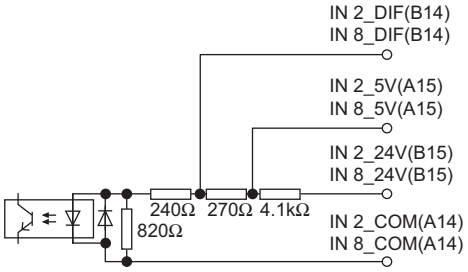
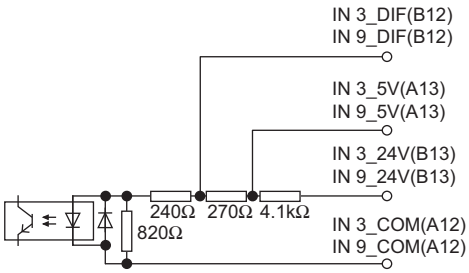
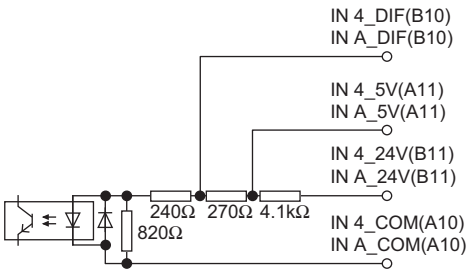
■List of output signals

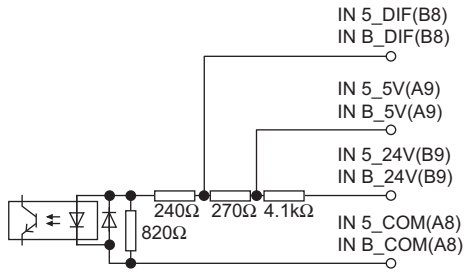
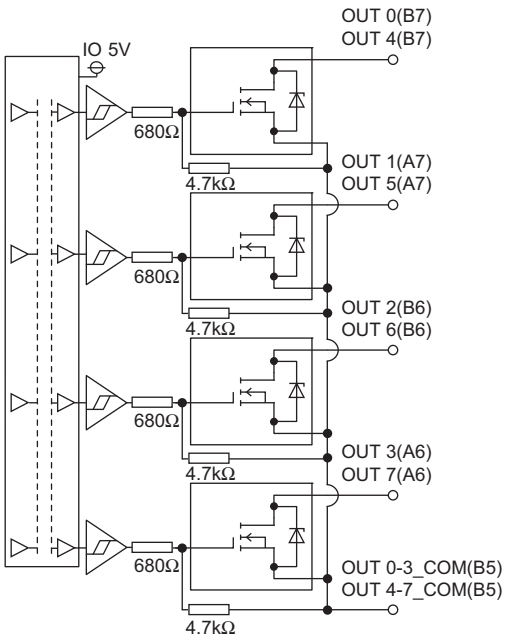
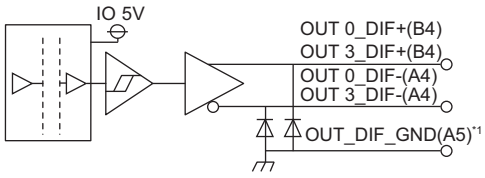
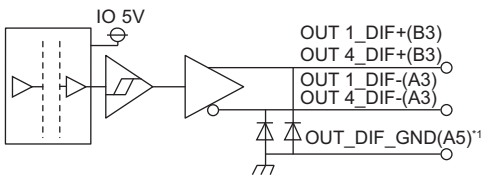
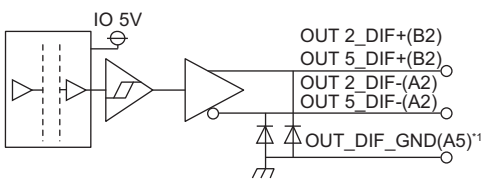
The following table lists the output signals of the flexible high-speed I/O control module.

Pin No.	CON1		CON2		Description
	Symbol	Signal name	Symbol	Signal name	
B7	OUT 0	High-speed output 0	OUT 4	High-speed output 4	5 to 24VDC output
A7	OUT 1	High-speed output 1	OUT 5	High-speed output 5	
B6	OUT 2	High-speed output 2	OUT 6	High-speed output 6	
A6	OUT 3	High-speed output 3	OUT 7	High-speed output 7	
B5	OUT 0-3_COM	High-speed output 0-3 common	OUT 4-7_COM	High-speed output 4-7 common	High-speed output common
A5	OUT_DIF_GND	High-speed output common	OUT_DIF_GND	High-speed output common	High-speed output differential ground
B4	OUT 0_DIF+	High-speed output 0 differential+	OUT 3_DIF+	High-speed output 3 differential+	Outputs the differential output + (plus) side.
A4	OUT 0_DIF-	High-speed output 0 differential-	OUT 3_DIF-	High-speed output 3 differential-	Outputs the differential output - (minus) sides
B3	OUT 1_DIF+	High-speed output 1 differential+	OUT 4_DIF+	High-speed output 4 differential+	Outputs the differential output + (plus) side.
A3	OUT 1_DIF-	High-speed output 1 differential-	OUT 4_DIF-	High-speed output 4 differential-	Outputs the differential output - (minus) sides
B2	OUT 2_DIF+	High-speed output 2 differential+	OUT 5_DIF+	High-speed output 5 differential+	Outputs the differential output + (plus) side.
A2	OUT 2_DIF-	High-speed output 2 differential-	OUT 5_DIF-	High-speed output 5 differential-	Outputs the differential output - (minus) sides
B1	NC	NC	NC	NC	Empty pin
A1	NC	NC	NC	NC	

Internal circuit of the interface for external devices

The following table lists the internal circuits of the interface for external devices of the flexible high-speed I/O control module.

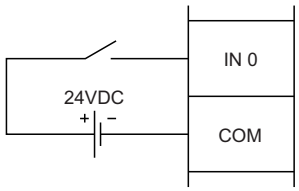
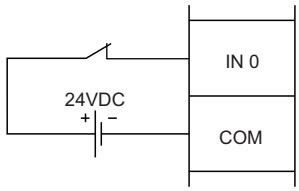
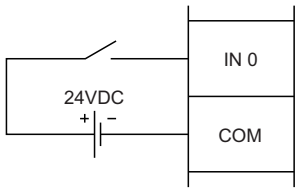
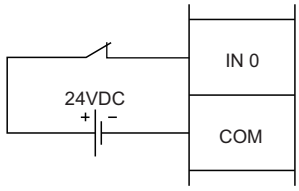
I/O classification	Internal circuit	Connector		Signal name	
		CON1	CON2	CON1	CON2
Input		B19	B19	High-speed input 0 24VDC	High-speed input 6 24VDC
		A19	A19	High-speed input 0 5VDC	High-speed input 6 5VDC
		B18	B18	High-speed input 0 differential	High-speed input 6 differential
		A18	A18	High-speed input 0 common	High-speed input 6 common
		B17	B17	High-speed input 1 24VDC	High-speed input 7 24VDC
		A17	A17	High-speed input 1 5VDC	High-speed input 7 5VDC
		B16	B16	High-speed input 1 differential	High-speed input 7 differential
		A16	A16	High-speed input 1 common	High-speed input 7 common
		B15	B15	High-speed input 2 24VDC	High-speed input 8 24VDC
		A15	A15	High-speed input 2 5VDC	High-speed input 8 5VDC
		B14	B14	High-speed input 2 differential	High-speed input 8 differential
		A14	A14	High-speed input 2 common	High-speed input 8 common
		B13	B13	High-speed input 3 24VDC	High-speed input 9 24VDC
		A13	A13	High-speed input 3 5VDC	High-speed input 9 5VDC
		B12	B12	High-speed input 3 differential	High-speed input 9 differential
		A12	A12	High-speed input 3 common	High-speed input 9 common
		B11	B11	High-speed input 4 24VDC	High-speed input A 24VDC
		A11	A11	High-speed input 4 5VDC	High-speed input A 5VDC
		B10	B10	High-speed input 4 differential	High-speed input A differential
		A10	A10	High-speed input 4 common	High-speed input A common

I/O classification	Internal circuit	Connector		Signal name	
		CON1	CON2	CON1	CON2
Input		B9	B9	High-speed input 5 24VDC	High-speed input B 24VDC
		A9	A9	High-speed input 5 5VDC	High-speed input B 5VDC
		B8	B8	High-speed input 5 differential	High-speed input B differential
		A8	A8	High-speed input 5 common	High-speed input B common
Output		B7	B7	High-speed output 0	High-speed output 4
		A7	A7	High-speed output 1	High-speed output 5
		B6	B6	High-speed output 2	High-speed output 6
		A6	A6	High-speed output 3	High-speed output 7
		B5	B5	High-speed output 0-3 common	High-speed output 4-7 common
		A5	A5	High-speed output common*1	High-speed output common*1
		B4	B4	High-speed output 0 differential+	High-speed output 3 differential+
		A4	A4	High-speed output 0 differential-	High-speed output 3 differential-
		B3	B3	High-speed output 1 differential+	High-speed output 4 differential+
		A3	A3	High-speed output 1 differential-	High-speed output 4 differential-
		B2	B2	High-speed output 2 differential+	High-speed output 5 differential+
		A2	A2	High-speed output 2 differential-	High-speed output 5 differential-

*1 The high-speed output common (A5) is connected with the common wire of high-speed output 0 to 5 differential.

■Input signal status in the hardware logic (High/Low)

The input signal status (High/Low) in the hardware logic is determined depending on the input signals (ON/OFF) from external devices and logical selection.

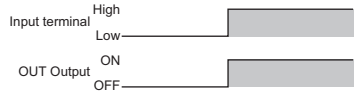
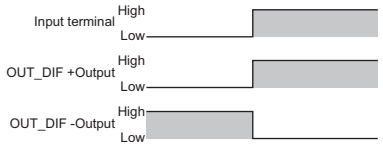
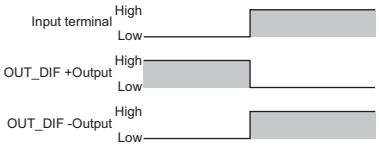
Logic selection*1	External wiring	High/Low state of the external input signal IN 0 observed from the flexible high-speed I/O control module*2
Not inverted	When a voltage is not applied (OFF) 	Low
	When a voltage is applied (ON) 	High
Inverted	When a voltage is not applied (OFF) 	High
	When a voltage is applied (ON) 	Low

*1 Set the logic selection with the parameters of the external input block. For details, refer to the following.
☞ Page 106 External input block

*2 The input signal status in the hardware logic is described as High and Low. For details, refer to the following.
☞ Page 104 Signal status name

■Status of an output signal to external devices (ON/OFF)

The status of an output signal to external devices (ON/OFF) is determined depending on the status of Input terminal of the external output block (High/Low) and logic selection.

Output type	Logic selection*1*2	
	Not inverted	Inverted
DC		
Differential		

*1 Set the logic selection with the parameters of the external output block. For details, refer to the following.
☞ Page 123 External output block

*2 The output signal status in the hardware logic is described as High and Low. For details, refer to the following.
☞ Page 104 Signal status name

Connectable encoders

The following tables list encoders that can be connected to the flexible high-speed I/O control module.

- Encoders with the following counting methods

Counting method	Condition
Incremental method	—
Absolute method	Encoders with the following specifications can be connected. • Parallel interface • Resolution: 1 to 12 bits • The absolute code is in pure binary, Gray code, or BCD.
	Encoders with the following specifications can be connected. • SSI (Synchronous Serial Interface) • Resolution: 1 to 32 bits • The absolute code is in pure binary or Gray code.

- Encoders of the following output type

Output type	Condition
Open collector output type	Check if the output voltage of the encoder meets the specifications of the flexible high-speed I/O control module.
Line driver output type (equivalent to AM26LS31)	
CMOS level voltage output type	

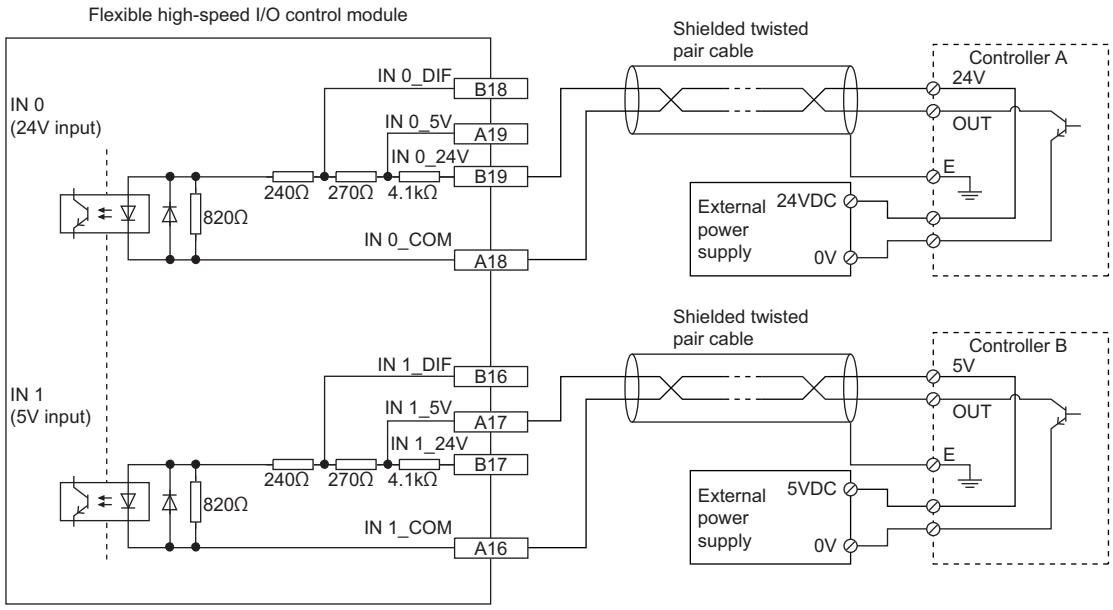
Restriction

TTL level voltage output type encoders cannot be used with the flexible high-speed I/O control module.

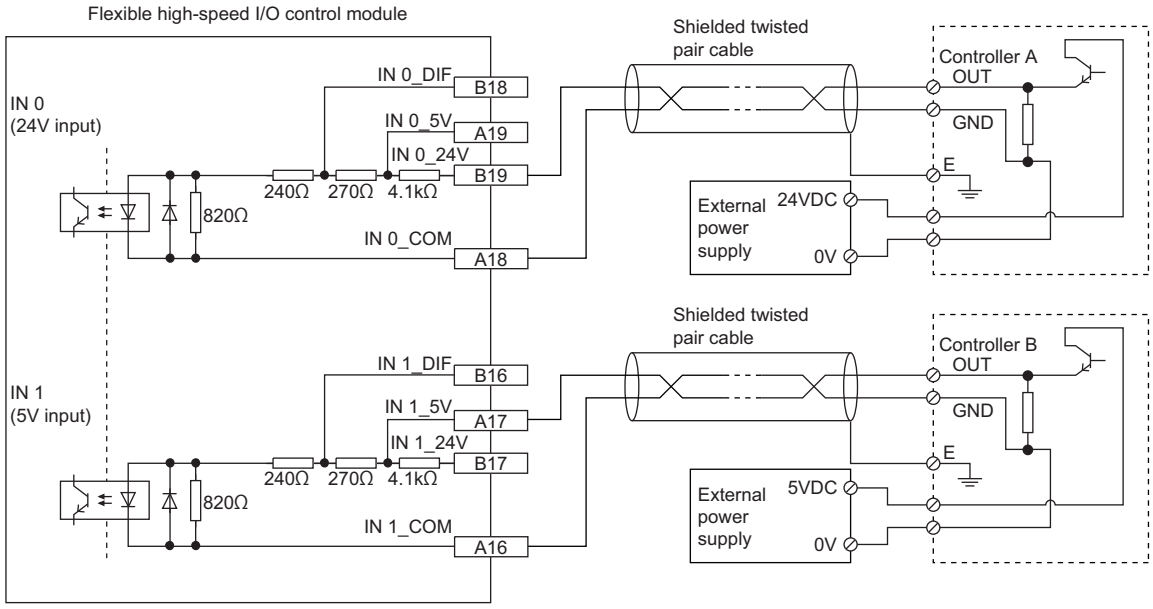
6.3 Examples of Wiring Between a Controller and External Input Terminals

This section shows examples of wiring between a controller and external input terminals.

Example of external wiring with a controller (Sync load type)



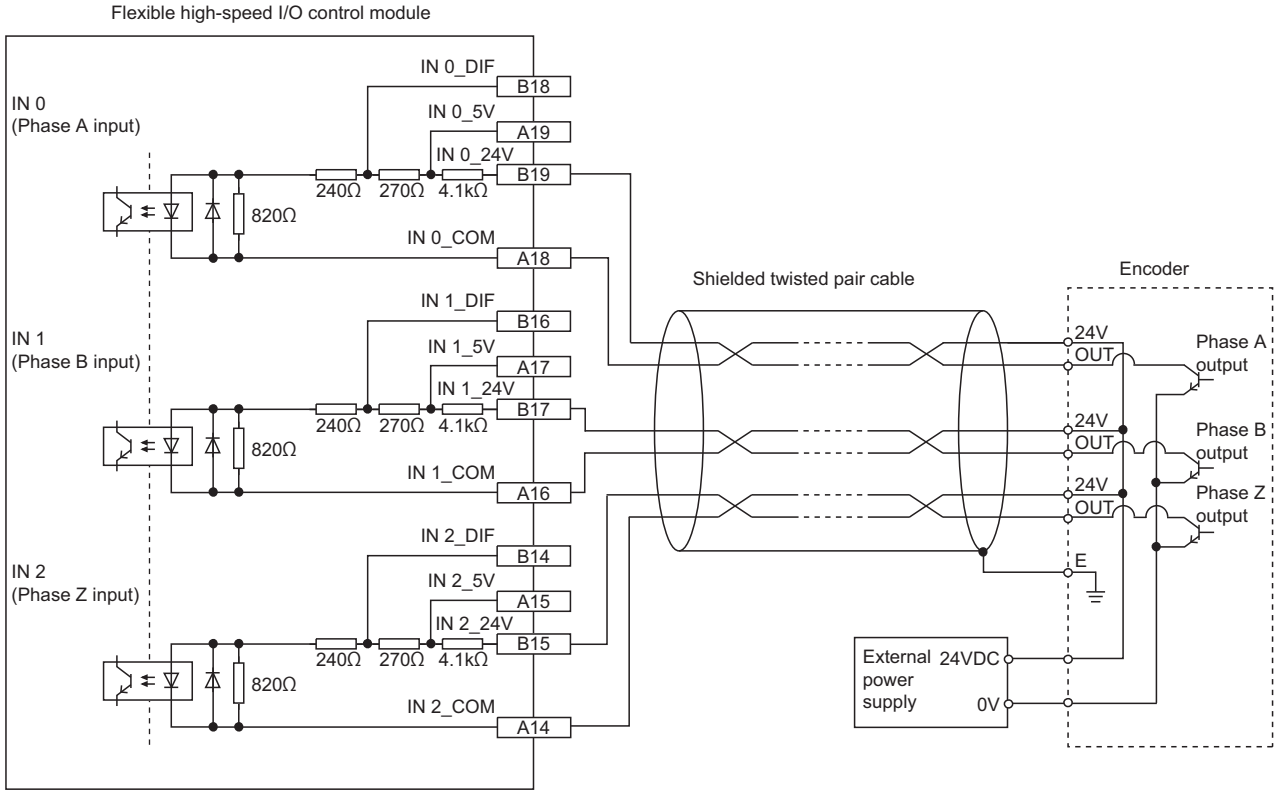
Example of external wiring with a controller (Source load type)



6.4 Example of External Wiring Between the Flexible High-speed I/O Control Module and an Encoder

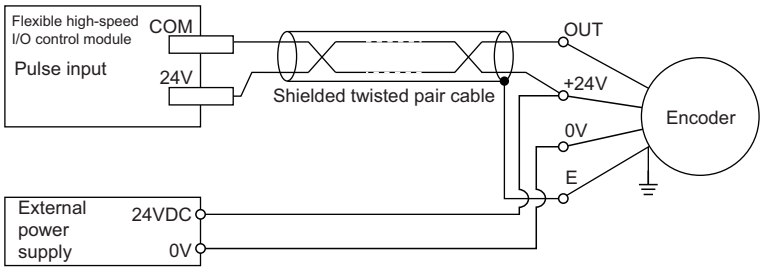
This section shows an example of external wiring between the flexible high-speed I/O control module and an encoder.

Example of external wiring with an open collector output type encoder (24VDC)

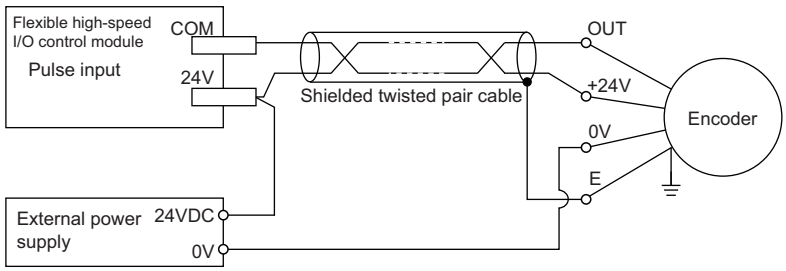


Point

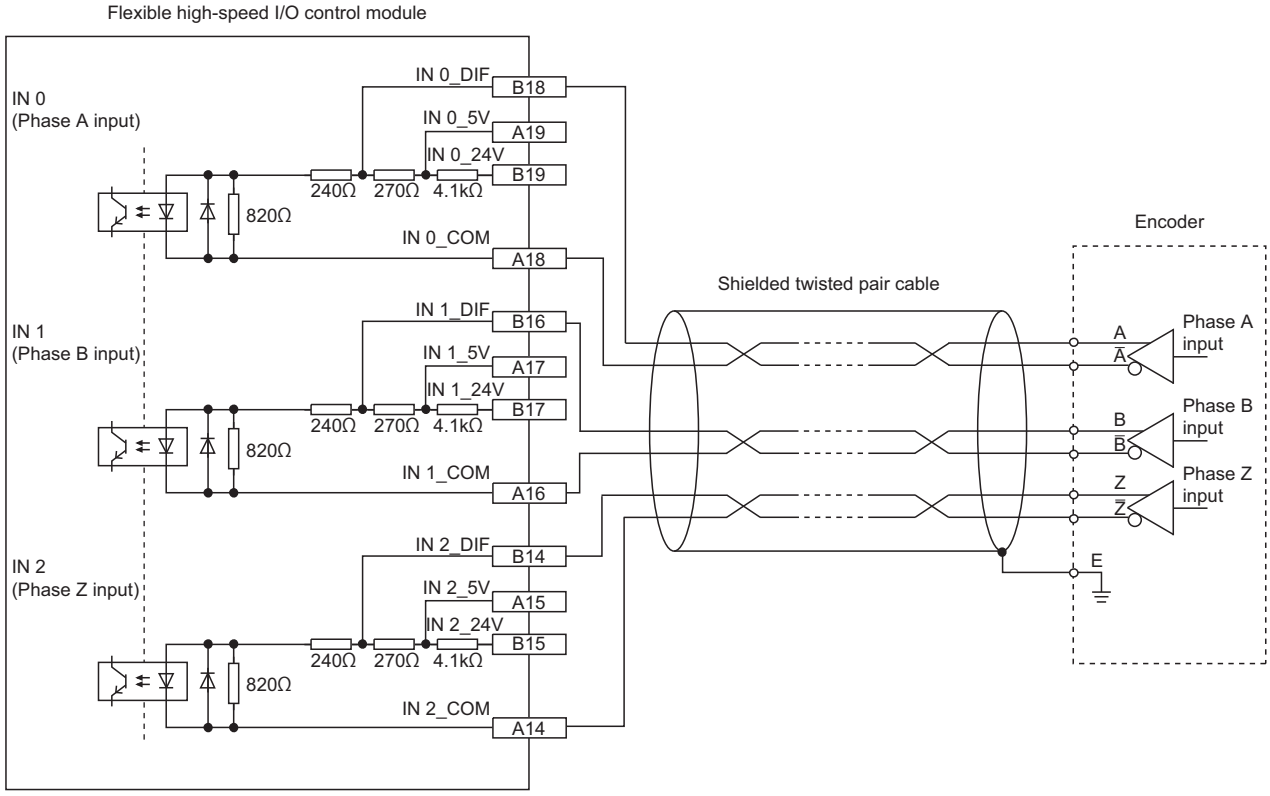
- For the wiring between the flexible high-speed I/O control module and an encoder, separate the power supply cables and signal wires.



- Do not wire the module and an encoder as shown in the figure below. Because a current flows through a shielded twisted pair cable in a single direction and the canceling effect disappears, the module is easy to be affected by electromagnetic induction.

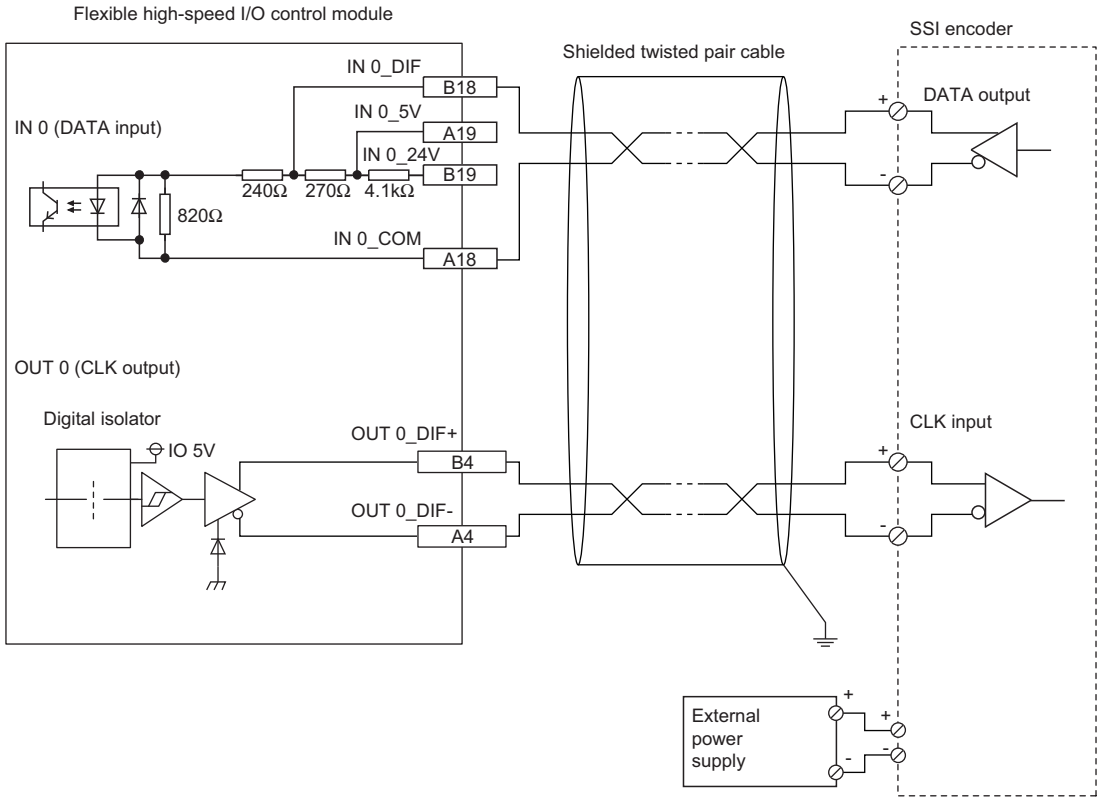


Example of external wiring with a line driver (equivalent to AM26LS31) encoder



Example of external wiring with the SSI encoder (serial communication)

Connect the flexible high-speed I/O control module to the SSI encoder using a shielded twisted pair cable of 0.2mm^2 or thicker (24 AWG or larger). Make sure to check the SSI encoder specifications.
In addition, separately prepare an external power supply for the SSI encoder.



- Connect the DATA input to any of IN 0 to IN B.
- Connect the CLK output to OUT 0_DIF for SSI_Encoder_0, and to OUT 1_DIF for SSI_Encoder_1.

Relation between transmission speed and maximum cable length (reference value)

Transmission speed	Maximum cable length
100kHz	400m
200kHz	190m
300kHz	120m
400kHz	80m
500kHz	60m
1MHz	25m
1.5MHz	10m
2MHz	5m

The maximum cable length described in the above is a reference value. Depending on the response performance of the SSI encoder to be connected, the maximum cable length may become shorter than the above description because a response delay occurs.
Therefore, check the operation using an actual encoder to be connected, and use the module.

Point

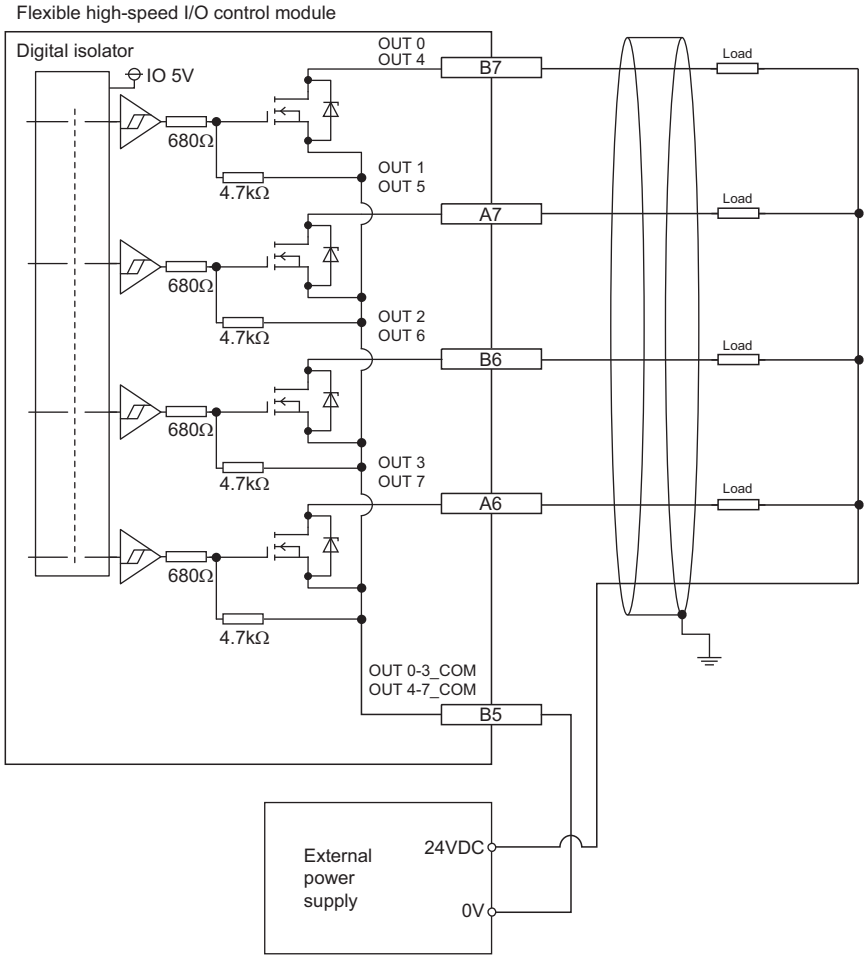
If the cable longer than the maximum length described above is used, the module becomes following states.

- An encoder value is fixed to an incorrect value and the module does not count the value correctly.
- An encoder value fluctuates and the module does not count the value correctly.
- An encoder value cannot be read and the module does not count the value correctly.

6.5 Example of External Wiring with External Output Terminals

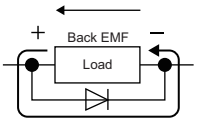
This section shows an example of external wiring with external output terminals.

Example of external wiring with output terminals (Sink output type)

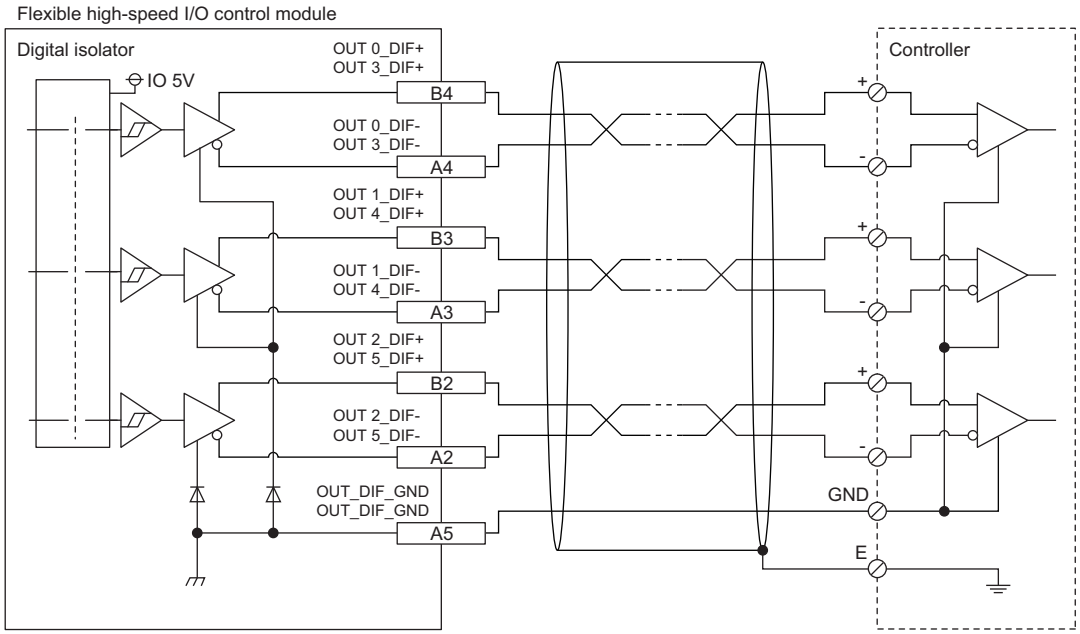


Point

When connecting an inductive load, connect a diode in parallel with the load to prevent back EMF from being generated to protect output elements.



Example of external wiring with differential receivers (Differential output type)



Point

When connecting differential output terminals to differential receivers of the drive unit, connect the high-speed output common (OUT_DIF_GND) and the common terminals of the differential receivers of the drive unit. When the high-speed output common terminals are not connected, the potential difference will be generated between the high-speed output common (OUT_DIF_GND) and the common terminals of the differential receivers of the drive unit, damaging the module or causing a malfunction.

7 FUNCTIONS

This chapter describes the details on the functions that can be used in the flexible high-speed I/O control module and their setting methods.

7.1 Hardware Logic Control Function

Users can create the hardware logic to perform a desired control with the configuration tool.
For details, refer to the following.
☞ Page 103 CREATING A HARDWARE LOGIC

7.2 Error History Function

The errors that occurred in the flexible high-speed I/O control module are stored in the buffer memory areas (Un\G8010 to Un\G8169) as error history.
Up to 16 errors can be stored.

Processing of the error history function

The error code and error time of each error are stored in Error history No. 1 (start address: Un\G8010) and sequentially thereafter. The error time is stored as shown below.

Ex.
The following shows the case of Error history No. 1.

	b15 to b8	b7 to b0
Un\G8010	Error code	
Un\G8011	First two digits of the year	Last two digits of the year
Un\G8012	Month	Day
Un\G8013	Hour	Minute
Un\G8014	Second	Day of the week
Un\G8015 to Un\G8019	System area	

Item	Description	Storage example*1
First two digits of the year/last two digits of the year	Stored as a BCD code.	2015H
Month/day		0424H
Hour/minute		1035H
Second		40H
Day of the week	For each day of the week, one of the following values is stored as a BCD code. Sunday: 0H, Monday: 1H, Tuesday: 2H, Wednesday: 3H, Thursday: 4H, Friday: 5H, Saturday: 6H	5H

*1 Value of when an error occurred at 10:35:40 on Friday, April 24th, 2015

Clearing the error history

The error history can be cleared with one of the following methods.

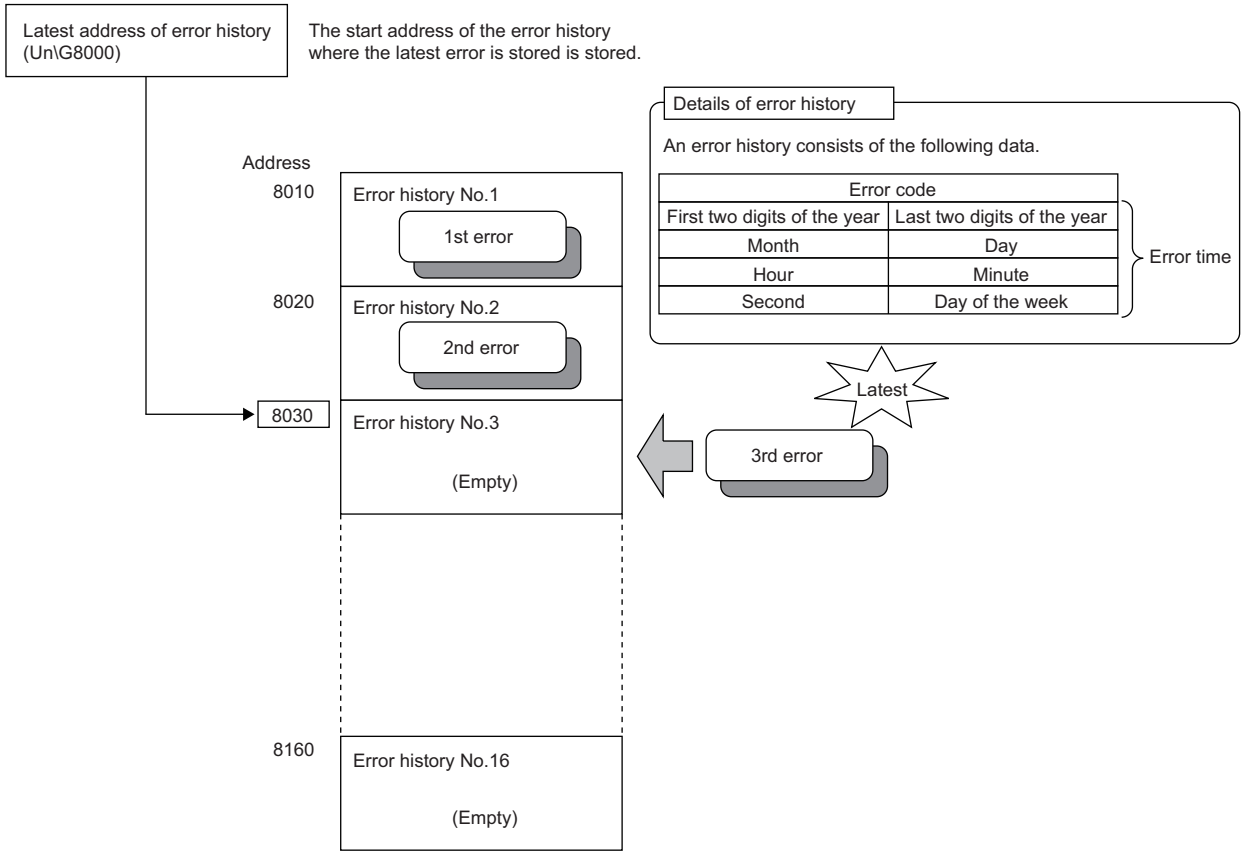
- Turning off the power
- Resetting the CPU module
- Setting Clear setting of error history (Un\G8002) to Clear the history (1) and turning on and off Error clear request (YF)

Checking the error history

The start address of the error history where the latest error has been stored can be checked with Latest address of error history (Un\G8000).

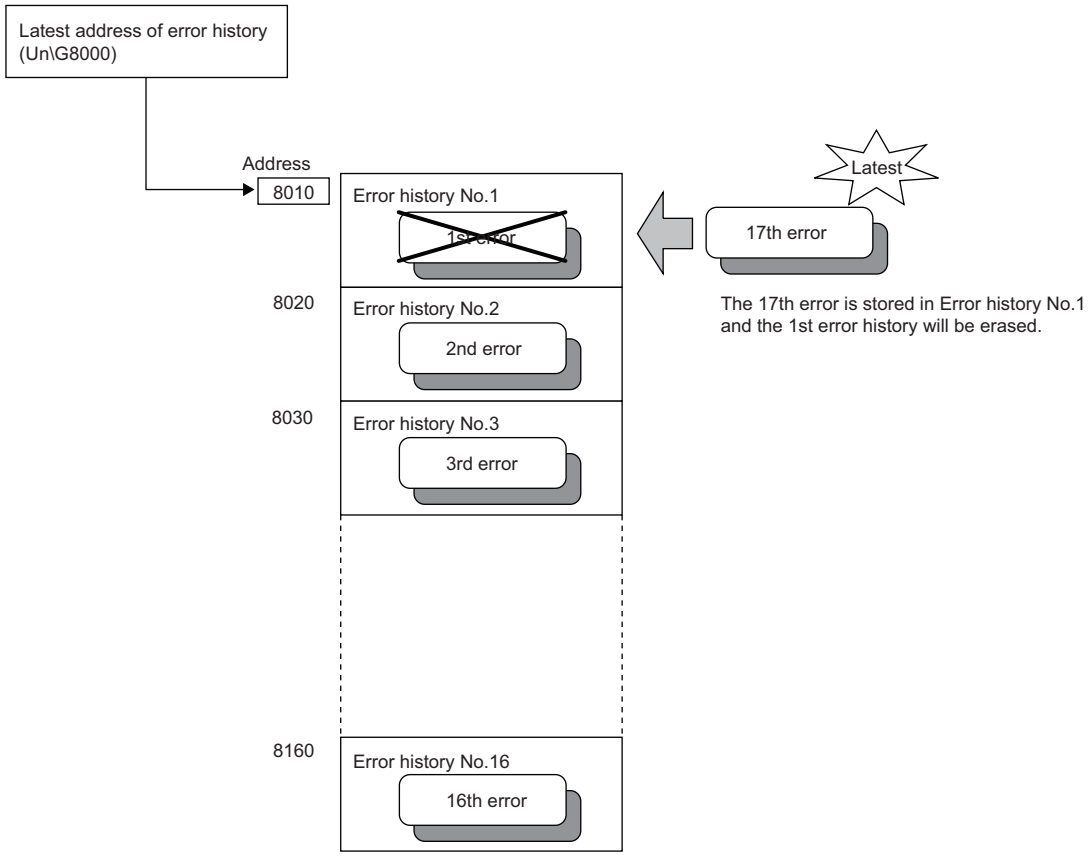
Ex.

The following shows the case in which the third error has occurred. The third error is stored in Error history No. 3 and 8030 (start address of Error history No.3) is stored in Latest address of error history (Un\G8000).



Ex.

The following shows the case in which the 17th error has occurred. The 17th error is stored in Error history No. 1 and 8010 (start address of Error history No. 1) is overwritten to Latest address of error history (Un\G8000).

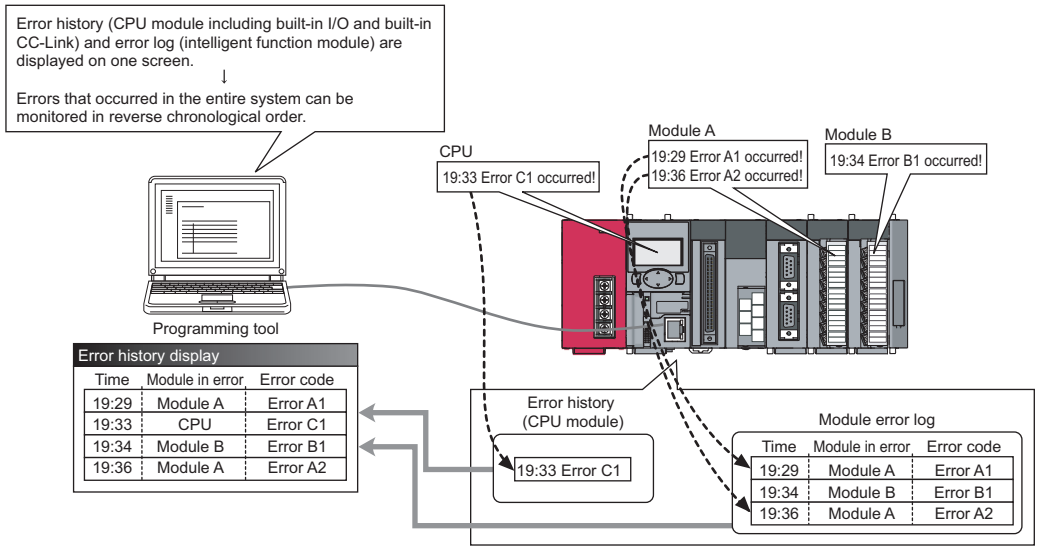


Point

If the storage areas of the error history become full, the value in Error history No. 1 (Un\G8010 to Un\G8019) is overwritten and sequentially thereafter to keep registering errors. (The errors before the overwriting are deleted.)

7.3 Module Error Collection Function

The errors that occurred in the flexible high-speed I/O control module are collected in the CPU module.
To hold errors even after the power is turned off or the CPU module is reset, save the errors in the memory that can hold data during power failure in the CPU module.



[Example of screen display]

No.	Error Code	Date and Time	Model Name	Start I/O
00125	0070	2009/12/10 17:02:37	L60AD4	0030
00124	0070	2009/12/10 17:00:05	L60AD4	0030
00123	0CE4	2009/12/10 17:00:04	L26CPU-BT	----
00122	05DC	2009/12/10 16:15:50	L26CPU-BT	----
00121	0070	2009/12/10 15:59:30	L60DA4	0030
00120	0070	2009/12/10 15:45:02	L60DA4	0010
00119	05DC	2009/12/10 14:14:38	L26CPU-BT	----
00118	0070	2009/12/10 14:12:03	L60DA4	0010
00117	0CE4	2009/12/10 13:59:54	L26CPU-BT	----
00116	0CE4	2009/12/10 13:35:11	L26CPU-BT	----
00115	05DC	2009/12/10 11:11:45	L26CPU-BT	----
00114	0070	2009/12/10 11:07:05	L60AD4	0010
00113	0CE4	2009/12/10 11:07:04	L26CPU-BT	----
00112	0070	2009/12/10 11:03:49	L60AD4	0010
00111	0CE4	2009/12/10 11:03:48	L26CPU-BT	----
00110	05DC	2009/12/09 16:30:58	L26CPU-BT	----
00109	0070	2009/12/09 16:29:33	L60DA4	0010
00108	0070	2009/12/09 16:29:12	L60DA4	0010
00107	083B	2009/12/09 16:29:11	L26CPU-BT	----

Point

For details on the module error collection function, refer to the following.
MELSEC-L CPU Module User's Manual (Function Explanation, Program Fundamentals)

7.4 Error Clear Function

When an error has occurred, the error can be cleared from "System Monitor".

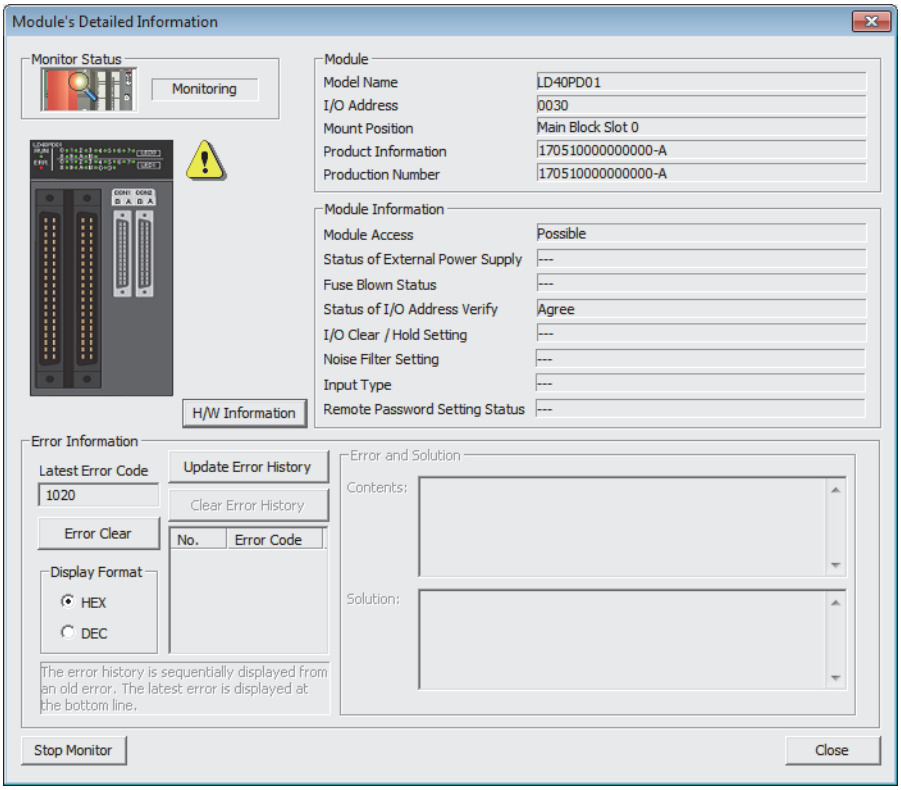
Clicking the [Error Clear] button in "System Monitor" clears the latest error code stored in Latest error code (Un\G100) and turns off the ERR. LED. This action is the same action as the one to be taken when errors are cleared with Error clear request (YF) or the display unit.

When Clear setting of error history (Un\G8002) has been set to Clear the history. (1), the error history is also cleared.

For how to clear errors with Error clear request (YF) or the display unit, refer to the following.

☞ Page 246 Error clear request (YF)

☞ Page 208 Checking and Clearing Errors



8 FUNCTIONS OF THE CONFIGURATION TOOL

This chapter describes the configuration tool for creating the hardware logic and writing it into the flexible high-speed I/O control module.

For how to get the configuration tool, refer to the following.

☞ Page 251 How to Get the Configuration Tool

8.1 How to Install and Uninstall the Configuration Tool

For the procedures of installing and uninstalling the configuration tool, refer to the following.

📖 Flexible High-Speed I/O Control Module Configuration Tool Installation Instructions

8.2 Starting and Exiting the Configuration Tool

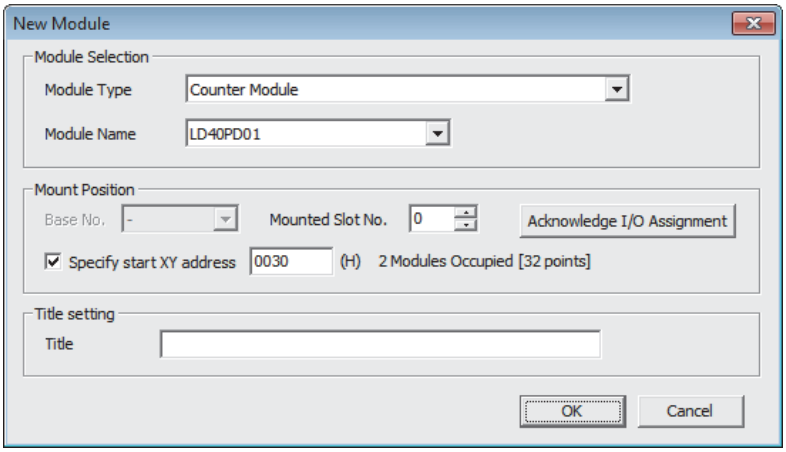
This section describes how to start and exit the configuration tool.

Start

Before starting the configuration tool, add the module with GX Works2. The following describes the operation method.

1. Add the flexible high-speed I/O control module on GX Works2.

[Project window] of GX Works2 ⇨ [Intelligent Function Module] ⇨ Right-click ⇨ [New Module]

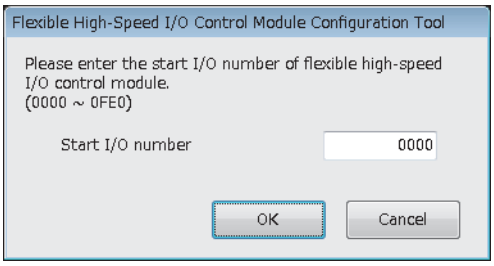


2. Write the set parameters into the CPU module.

3. Start the configuration tool.

[Start] ⇨ [All Programs] ⇨ [MELSOFT] ⇨ [FlexIo Configurator] ⇨ [FlexIo_Configurator]

4. Input the start I/O number of the flexible high-speed I/O control module and click [OK].



■Connection target

Setting the I/O assignment to GX Works2 and the configuration tool enables writing of data into the flexible high-speed I/O control module and the monitor display through the CPU module.

However, do not change the I/O assignment on GX Works2 after the configuration tool is started. If the I/O assignment is changed on GX Works2 and data writing to the module, the monitor display, or simulation is executed after the configuration tool has been started, a communication error will occur.

Exit

Select [Project] and [Exit] in the configuration tool.

8.3 Switching the Language

The configuration tool supports multiple languages. Users can switch the language to be displayed in the menu on a personal computer.

How to switch the language

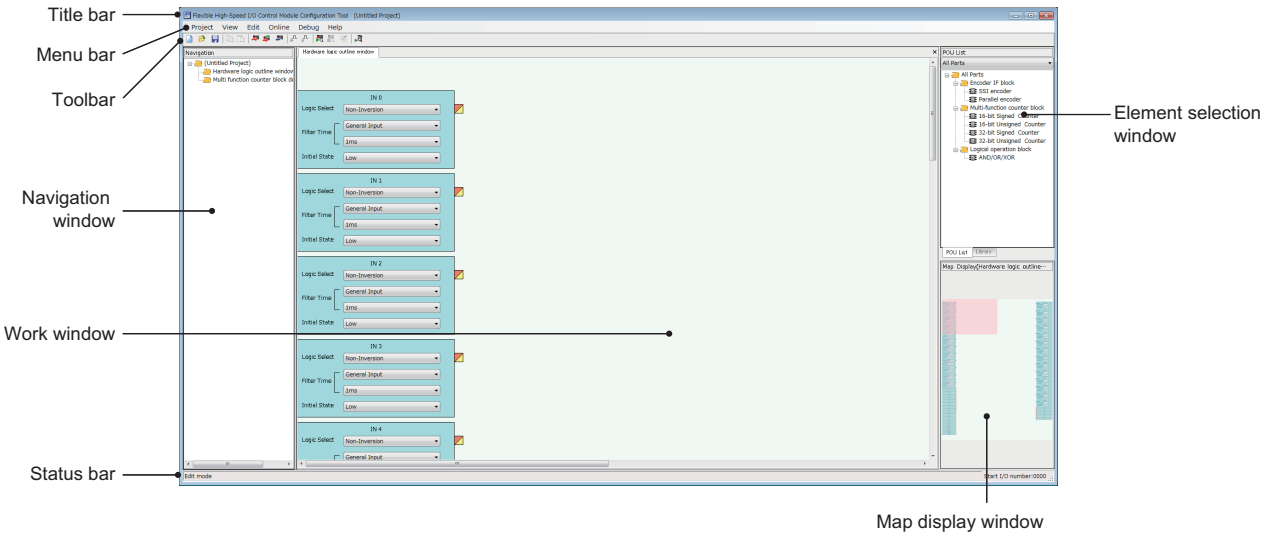
 [View] ⇨ [Switching display language]

Restriction

When a selected language is different from the one set to the OS, character strings may not be properly displayed.

8.4 Window Layout

The following figure shows the whole window layout.



For details on each item, refer to the following.

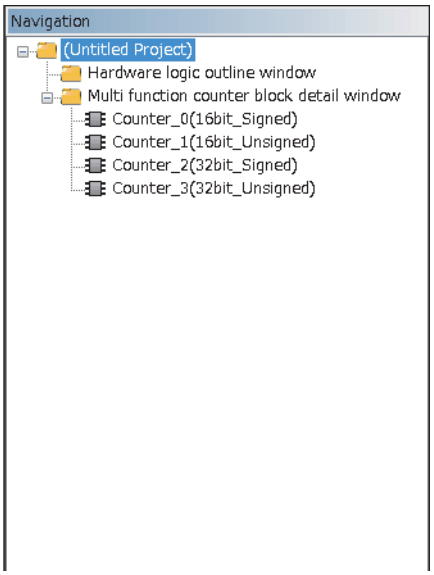
☞ Page 67 Navigation window
☞ Page 69 Work window
☞ Page 68 Element Selection window
☞ Page 70 Map display window

Navigation window

In the navigation window, the hardware logic outline window and names of multi function counter blocks arranged in the window (Counter_☐: A multi function counter block number comes in ☐.) are displayed in the tree format.

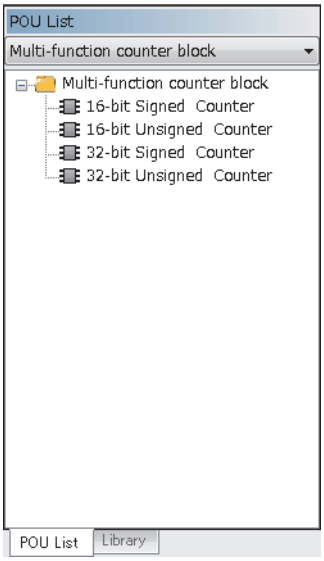
For details on the hardware logic outline window and multi function counter blocks, refer to the following.

☞ Page 103 CREATING A HARDWARE LOGIC



Element Selection window

In the Element Selection window, the main blocks that can be arranged when the hardware logic is created are displayed in the tree format.
This window displays only the blocks in a category selected from the drop-down menu at the upper section of the window.
When a multi function counter block is selected in the Element Selection window and arranged on the work window, the tab of the block is added in the work window.



"Library" tab

Select the "Library" tab to display the libraries provided by the manufacturer and the user libraries registered in the configuration tool.
For the registration method, refer to the following.
☞ Page 85 Library Function

Work window

The hardware logic is created or the monitor display is executed in the work window.

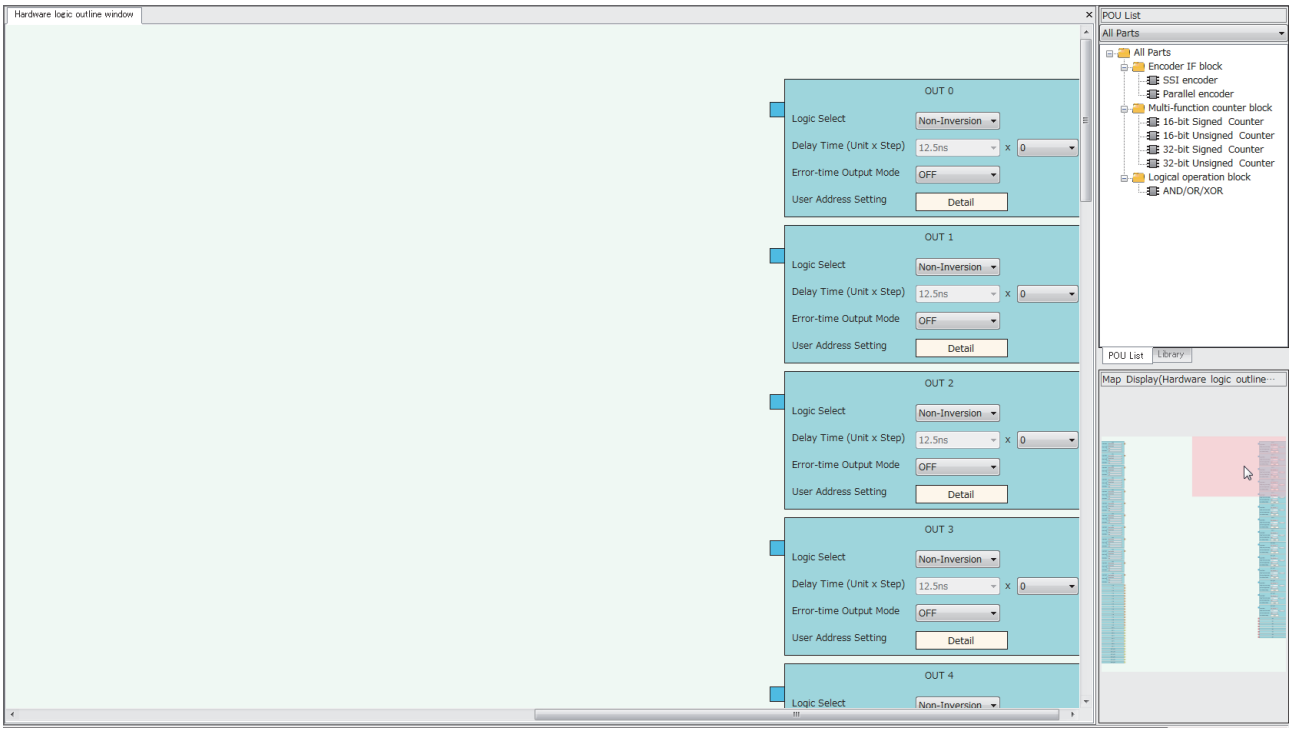
One of the hardware logic outline window (one window) and multi function counter block detail windows (up to eight windows) is displayed. Switch the window with one of the following operations.

- Double-clicking the item to display in the Navigation window
- Double-clicking a multi function counter block in the hardware logic outline window
- Clicking a tab at the upper section of the work window

Map display window

The map display window displays the hardware logic outline window that is currently being displayed or a whole image of multi function counter block detail windows in the work window.

Click the area to display to move the display position of the work window.



8.5 List of Menus of the Configuration Tool

[Project] menu

Menu	Reference
[Project] ⇨ [New]	☞ Page 72 Creating a new project
[Project] ⇨ [Open]	☞ Page 72 Opening a project
[Project] ⇨ [Save]	☞ Page 73 Saving an existing project
[Project] ⇨ [Save As]	☞ Page 73 Saving a project with a new name
[Project] ⇨ [Security]	☞ Page 74 Security
[Project] ⇨ [Exit]	☞ Page 65 Exit

[View] menu

Menu	Reference
[View] ⇨ [Switching display language]	☞ Page 66 Switching the Language

[Edit] menu

Menu	Reference
[Edit] ⇨ [Copy]	☞ Page 83 Copying a block
[Edit] ⇨ [Paste]	☞ Page 84 Pasting a block
[Edit] ⇨ [Insert and Paste]	
[Edit] ⇨ [Block Delete]	☞ Page 79 Deleting a block
[Edit] ⇨ [Export block]	☞ Page 85 Library Function
[Edit] ⇨ [Library Registration]	
[Edit] ⇨ [Library Delete]	

[Online] menu

Menu	Reference
[Online] ⇨ [Write to Module (execution memory)]	☞ Page 89 Writing data to the module
[Online] ⇨ [Write to Module (execution + flash ROM)]	
[Online] ⇨ [Read from Module (flash ROM)]	☞ Page 90 Reading data from the module
[Online] ⇨ [Verify with Module (Flash ROM)]	☞ Page 91 Verifying with the module
[Online] ⇨ [Module operation] ⇨ [Hardware logic control start]	☞ Page 92 Module operation
[Online] ⇨ [Module operation] ⇨ [Hardware logic control stop]	
[Online] ⇨ [Monitor] ⇨ [Start Monitoring]	☞ Page 93 Monitor
[Online] ⇨ [Monitor] ⇨ [Stop Monitoring]	
[Online] ⇨ [Monitor] ⇨ [End Monitoring]	

[Debug] menu

Menu	Reference
[Debug] ⇨ [Simulation]	☞ Page 95 Simulation function

[Help] menu

Menu	Reference
[Help] ⇨ [Version Information]	☞ Page 102 Checking the version of the configuration tool

8.6 Project Management

The configuration tool manages the hardware logic as a project.
This section describes the basic operations of the configuration tool for projects, such as creating, opening, and saving of a project.
Because a created project can be managed as a project file, changing of a project name, copying and pasting of a project, and other operations can be easily executed with Windows® Explorer.

Creating a new project

Create a new project.

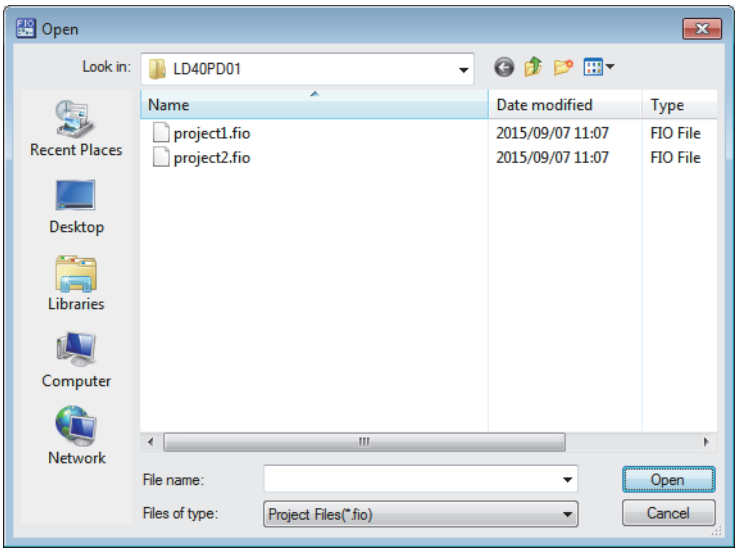
[Project] ⇨ [New]

Opening a project

Read a project saved in a hard disk or other areas in a personal computer.

1. Open the "Open" window.

[Project] ⇨ [Open]



2. Select a project to open and click the [Open] button.

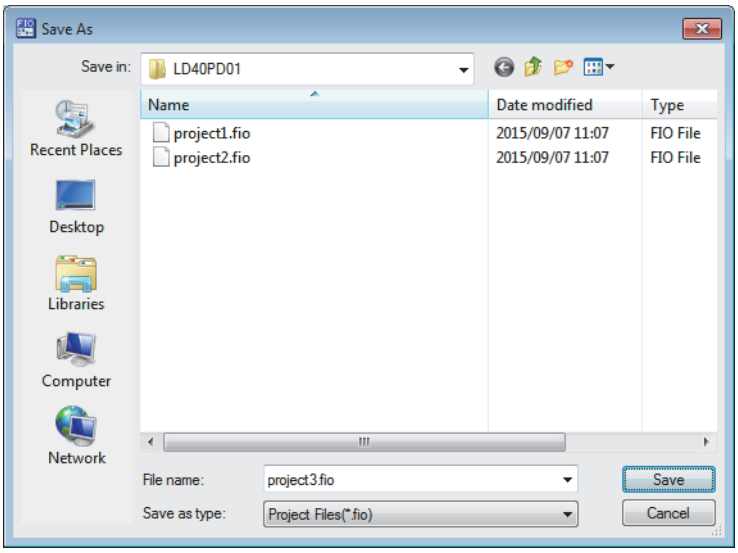
Saving a project file

Save a project file in a hard disk or other areas in a personal computer.

Saving a project with a new name

Name the project being edited and save the project file.

[Project] ⇨ [Save As]



Saving an existing project

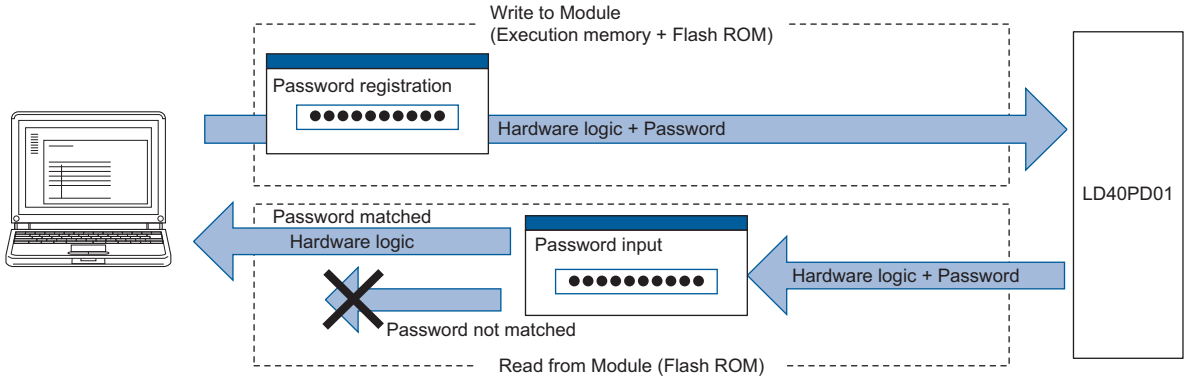
Overwrite the hardware logic information being edited on an existing project file.

[Project] ⇨ [Save]

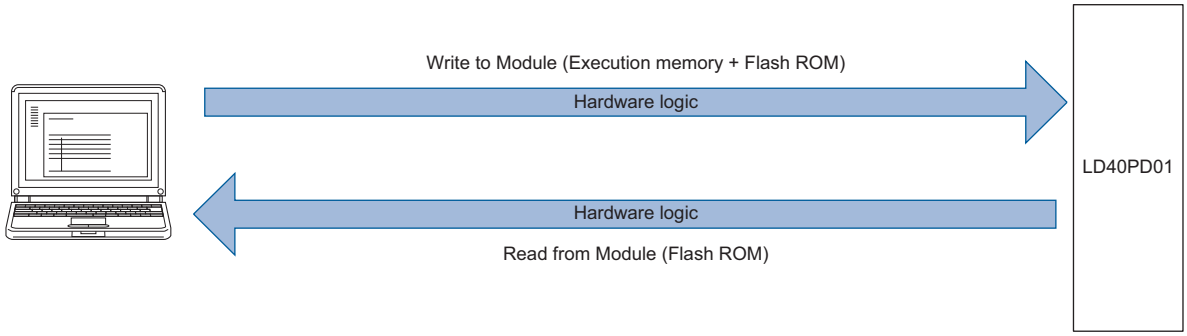
Security

When the hardware logic is written into a flash ROM, add a password to prevent inappropriate access to read the data.
After the security is set to "Enable" and [Write to Module (execution + flash ROM)] in [Online] is executed, the password input window is displayed. After a password is input and writing data into the module is completed, the security becomes valid.
To read the hardware logic to which the security has been enabled from a flash ROM to the module, input the set password.

- When the security is enabled



- When the security is disabled



Setting method

[Project] ⇨ [Security] ⇨ [Enable] or [Invalid]

When a new project is created, the security has been set to "Enable".

Operation details and restrictions

The security setting is saved in a project.

The security of the project created with the configuration tool of version 1.000A is set to "Invalid".

■Actions to be taken when "Write to Module (execution + flash ROM)" is executed

Security setting	Description
Enable	• The password registration window is displayed. • The hardware logic is written with a password.
Invalid*1	• The password registration window is not displayed. • The hardware logic is written without a password.

*1 When "Write to Module (execution memory)" is executed, the action same as the one to be taken when the security setting is "Invalid" is executed.

■Actions to be taken when "Read from Module (flash ROM)" is executed

Hardware logic in the module	Description
With a password	• The password input window is displayed. • Only when the input password matches the password in the module, the hardware logic can be read.
Without a password	• The password input window is not displayed. • The hardware logic can be always read.

■Operations that change the security setting

When one of the following operations is performed, the security setting is changed.

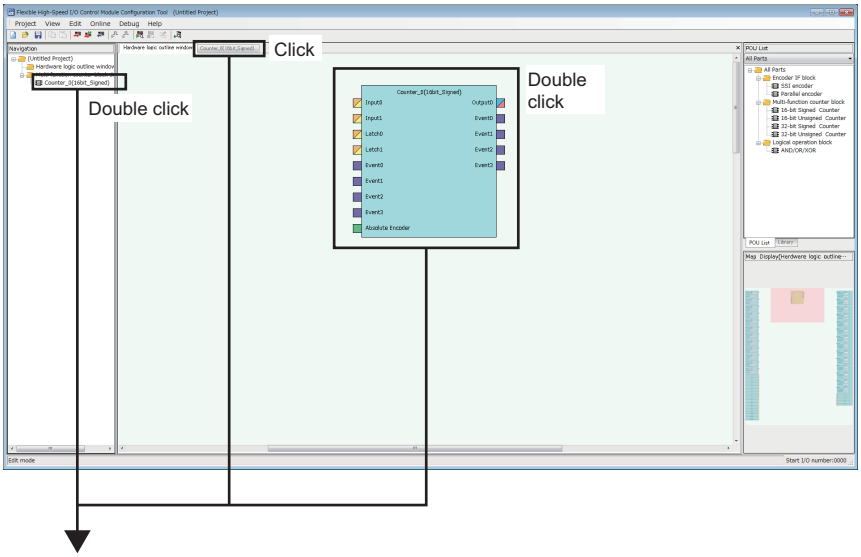
Operation	Security setting
Creating a new project	"Enable" is set.
Opening a project	The project setting is reflected.
Reading data from the module	The setting stored in the flash ROM of the flexible high-speed I/O control module is reflected.

8.7 Windows for Creating the Hardware Logic

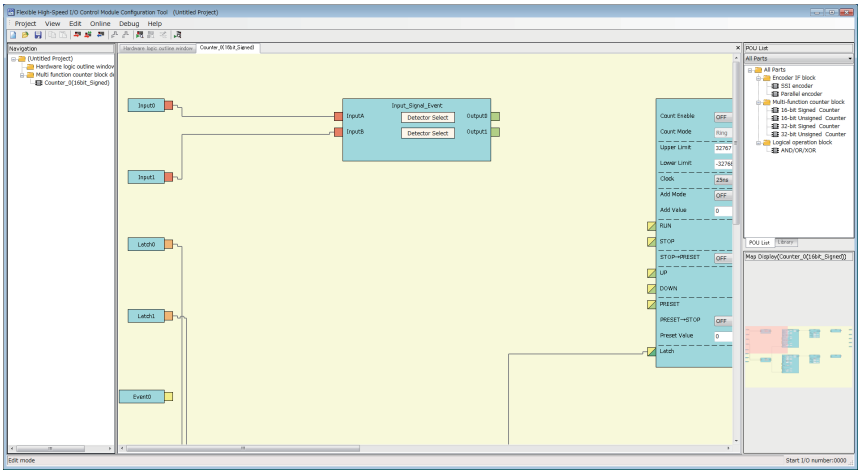
The following two types of window are prepared for creating the hardware logic. The window can be switched between the hardware logic outline window and the multi function counter block detail window.

Window	Description
Hardware logic outline window	This window is for creating the outline of the hardware logic in the flexible high-speed I/O control module. Multi function counter blocks are arranged, external I/O terminals are linked, and settings are configured in this window.
Multi function counter block detail window	This window is for configuring the detail settings of the multi function counter blocks arranged in the hardware logic outline window. Switch multi function counter block detail windows (up to eight windows) and edit each multi function counter block.

Hardware logic outline window



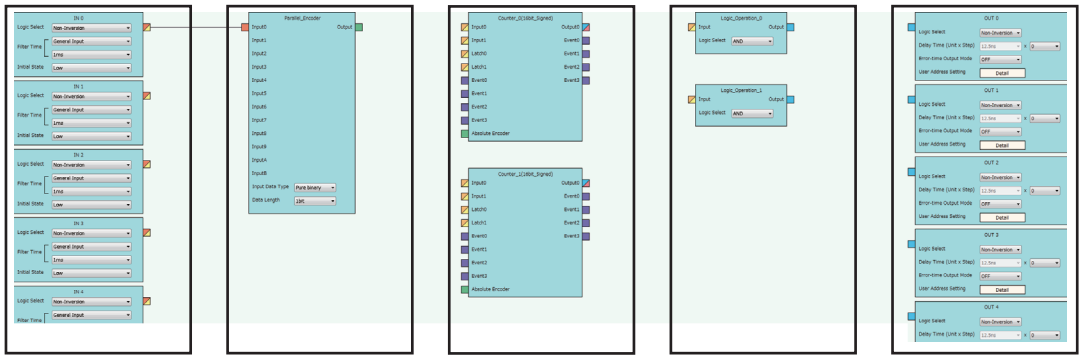
Multi function counter block detail window



Hardware logic outline window

The hardware logic outline window is composed of the following five sections. Depending on the section, the blocks that can be arranged differ.

Change the setting and wiring of each block to create the hardware logic with various functions.



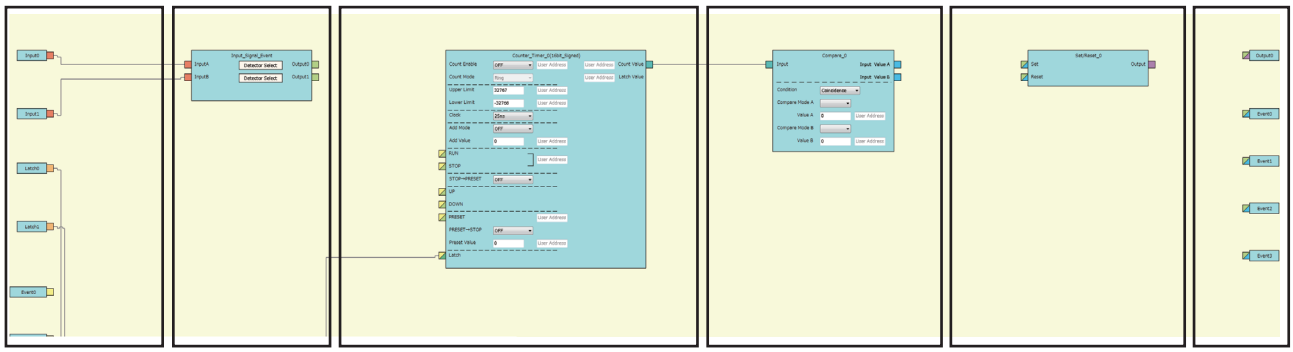
Section	Description	Blocks and terminals that can be arranged*1
First section	The blocks corresponding to inputs to the hardware logic have been arranged in this section. All the blocks in the first section are arranged when a project is started, and any blocks cannot be deleted or newly added from the Element Selection window.	• External input block • Y device terminal • OUT terminal
Second section	Blocks corresponding to encoder inputs are arranged in this section.	• Parallel encoder block • SSI encoder block
Third section	Blocks that execute count with external input signals and the internal clock are arranged in this section.	Multi function counter block
Fourth section	Blocks that calculate logical operations to input signals and outputs of multi function counter blocks are arranged in this section.	Logical operation block
Fifth section	The blocks corresponding to outputs of the hardware logic have been arranged in this section. All the blocks in the fifth section are arranged when a project is started, and any blocks cannot be deleted or newly added from the Element Selection window.	• External output block • SI device terminal

*1 For details on each block and terminal, refer to the following.

☞ Page 103 CREATING A HARDWARE LOGIC

Multi function counter block detail window

A multi function counter block detail window is composed of the following six sections.
Change the setting and wiring of each block to create various count operations.



Section	Description	Block and terminals that have been arranged*1
First section	The terminals corresponding to inputs to a multi function counter block have been arranged in this section. An input to a multi function counter block in the hardware logic outline window is handled as an input in the multi function counter block detail window.	• Input terminal • Latch input terminal • Event input terminal
Second section	Select a signal detection condition for each input signal. Desired conditions can be detected with the combinations of High/Low and rise/fall.	• Input signal event detection block • Latch event detection block
Third section	Counter timers that function depending on each event have been arranged. Switching of 16-bit signed counter/16-bit unsigned counter and 32-bit signed counter/32-bit unsigned counter is determined depending on the blocks arranged in the hardware logic outline window and cannot be changed in the multi function counter block detail window.	• Counter timer block (16bit_Unsigned) • Counter timer block (16bit_Signed) • Counter timer block (32bit_Unsigned) • Counter timer block (32bit_Signed)
Fourth section	An operation to compare a count value and a setting value of a counter timer is executed. Coincidence detections of count values can be executed with the comparison operation.	• Compare block • Cam switch block*2
Fifth section	Based on results of the comparison operation and event detections, the signals to be externally output are controlled.	• Set/reset block • Cam switch block*2
Sixth section	The terminals corresponding to outputs of a multi function counter block have been arranged in this section. Outputs from the multi function counter block detail window are handled as outputs from the multi function counter block in the hardware logic outline window.	• Output terminal • Event output terminal • Cam switch output terminal

*1 For details on each block and terminal, refer to the following.
☞ Page 127 Multi Function Counter Block

*2 A cam switch block is arranged across the fourth and fifth sections.

How to use blocks

Arranging blocks

The following describes how to arrange a block.

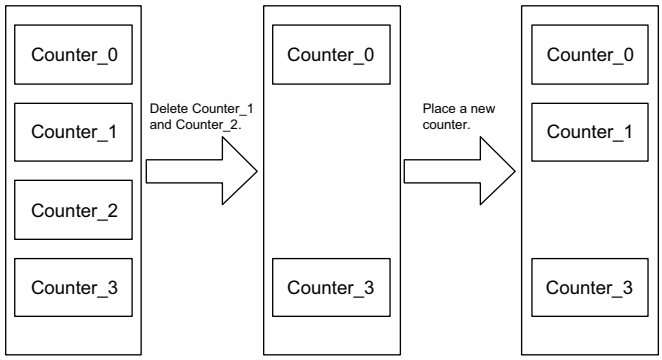
1. Select a block in the Element Selection window. Drag and drop the block into the hardware logic outline window.

When a block is dragged into the hardware logic outline window, the area to which the block can be dropped is highlighted.

2. When the selected block is dropped into the work window, the block is automatically arranged in the highlighted area.

Point

When three or more blocks have been arranged in the same section and blocks arranged between the top and bottom ones are deleted, that area becomes vacant. When a new block is arranged under this situation, the vacant area is highlighted and the block is arranged there.



Deleting a block

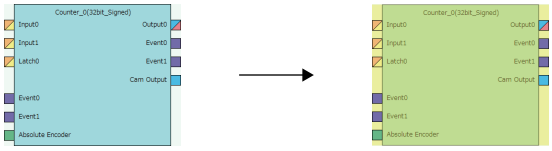
The following describes how to delete a block.

Only the blocks arranged from the Element Selection window can be deleted. The blocks that have been arranged by default cannot be deleted.

When a block is deleted, the link of the block is also deleted.

1. Click the block to be deleted.

The block is highlighted (displayed in yellow) and selected.



2. Right-click the block and select "Block Delete" from the context menu. Or press the Delete key.

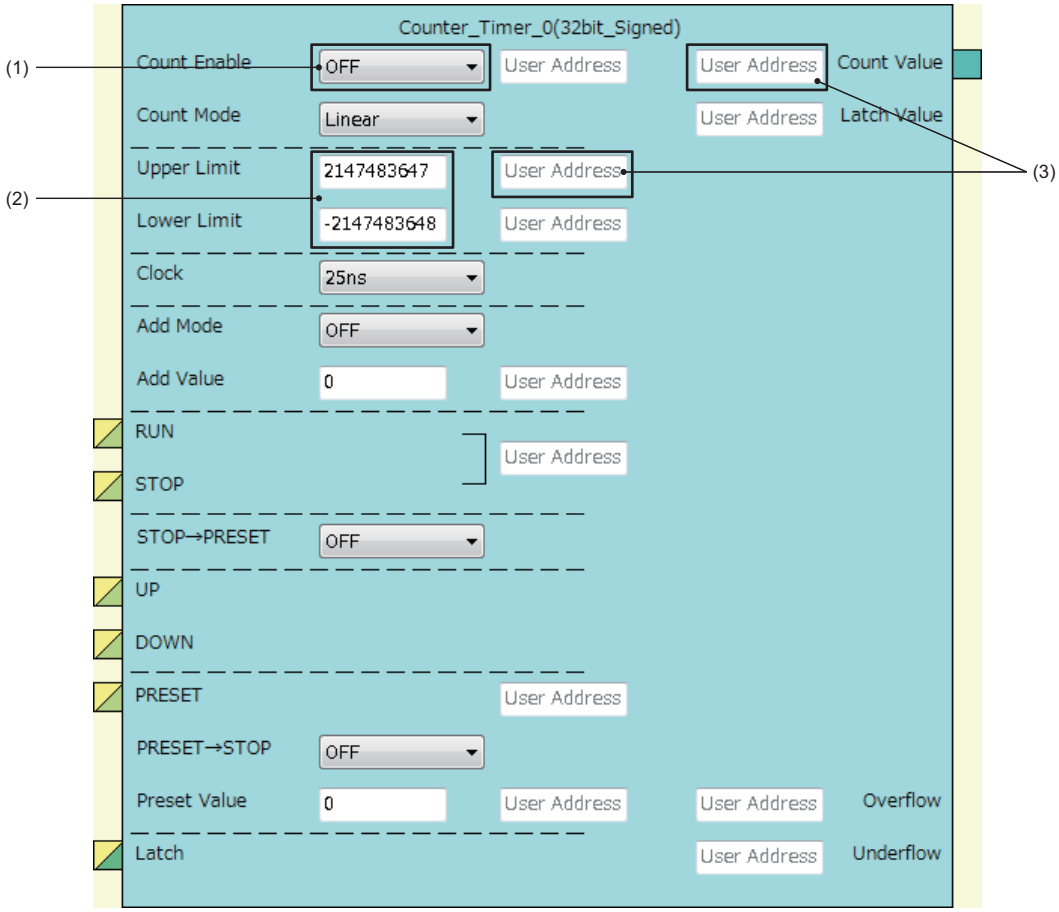
When a block is deleted, the link of the block is also deleted.

Point

- Users can also delete multi function counter blocks by right-clicking a multi function counter block name (Counter_☐) in the tree of the Navigation window and selecting "Block Delete" from the context menu.
- Select [Edit] ⇨ [Block Delete] to perform the same operation as selecting "Block Delete" from the context menu.

Block setting

Configure block settings by changing values in the drop-down lists and text boxes of each block.



No.	Item name	Description
(1)	Drop-down list	Select a setting value from the drop-down list.
(2)	Text box	Input a one-byte numerical value (decimal).
(3)	User Address	• By assigning buffer memory addresses to "User Address", input terminal status and parameter setting values can be changed with programs and values of a hardware logic can be monitored during the hardware logic control. For details, refer to the following (☞ Page 133 Assignment of "User Address"). • Input decimal values in the setting. • The range of settable buffer memory addresses is 1000 to 1099 (High speed area: 1000 to 1029, low speed area: 1030 to 1099). For details, refer to the following (☞ Page 80 Input range of User Address).

■Input range of User Address

Input range	Description
1000 to 1029	• The monitor items and setting items assigned in this area are read or written at a high speed (100μs). These items are also read or written when the flexible high-speed I/O control module sends an interrupt signal to the CPU module. • Assign even addresses to the parameters of two words (32 bits). Odd addresses cannot be assigned.
1030 to 1099	• The monitor items and setting items assigned in this area are read or written at a low speed (1ms). • Assign even addresses to the parameters of two words (32 bits). Odd addresses cannot be assigned.

Restriction

A single buffer memory address cannot be specified in several "User Address".
For example, when the buffer memory address 1000 has been specified in "Count Value" and 1000 is specified in "Latch Value", the value in User Address is returned to the initial value.

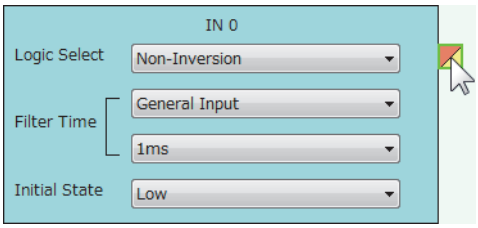
Linking blocks

Link blocks so that an output terminal of the left block in the window is handled as a start point and the input terminal of the right block in the window is handled as an end point.

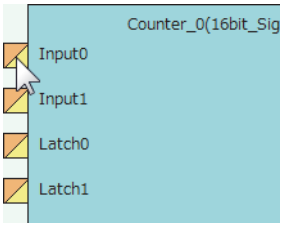
The following describes how to link blocks.

1. Click the terminal to be a start point.

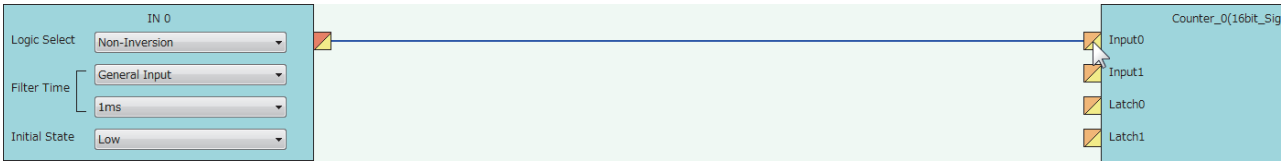
The outer frame of the selected terminal is highlighted.



2. Click the terminal to be an end point.



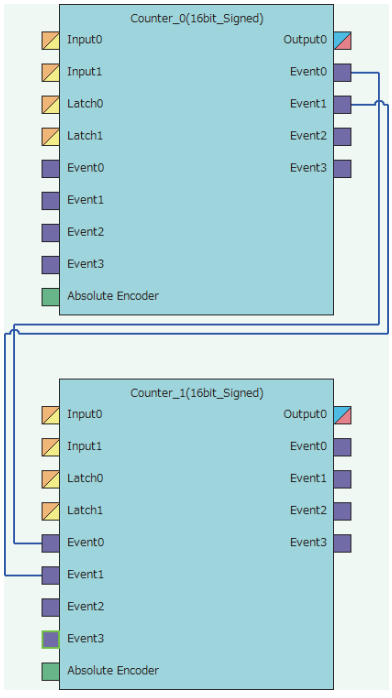
The start point and end point are automatically linked.



Point

Event terminals of a multi function counter block can be linked to Event terminals of another multi function counter block arranged in the same section.

Handle an Event terminal at the output side (right side of a multi function counter block) as a start point and an Event terminal at the input side (left side of a multi function counter block) as an end point, and link these terminals.



■Linking conditions of terminals

Terminals in the same color can be linked. Terminals with two colors can be linked with the terminals with either of the two colors.

For details on the terminal colors, refer to the following.

☞ Page 103 Main Blocks in the Hardware Logic Outline Window

■Link type

The two link colors, blue and gray, are provided.

- A connection line between a linked output terminal and input terminal is blue.
- Gray connection lines indicate that the terminals have been automatically connected. Users cannot link the terminals.

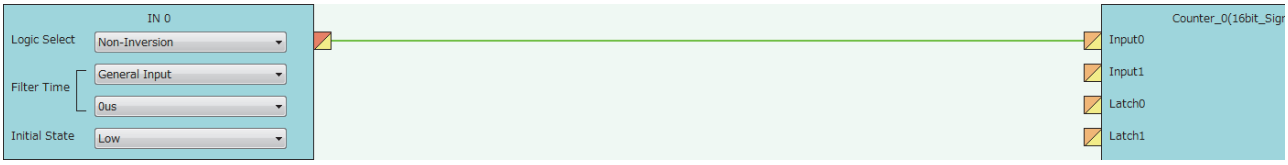
■Deleting links

The following describes how to delete a link.

Only blue connection lines can be deleted. Gray connection lines cannot be deleted.

1. Click the link to be deleted.

The link is highlighted (displayed in green) and selected.



2. Right-click the link and select "Wiring Delete" from the context menu. Or press the Delete key.

Copying a block

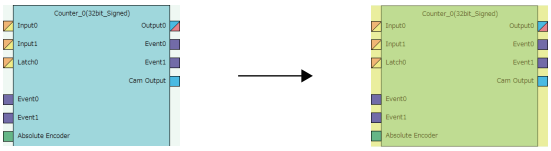
A block arranged in the hardware logic outline window can be copied by block unit. The setting values can be changed by block in a batch and an arranged block can be copied.

■Procedure of copying a block

The following describes the procedure of copying a block.

1. Click the block to be copied.

The block is highlighted (displayed in yellow) and selected.



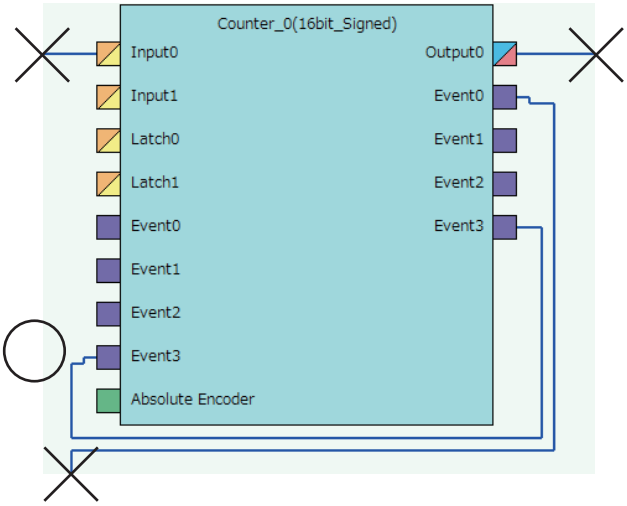
2. Right-click the block and select "Copy" from the context menu.

Point

- Users can also copy multi function counter blocks by right-clicking a multi function counter block name (Counter_☐) in the tree of the Navigation window and selecting "Copy" from the context menu.
- Select [Edit] ⇨ [Copy] to perform the same operation as selecting "Copy" from the context menu.

■Operation details and restrictions

- Multiple blocks cannot be copied at a time. Only a single block can be copied.
- The link between the block to be copied and other blocks is not copied. However, when the block to be copied is a multi function counter, link information in the multi function counter block detail window is also copied.
- The following table shows which main blocks can be copied.

Section*1	Target block	Copying	Item to be copied
1	External input block	Possible	Setting values of the block
	• Y device terminal • OUT terminal	Impossible	—
2	• Parallel encoder block • SSI encoder block	Possible	Setting values of the block
3	Multi function counter block	Possible	• Setting values in the multi function counter block detail window (the setting value of User Address is not included) and links • Link between Event terminals of a multi function counter block in the hardware logic outline window (the links across blocks cannot be copied.) 
4	Logical operation block	Possible	The setting value of the block
5	External output block	Possible	Setting values of the block
	SI device terminal	Impossible	—

*1 This indicates a section in the hardware logic outline window.

Pasting a block

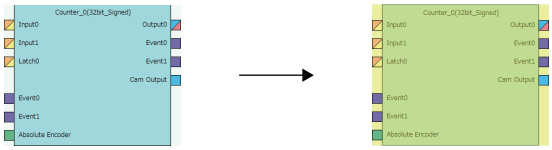
This function pastes the copy of a block. Select [Edit] ⇨ [Paste] for a block with the same type as the copy to overwrite the setting values with the ones of the copy at a time. Select [Edit] ⇨ [Insert and Paste] to add the copy as a new block in the hardware logic outline window.

■Procedure of [Paste]

The following describes the procedure of [Paste].

1. Click the block on which the copy is to be pasted.

The block is highlighted (displayed in yellow) and selected.



2. Right-click the block and select "Paste" from the context menu.

3. The setting values of the block are overwritten with the ones of the copy.

Point

- Users can also paste multi function counter blocks by right-clicking a multi function counter block name (Counter_☐) in the tree of the Navigation window and selecting "Paste" from the context menu.
- Select [Edit] ⇨ [Paste] to perform the same operation as selecting "Paste" from the context menu.

■Procedure of [Insert and Paste]

The following describes the procedure of [Insert and Paste].

1. Select the following item.

[Edit] ⇨ [Insert and Paste]

2. The copy of a block is added as a new block in the hardware logic outline window.

■Operation details and restrictions

- Selecting the block on which the copy of a block is to be pasted and selecting [Edit] ⇨ [Paste] overwrites the setting values of the target block with the ones of the copy at a time.
- Selecting [Edit] ⇨ [Insert and Paste] adds the copy of a block as a new block in the hardware logic outline window.
- Only a block with the same type as the copy of a block can be specified as a "Paste" target. If a block whose type is different from the one of the copy has been selected, the copy cannot be pasted. The setting values of a multi function counter block cannot be overwritten unless the data type of sign/unsigned and 16 bits/32 bits matches between the paste target and the copy.

8.8 Library Function

A library is a block in which the types and setting values of main blocks have been combined. Libraries can be shared between multiple projects by registering them in the configuration tool.

There are the following two types of library.

Library type	Description
Library provided by the manufacturer	The setting to enable specific functions has been applied to main blocks. Users can save time to create the hardware logic by using a library for a desired function.
User library	The blocks set by users can be exported as a user library. By exporting the blocks as a library, users can utilize the blocks that are frequently used for other projects and save time to create the hardware logic.

Export

The blocks arranged in the hardware logic outline window can be exported as a library file (.fiolib).

By exporting the blocks whose operations have been checked as library files and registering them as libraries, users can utilize them and save time to create the hardware logic.

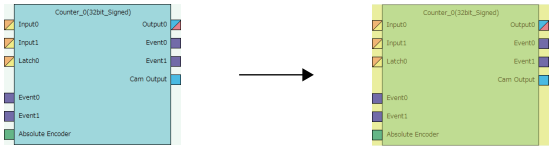
Users can name library files when exporting blocks as libraries.

Export procedure

The following describes the export procedure.

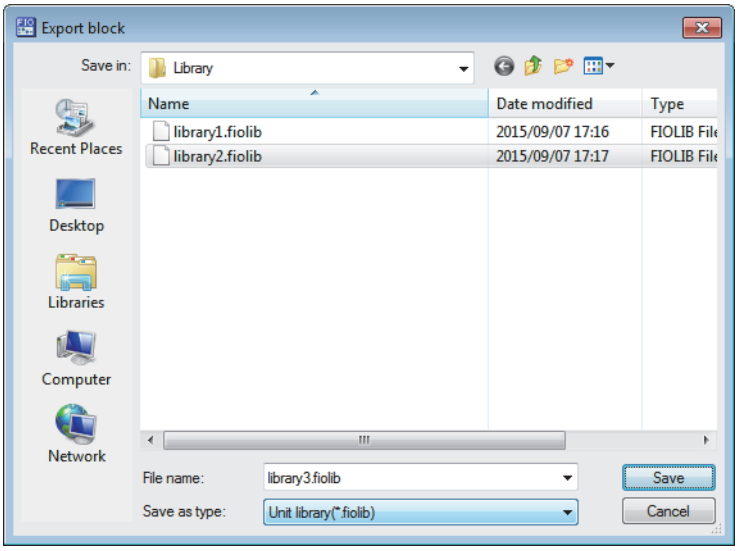
1. Click the block to be exported.

The block is highlighted (displayed in yellow) and selected.



2. Right-click the block and select "Export block" from the context menu.

3. Store the library file.

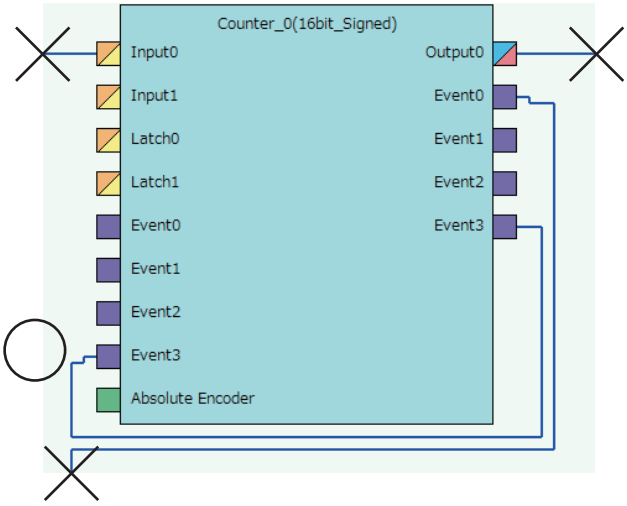


Point

Users can also export multi function counter blocks by right-clicking a multi function counter block name (Counter_☐) in the tree of the Navigation window and selecting "Export block" from the context menu.

Operation details and restrictions

- Multiple blocks cannot be exported at a time. Only a single block can be exported.
- The link between the block to be exported and other blocks is not exported. However, when the block to be exported is a multi function counter, the link information in the multi function counter block detail window and the link between Event terminals of a multi function counter block in the hardware logic outline window are also exported.
- The following table shows which main block can be exported.

Section*1	Target block	Export	Item to be exported
1	• External input block • Y device terminal • OUT terminal	Impossible	—
2	• Parallel encoder block • SSI encoder block	Possible	Setting values of the block
3	Multi function counter block	Possible	• Setting values in the multi function counter block detail window (the setting value of User Address is not included) and links • Link between Event terminals of a multi function counter block in the hardware logic outline window (the links across blocks cannot be exported.) 
4	Logical operation block	Impossible	—
5	• External output block • SI device terminal	Impossible	—

*1 This indicates a section in the hardware logic outline window.

Library operation

The following describes the library.

Restriction

No library exists immediately after the installation of the configuration tool. Register libraries as necessary.

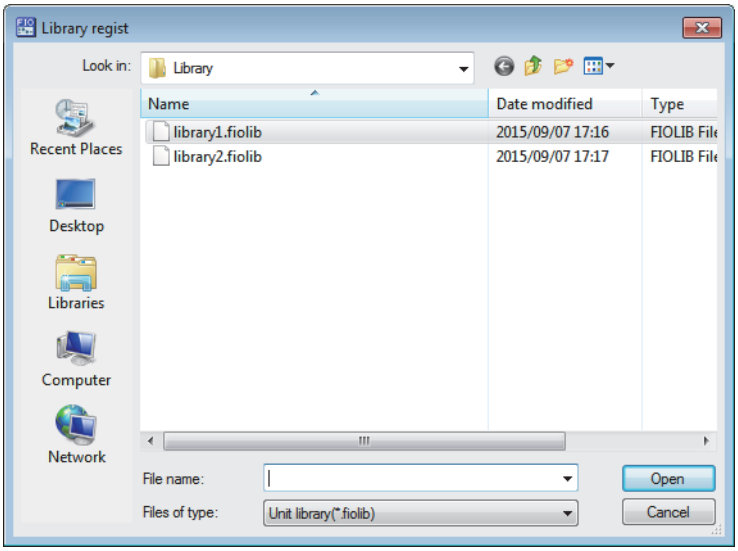
Registering a library

Register the libraries provided by the manufacturer and exported user libraries in the configuration tool. Registering libraries adds the blocks in library files in the "Library" tab in the Element Selection window.

1. Select the following item.

[Edit] ⇨ [Library Registration]

2. Open a library file to be registered in the configuration tool.



3. The registered library is added in the "Library" tab in the Element Selection window.

How to use a library

Registered libraries can be selected from the Element Selection window and dragged and dropped into the work window to arrange them in the same way as main blocks.

1. Select a block in the Element Selection window. Drag and drop the block into the hardware logic outline window.

When a block is dragged into the hardware logic outline window, the area to which the block can be dropped is highlighted.

2. When the selected block is dropped into the work window, the block is automatically arranged in the highlighted area.

The block name of the arranged library is the same as the main block. For example, when a registered block as a library is a 16-bit unsigned counter, the name of the block arranged in the work window is "Counter_□(16bit_Unsigned)".

How to delete a library

Libraries that are no longer required can be deleted from the configuration tool.

1. Click the library to be deleted in the Element Selection window.

2. Right-click the library and select "Eliminate Registration of Library" from the context menu.

Even though the library is deleted, the library file is not deleted from the storage folder. To use the library again, register the library again.

Point

Select [Edit] ⇨ [Library Delete] to perform the same operation as selecting "Eliminate Registration of Library" from the context menu.

8.9 Online Functions

Connect the computer in which the configuration tool has been installed and the CPU module, and read or write data from/to the flexible high-speed I/O control module through the CPU module. The following table lists the online functions.

Function	Description	Reference
Write to Module (Execution memory)	Writes the hardware logic to only the execution memory.	☞ Page 89 Writing data to the module
Write to Module (Execution memory + Flash ROM)	Writes the hardware logic to both the execution memory and the flash ROM.	
Read from Module (Flash ROM)	Reads the hardware logic saved in the flash ROM to the configuration tool.	☞ Page 90 Reading data from the module
Verify with Module (Flash ROM)	Verifies the hardware logic in the configuration tool and the setting data written in the flash ROM.	☞ Page 91 Verifying with the module
Module operation	Starts/stops the hardware logic control.	☞ Page 92 Module operation
Monitor	Monitors the on/off states of I/O terminals and count values. The following lists the items that can be monitored.*1 • High/Low states of output terminals in an external input block (hardware logic outline window) • High/Low states of input terminals in an external output block (hardware logic outline window) • Internal action states of input terminals and count values in a counter timer block (multi function counter block detail window)	☞ Page 93 Monitor

*1 The statuses of I/O signals in the hardware logic are described as High and Low. For details, refer to the following.
☞ Page 104 Signal status name

Restriction

If a communication error occurs while an online function is being executed, the possible cause is one of the following causes. Check the target module and communication status.

- A module with the target start I/O number does not exist.
- A communication error has occurred during online access.
- Cable error

Writing data to the module

Write the hardware logic to the execution memory of the flexible high-speed I/O control module.
The execution memory and the flash ROM can be selected as the write destination of the data. Select only the execution memory or both the execution memory and the flash ROM as the write destination.
Because the hardware logic written into the flash ROM is read to the execution memory at power-on, a control can be started without re-setting. However, the number of writable times to a flash ROM is 10000 times. Thus, using different write destinations as shown in the following examples is recommended.

- When the adjustment is repeated with changing the settings, select "Write to Module (execution memory)".
- After the adjustment is completed, select "Write to Module (execution + flash ROM)".

Users can set a password for the hardware logic by setting "Enable" in the [Security] menu of [Project]. For the hardware logic with a password, users are required to input the password for reading the hardware logic from the module.

Writing data

The following describes how to write data.

1. Select a writing method depending on a selected write destination.

[Online] ⇨ [Write to Module (execution memory)] or [Write to Module (execution + flash ROM)]

When "Write to Module (execution + flash ROM)" has been selected and the number of writes to flash ROM exceeds 10000 times, the error window is displayed. Data can be written to the module even in such situation. However, the data written in the flash ROM is not guaranteed.

2. When the following conditions are satisfied, set a password.

- "Enable" has been set in the [Security] menu of [Project].
- [Write to Module (execution + flash ROM)] has been selected.

Point

- If data writing is executed while the hardware logic control is operating, the hardware logic control will stop and the data will be written to the module. After the data writing is completed, the hardware logic control restarts.
- If data writing is executed while the hardware logic control has stopped, the stop status of the hardware logic control will continue.

Reading data from the module

Read the hardware logic saved in the flash ROM of the flexible high-speed I/O control module to the configuration tool. The hardware logic being edited is overwritten by the read data. Save the hardware logic before the data reading as necessary.

Reading data

The following describes how to read data.

1. Select the following item.

 [Online] ⇨ [Read from Module (flash ROM)]

2. To read the hardware logic with a password, input the password set when the data was written to the module.

Verifying with the module

Verify the hardware logic in the project file being edited and the hardware logic saved in the flash ROM of the flexible high-speed I/O control module. Verification results are displayed in a list and mismatches can be checked.

Verifying the hardware logic

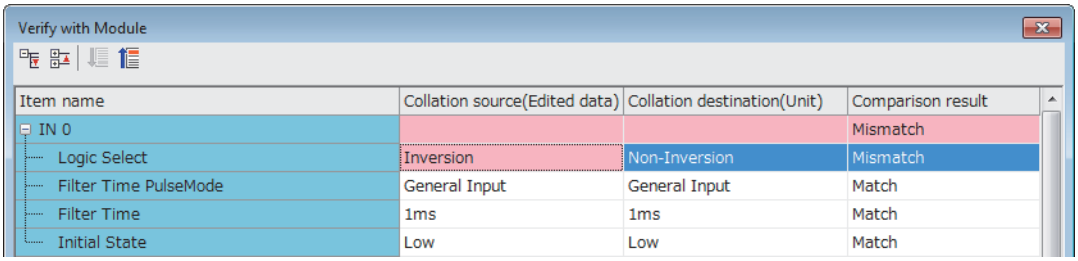
The following describes how to verify the hardware logic.

1. Select the following item.

[Online] ⇨ [Verify with Module (Flash ROM)]

2. Verification results are displayed.

In the verification result window, the match/mismatch status (the links to the input terminals of each block, setting values of the block, and User Address) are displayed.



Item name	Collation source(Edited data)	Collation destination(Unit)	Comparison result
IN 0			Mismatch
Logic Select	Inversion	Non-Inversion	Mismatch
Filter Time PulseMode	General Input	General Input	Match
Filter Time	1ms	1ms	Match
Initial State	Low	Low	Match

3. Double-click a mismatch to jump to the corresponding section in the work window. When the links are mismatched, the corresponding link in the work window is selected.

Module operation

The hardware logic control can be started or stopped with the configuration tool.
Start or stop the hardware logic control under the following situations.

Operation	Situation
Starting the hardware logic control	• Use this operation after the power is turned on. The hardware logic control is stopped after the power-on. Check the safety and select [Hardware logic control start] to start the control. • Use this operation after the completion of the simulation. The hardware logic control is stopped after the completion of the simulation. Select [Hardware logic control start] to start the control again.
Stopping the hardware logic control	Use this operation to check the module and system status. Select [Hardware logic control stop] to stop the control. When checking the module and system status, stop the hardware logic control for safety.

How to start or stop the hardware logic control

The following describes how to start or stop the hardware logic control.

[Online] ⇨ [Module operation] ⇨ [Hardware logic control start] or [Hardware logic control stop]

This operation can be performed during monitor execution. For details on the monitor, refer to the following.

☞ Page 93 Monitor

Restriction

When the hardware logic control is stopped, the count value of the counter timer block is reset. To stop the count operation without resetting the count value, turn off the count enable of the counter timer block.

Checking the operating status of the hardware logic control

The operating status of the hardware logic control can be checked in the toolbar during monitor execution.

Hardware logic control status	Button status	Remarks
During hardware logic control		The "Hardware logic control stop" button can be pressed during the hardware logic control.
During hardware logic control stop		The "Hardware logic control start" button can be pressed during the hardware logic control stop.

When the hardware logic control is started or stopped from the configuration tool, Hardware logic control flag (X4) turns on or off. Thus, users can check the operating status of the hardware logic control by monitoring the status of Hardware logic control flag (X4) in GX Works2.

For details on Hardware logic control flag (X4), refer to the following.

☞ Page 241 Hardware logic control flag (X4)

Relations of operations with output signals and window operations

The hardware logic control can be started or stopped with the configuration tool or output signals (Y4, Y5). The (start or stop) status of the hardware logic control changes depending on the last operation performed.

- When [Hardware logic control start] is selected with Hardware logic control stop request (Y5) on, the hardware logic control is started.
- When [Hardware logic control stop] is selected with Hardware logic control start request (Y4) on, the hardware logic control is stopped.

For details on Hardware logic control start request (Y4) and Hardware logic control stop request (Y5), refer to the following.

☞ Page 244 Hardware logic control start request (Y4)
☞ Page 244 Hardware logic control stop request (Y5)

Monitor

The High/Low states of I/O terminals and count values are displayed in the hardware logic outline window or a multi function counter block detail window.

The following lists the items that can be monitored.

Window	Block	Item
Hardware logic outline window	External input block	ON/OFF state of the corresponding external input terminal
		High/Low state of the output terminal
	Multi function counter block	High/Low state of the Output 0 terminal
	External output block	High/Low state of the input terminal
		ON/OFF state of the corresponding external output terminal
Multi function counter block detail window	Counter timer block	• Internal action state of the input terminal • Count value

How to use

The following shows how to start, stop, and end the monitoring.

[Online] ⇨ [Monitor] ⇨ [Start Monitoring], [Stop Monitoring], or [End Monitoring]

The monitoring can be started, stopped, or ended under the following conditions.

Operation	Condition
[Start Monitoring]	Can be used when the window mode*1 is "Edit Mode" or "Monitor Mode".
[Stop Monitoring]	Can be used when the window mode*1 is "Monitor Mode".
[End Monitoring]	Can be used when the window mode*1 is "Monitor Mode".

*1 The current window mode can be checked on the status bar.

Restriction

Although switching of the window between the hardware logic outline window and multi function counter block detail windows and changing of the display position by the map display window are allowed even during monitoring, operations other than them cannot be executed.

Monitor display

■Monitor display target

The following terminals can be monitored. Monitor values of the terminals that have not been linked are not displayed.

Window name	Block name		Terminal	Item to be monitored*2
Hardware logic outline window	External input block	IN 0 to IN B	—	ON/OFF state of the input terminal (external terminal)
			Output terminal	High/Low state of a terminal
	Multi function counter block	Counter_0 to Counter_7	Output 0 terminal	High/Low state of a terminal
	External output block	OUT 0 to OUT 7	Input terminal	High/Low state of a terminal
			—	ON/OFF state of the output terminal (external terminal)
		OUT 0_DIF to OUT 5_DIF	Input terminal	High/Low state of a terminal
			—	ON/OFF state of the output terminal (external terminal)
Multi function counter block detail window	Counter timer block	Counter_Timer_0 to Counter_Timer_7	RUN terminal	Internal action state of the counter timer block to an input terminal*1
			STOP terminal	
			UP terminal	
			DOWN terminal	
			PRESET terminal	
			Count Value terminal	Count value

*1 When a buffer memory address is assigned to User Address of each terminal and a control is executed, the input state from the buffer memory cannot be monitored.
When checking the input state from the buffer memory, monitor the corresponding buffer memory area with "Device/Buffer Memory Batch" of GX Works2.

*2 For the input terminal (external terminal) of an external input block and the output terminal (external terminal) of an external output block, the latest ON/OFF state of each terminal is displayed even while the hardware logic is stopped.
For other items, monitor values are not updated while the hardware logic control is stopped.

■Item to be monitored

Monitor values are displayed at the upper section of the terminal or block. The ON/OFF state or Low/High state is displayed as follows.

- Off: Off state or Low state
- On: On state or High state

When the monitoring has stopped, the values immediately before the monitoring stop are displayed.

8.10 Debug Function

Simulation can be executed as the debug function.

Simulation function

The simulation function verifies the hardware logic written into the flexible high-speed I/O control module without wiring with external devices.

With the configuration tool, create "simulation input data", the substitute for external input signals, and write the data into the flexible high-speed I/O control module to operate the hardware logic.

Simulation results can be saved in CSV files. Saved results can be visually checked with GX LogViewer.

Restriction

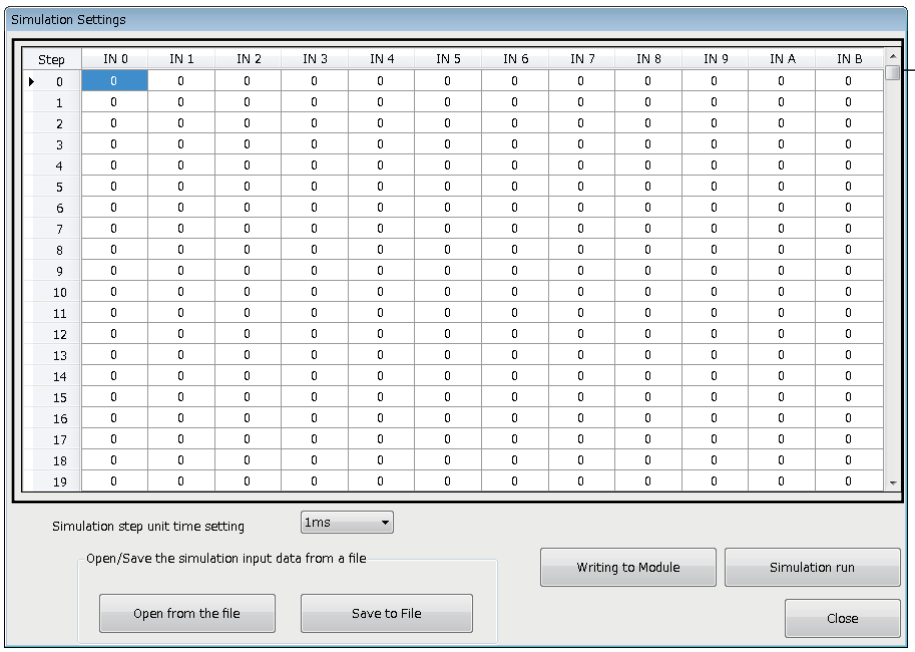
- During simulation, external outputs are actually turned on or off. Thus, execute the simulation under the situation in which the module has not be connected with external devices or paying adequate attention not to affect the system.
- Even though the simulation is executed with the hardware logic where an SI device terminal is linked, an interrupt request to the CPU module is not output.
- Even though the simulation is executed with the hardware logic where an SSI encoder block has been arranged, the communication with an SSI encoder will not be performed. Thus, position data of the SSI encoder is not reflected to simulation execution results.

Window layout

The following describes the configurations of the "Simulation Settings" window. In this window, "simulation input data" can be created and written into the flexible high-speed I/O control module or simulation is executed.

(Simulation input data is composed of external input signal data and "Simulation step unit time setting" in this window.)

[Debug] ⇨ [Simulation]



The following table lists the items to be displayed in the "Simulation Settings" window.

Item	Description
External input signal data setting area	To verify the hardware logic, set the status of data to be imported as external input signals (IN 0 to IN B). The setting value 0 indicates that an external input signal is off, and the setting value 1 indicates that an external input signal is on. Click a cell and switch the value between 0 (OFF) to 1 (ON). Columns in the area indicate the 12 points of the external input signals (IN 0 to IN B) and rows indicate 2048 steps (0 to 2047). In the simulation, the hardware logic is executed one step by one step at every cycle which is set in "Simulation step unit time setting".
"Simulation step unit time setting"	Set the cycle to switch external input signal data to the next step. Sampling of simulation results is also executed at this set cycle.
"Open from the file" button	Reads the simulation input data saved in a CSV file to the "Simulation Settings" window.
"Save to File" button	Saves the simulation input data in the "Simulation Settings" window into a CSV file.
"Writing to Module" button	Writes the simulation input data set in the "Simulation Settings" window into the module. The written data is held until the flexible high-speed I/O control module is powered off. To execute the simulation, write simulation input data into the module in advance.
"Simulation run" button	Executes the simulation with the simulation input data and hardware logic written into the module. After the completion of the simulation, the "A simulation execution result is saved." dialog box is displayed. Save the simulation execution result.
"Close" button	Closes the "Simulation Settings" window.

Data that can be acquired as simulation execution results

Users can acquire the following data by executing simulation. The execution result data acquired after simulation can be saved in a CSV format file. The file can be visually checked with GX LogViewer.

Window name	Block name		Terminal	Data to be acquired
Hardware logic outline window	External input block	IN 0 to IN B	Output terminal	High/Low state of a terminal
	External output block	OUT 0 to OUT 7	Input terminal	
		OUT 0_DIF to OUT 5_DIF	Input terminal	
Multi function counter block detail window*1	Counter timer block	Counter_Timer_0 to Counter_Timer_7	RUN terminal	Internal action state of the counter timer block to an input terminal
			STOP terminal	
			UP terminal	
			DOWN terminal	
			PRESET terminal	
			Count Value terminal	Count value

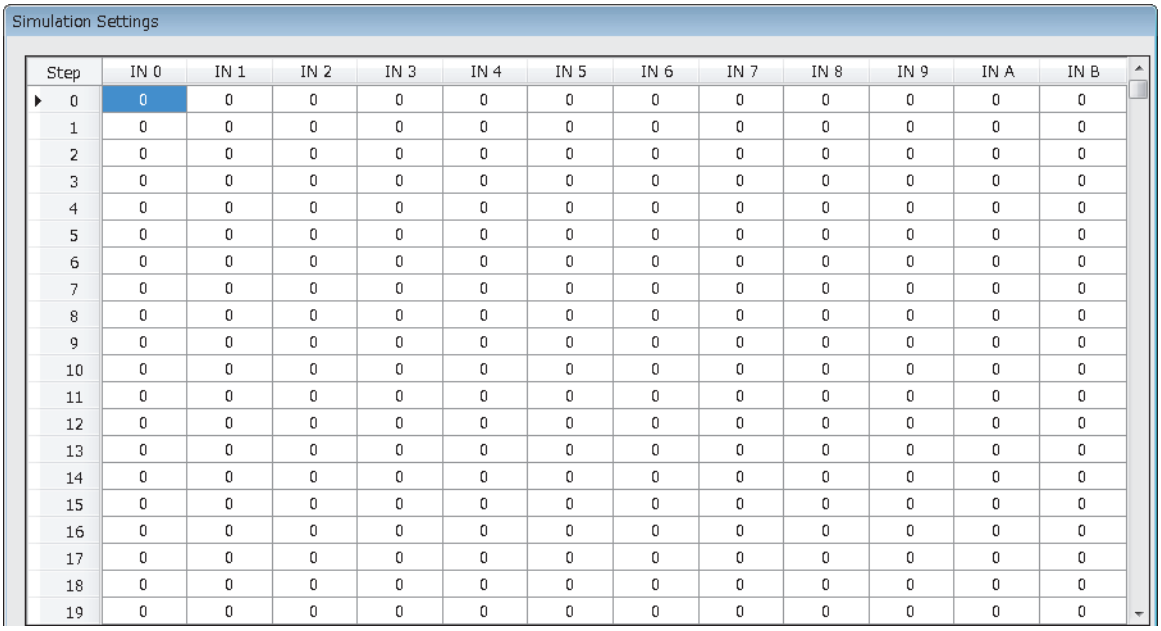
*1 Simulation results of the blocks arranged in the hardware logic outline window are acquired.

How to use

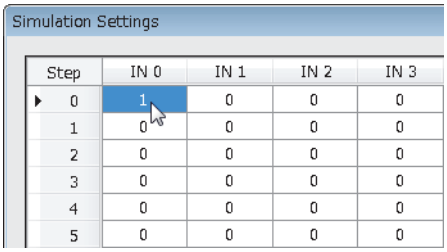
The following describes how to use the simulation function.

1. Open the "Simulation Settings" window.

[Debug] ⇨ [Simulation]



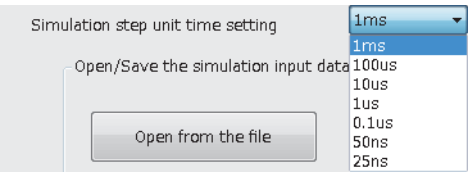
2. Click each cell in the external input signal data setting area and switch "0: External input signal OFF" and "1: External input signal ON". By default, "0: External input signal OFF" have been set in all cells.



3. Set "Simulation step unit time setting".

Changing "Simulation step unit time setting" changes the following timing.

- Timing to move external input data to the next step (Data is changed one step by one step at the set unit time.)
- Acquisition interval of execution result data (An execution result for one step is acquired at the set unit time.)



Users can save the set simulation input data with the "Save to File" button (Data is saved only in CSV format).

The following shows the CSV file format specifications. When creating a CSV file with any method other than the one using the "Simulation Settings" window, create the file in the same format.

Item name	Character
Delimiter	Comma (,)
Return code	CRLF (0x0D, 0x0A)

	A	B	C	D	E	F
1	8					
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
5	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0
9	0	0	0	0	0	0
10	0	0	0	0	0	0

Row	Description	
1st row	The simulation step unit time setting is output.	
	Simulation step unit time setting	Value output into a CSV file
	1ms	8
	100µs	7
	10µs	6
	1µs	5
	0.1µs	4
	50ns	3
	25ns	2
2nd to 2049th row	One row indicates one step, and external input signal data is output as "0: OFF" or "1: ON" in order of IN 0, IN 1 to IN B starting from the left row.	

Users can open a saved CSV file from "Open from the file" of "Open/Save the simulation input data from a file".

Restriction

- The "Writing to Module" button only writes simulation input data into the module. Write the hardware logic into the module in advance.
- The simulation input data written into the module is cleared when the module is powered off.
- When the external input signal data in the CSV file selected from "Open from the file" has less than 2048 steps or 12 rows, the data is not reflected in the "Simulation Settings" window. When the data has 2048 steps or more or 12 rows or more, the external input signal data of 2048 steps or 12 rows is read. The data that is not the read target is discarded.

4. Click "Writing to Module" to write the simulation input data into the flexible high-speed I/O control module.

Restriction

If a communication error has occurred during the communication with the module with the simulation function, the possible cause is one of the following causes. Check the target module and communication status.

- A module with the target start I/O number does not exist.
- A communication error has occurred during online access.
- Cable error

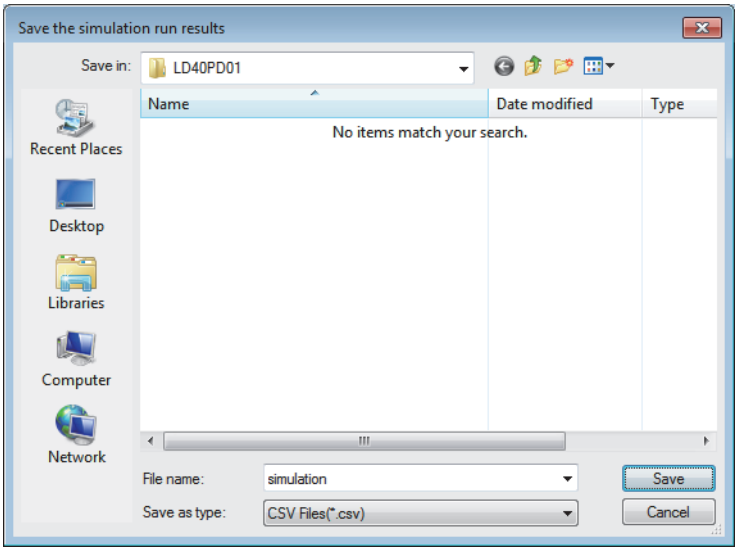
5. Click "Simulation run" to execute the simulation of the written simulation input data.

The simulation is executed by using the hardware logic and simulation input data written into the module. When the simulation input data has been edited, always press the "Write to Module" button to write the data into the module in advance.

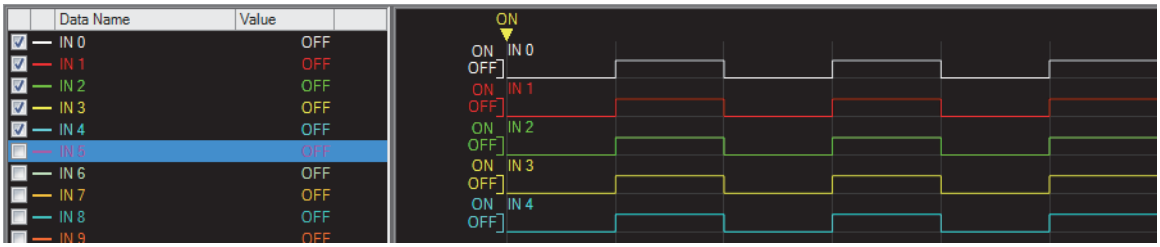
Restriction

- If the simulation is started during a hardware logic control, the hardware logic control will stop. After the completion of the simulation, the stop status of the hardware logic control will continue. To start the hardware logic control after the simulation, turn on Hardware logic control start request (Y4).
- If Hardware logic control start request (Y4) or Hardware logic control stop request (Y5) is turned on during the simulation, simulation execution results cannot be properly acquired.
- If Hardware logic control start request (Y4) is turned on while simulation execution results are being acquired after the simulation, the acquisition of the simulation execution results will stop.

6. Save the simulation execution results. (Data is saved only in the CSV format.)



7. The simulation execution results can be visually checked with GX LogViewer.



For details on GX LogViewer, refer to the following.

GX LogViewer Version 1 Operating Manual

CSV file format of simulation execution results

The following shows the CSV format specifications of simulation execution results.

Item name	Character
Delimiter	Comma (,)
Return code	CRLF (0x0D, 0x0A)

	A	B	C	D	E	F
1	[LOGGING]	LD40PD01_1	2	3	4	
2	BIT[1;0]	BIT[1;0]	BIT[1;0]	BIT[1;0]	BIT[1;0]	BIT[1;0]
3	IN 0	IN 1	IN 2	IN 3	IN 4	IN 5
4	1	1	1	1	1	1
5	1	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0
9	0	0	0	0	0	0
10	0	0	0	0	0	0

■1st row

[LOGGING], LD40PD01_1, 2, 3, and 4 are output (fixed output).

■2nd row

The data type of the simulation execution result is output.

Data type	Bit	Word (unsigned) Double word (unsigned)	Word (signed) Double word (signed)
Value output into a CSV file	BIT[1;0]	ULONG[DEC.0]	LONG[DEC.0]

TRIGGER[*] is output in the last column of the 2nd row (fixed output).

■3rd row

The name of each input or output terminal is output.

I/O terminal	Name to be output
• Input terminal in the hardware logic outline window • Output terminal in the hardware logic outline window	Block name, terminal name
• Input terminal in a multi function counter block detail window • Output terminal in a multi function counter block detail window	Multi function counter block name, block name, terminal name

Trigger is output in the last column of the 3rd row (fixed output).

■4th to 2051st row

The acquired data is chronologically output (at the set simulation step unit time).

Window name	Block name		Terminal	Data type	Data to be acquired
Hardware logic outline window	External input block	IN 0 to IN B	Output terminal	BIT[1;0]	Indicates the High/Low state of a terminal. 0: Low state 1: High state
	External output block	OUT 0 to OUT 7	Input terminal	BIT[1;0]	
		OUT 0_DIF to OUT 5_DIF	Input terminal	BIT[1;0]	
Multi function counter block detail window	Counter timer block	Counter_Timer_0 to Counter_Timer_7	RUN terminal	BIT[1;0]	Indicates the internal action state of the counter timer block to an input terminal. 0: Internal action stop status 1: Internal action execution status
			STOP terminal	BIT[1;0]	
			UP terminal	BIT[1;0]	
			DOWN terminal	BIT[1;0]	
			PRESET terminal	BIT[1;0]	
			Count Value terminal	ULONG[DEC.0]/ LONG[DEC.0]	Count value

[*] is output in the last column of the 4th row (fixed output).

Point

The data in the 0th step of the simulation input data is reflected to the initial value of the Output terminal in the external input block.

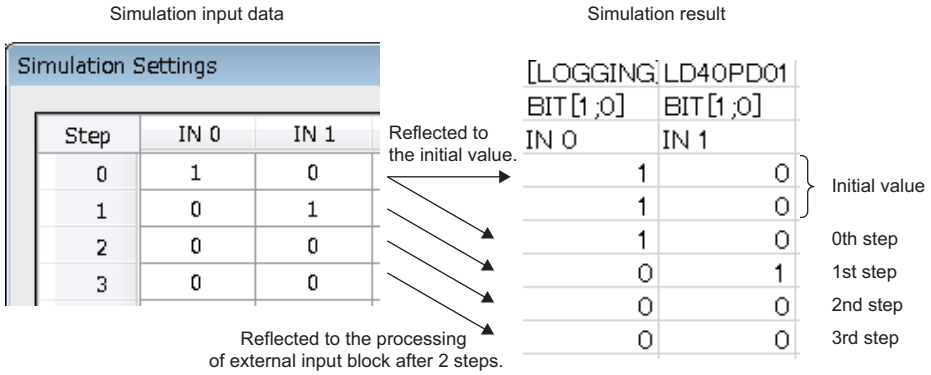
Because the processing time of the hardware logic affects the simulation step, the following time is required until the simulation input data changes the Output terminal in the external input block.

- When "Simulation step unit time setting" is "25ns", it takes time of 2 steps.
- When "Simulation step unit time setting" is other than "25ns", it takes time of 1 step.

Ex.

When simulation is executed with the simulation step unit time of 25ns and the external input block filter time of 0µs, the simulation result of an external input block is reflected as follows.

(When the filter time has been set, the simulation result is reflected after the time of the steps for the filter time passes.)



8.11 Help Function

As the help function, the software version of the configuration tool can be checked.

Checking the version of the configuration tool

Information including the software version of the configuration tool is displayed.

[Help] ⇨ [Version Information]

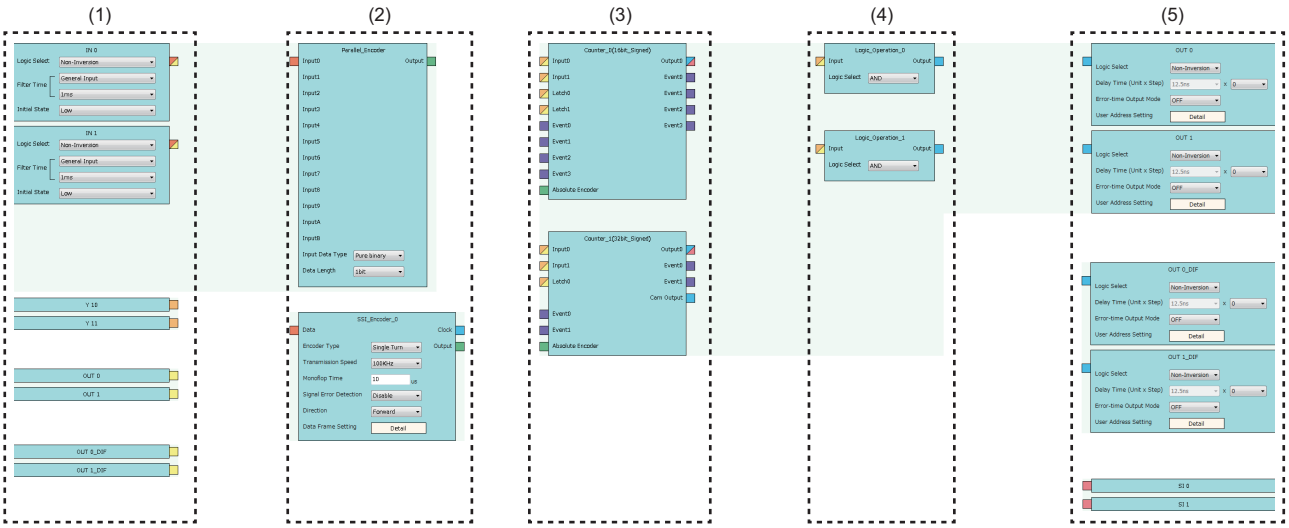
9 CREATING A HARDWARE LOGIC

This chapter describes how to create a hardware logic.

9.1 Main Blocks in the Hardware Logic Outline Window

With the flexible high-speed I/O control module, various controls are possible by arranging multi function counter blocks and various function blocks and linking these blocks.

In the hardware logic outline window, all of external input blocks, Y device terminals, and OUT terminals are arranged in the first section and all of external output blocks and SI device terminals are arranged in the fifth section when a project is stated. No blocks are arranged in the second to fourth sections. Arrange blocks and link them according to the control to be executed with the flexible high-speed I/O control module.



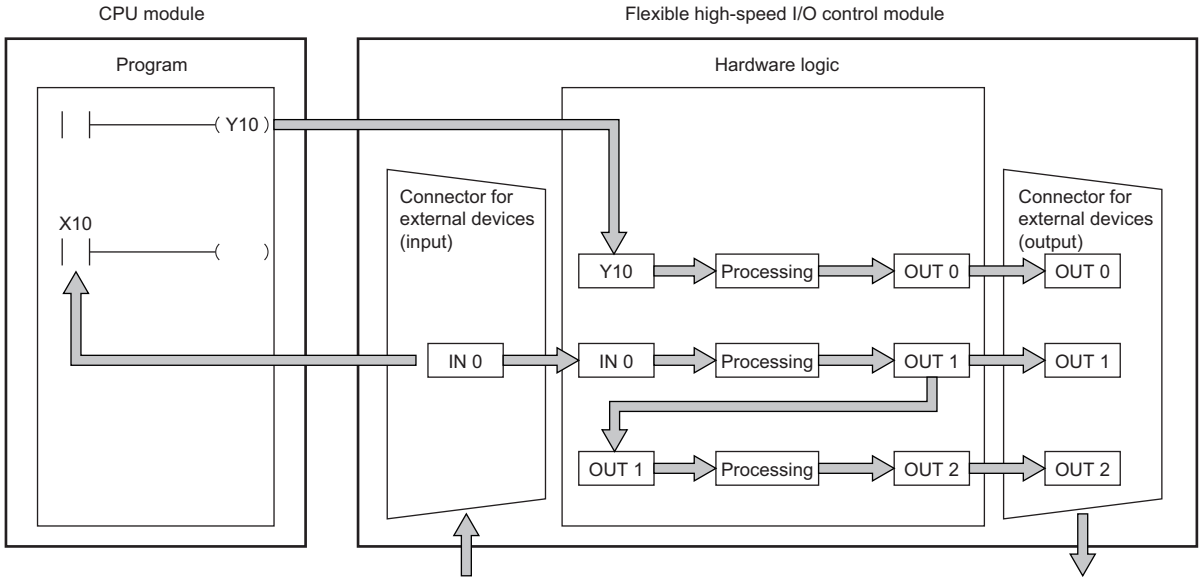
The following table shows sections where each main block can be arranged and the number of blocks that can be arranged in each section in the hardware logic outline window.

Section	Item name		Number of blocks that can be arranged*1	Remarks
First section	External input block		(12)	—
	Y device terminal		(16)	General command 0 to General command F (Y10 to Y1F) can be used as input signals.
	OUT terminal	DC output	(8)	Output signals from external output blocks in the fifth section can be used as input signals for the first section.
		Differential output	(6)	
Second section	Parallel encoder block		1	—
	SSI encoder block		2	—
Third section	Multi function counter block		8	—
Fourth section	Logical operation block		14	—
Fifth section	External output block	DC output	(8)	"OUT 0" to "OUT 7" are for DC output.
		Differential output	(6)	"OUT 0_DIF" to "OUT 5_DIF" are for differential output.
	SI device terminal		(8)	—

*1 The number in () indicates the number of blocks that are arranged by default and no additional blocks can be arranged.

Relationship of I/O in the hardware logic

This section describes the relationship between the I/O in the hardware logic and the I/O of X/Y devices and of the connectors for external devices.



Input terminal		Output terminal	
Y 10	Y device terminal	OUT 0	External output block
IN 0	External input block	OUT 1	External output block
OUT 1	OUT terminal	OUT 2	External output block

■Signal status name

In the flexible high-speed I/O control module, each signal status is called as shown below.

Signal status	Name	
Status of input signals from external devices	ON	OFF
Status of internal signals (terminals) of the hardware logic	High	Low
Status of DC output signals to external devices	ON	OFF
Status of differential output signals to external devices	High	Low

Link combination

The terminals to which the terminals of each main block can be linked are predetermined. An input terminal and an output terminal in the same color can be linked. Input terminals or output terminals cannot be linked each other.
The following table lists the combinations.

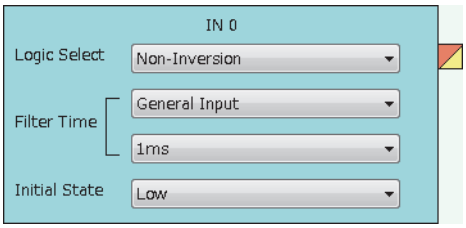
Output side		Input side		Color
Block name	**Terminal name**	**Block name**	**Terminal name**	
External input block	Output	Parallel encoder block	Input	Coral
		Multi function counter block	Input	Butterfly yellow
			Latch	
		Logical operation block	Input	
		SSI encoder block	Data	Coral
Y device terminal	Y	Multi function counter block	Input	Pale orange
			Latch	
		Logical operation block	Input	
OUT terminal	OUT OUT_DIF	Multi function counter block	Input	Butterfly yellow
			Latch	
		Logical operation block	Input	
Parallel encoder block	Output	Multi function counter block	Absolute Encoder	Celadon
SSI encoder block	Clock	External output block	OUT_DIF	Vermeer
	Output	Multi function counter block	Absolute Encoder	Celadon
Multi function counter block	Output	External output block	OUT	Vermeer
			OUT_DIF	
		SI device terminal	SI	Empire rose
	Event	Multi function counter block	Event	Columbine blue
	Cam Output	External output block	OUT	Vermeer
			OUT_DIF	
Logical operation block	Output	External output block	OUT	Vermeer
			OUT_DIF	

If multiple output terminals are linked to one input terminal, OR processing is executed on all input signals. If one output terminal is linked to multiple input terminals, the same signals are output for all the input terminals.

External input block

Outline

In the first section in the hardware logic outline window, 12 external input blocks ("IN 0" to "IN B") are arranged by default. Select which signal (among "IN 0" to "IN B") input from the connector for external devices is to be used as an input signal in the hardware logic. The selected input signal is output from the output terminal of the external input block through the filter. The output signal can be input to the input terminal of another block.



The external input block has the following functions.

- When "Logic Select" is set to "Inversion", inverted signals are output.
- The digital filter reduces the effect of external noise.
- The signal selected as an initial state is output when hardware logic control stops.

Parameter

The following table shows the parameters of the external input block.

Variable name	Data type	Valid range	Default value	Description
Logic Select	Bit	Inversion Non-Inversion	Non-Inversion	Set Non-Inversion or Inversion for input signals.
Filter Time	Word	☞ Page 107 "Filter Time"	• General Input (Pulse input mode) • 1ms (Input response time/counting speed)	Select a type of the filter time. The filter time corresponding to the input response time of general-purpose input or the counting speed of each pulse input mode can be set.
Initial State	Bit	Low High	Low	Set the signal status during a hardware logic control stop to Low fixed or High fixed.

■"Filter Time"

General-purpose input or pulse input count can be selected for "Filter Time".

• General-purpose input (General Input 0μs to General Input 5ms)

Set this method to reduce noise. When a pulse width is less than the setting value of "Filter Time", the pulse is not detected as an input signal. If the setting value is too large, pulses other than noise cannot be detected. Thus, set the filter time suitable for the operating environment.

Input response time								
0μs	10μs	50μs	0.1ms	0.2ms	0.4ms	0.6ms	1ms (default value)	5ms

• Pulse input count (1-Phase Multiple of 1 (CW/CCW) 10kpps to 2-Phase Multiple of 4 8000kpps)

Set this method to count input pulses. A setting according to the pulse input mode and counting speed prevents incorrect count.

Pulse input mode	Counting speed							
1-Phase Multiple of 1 (CW/CCW)	10kpps (default value)	100kpps	200kpps	500kpps	1000kpps	2000kpps	—	—
1-Phase Multiple of 2	10kpps (default value)	100kpps	200kpps	500kpps	1000kpps	2000kpps	4000kpps	—
2-Phase Multiple of 1	10kpps (default value)	100kpps	200kpps	500kpps	1000kpps	2000kpps	—	—
2-Phase Multiple of 2	10kpps (default value)	100kpps	200kpps	500kpps	1000kpps	2000kpps	4000kpps	—
2-Phase Multiple of 4	10kpps (default value)	100kpps	200kpps	500kpps	1000kpps	2000kpps	4000kpps	8000kpps

■Setting method of "Filter Time"

1. Select a pulse input mode in the upper list box.

2. Select an item in the lower list box.

• When "General Input" has been selected in the upper list box, select an input response time.

• When an item other than "General Input" has been selected in the upper list box, select a counting speed.

If the item in the upper list box is changed to another one after an item is selected in the lower list box, the selection status of the lower list box returns to the default value.

■Minimum value of the pulse width that may be taken in as input

For general-purpose input, noise or others may be taken in as input depending on the filter time setting. The following table lists the minimum values of the pulse width that may be taken in as input for each filter time.

Filter time	Minimum value of the pulse width that may be taken in as input
10μs	6μs
50μs	32μs
0.1ms	0.06ms
0.2ms	0.12ms
0.4ms	0.24ms
0.6ms	0.36ms
1ms	0.6ms
5ms	3ms

■Link with SSI encoder blocks

When an external input block is linked with the "Data" terminal of an SSI encoder block, the "Filter Time" of the external input block is automatically changed according to the setting value of "Transmission Speed" of the SSI encoder block. Additionally, if the setting value of "Transmission Speed" of the SSI encoder block after linked is changed, the "Filter Time" of the external input block is automatically changed according to the new value.

When the link between the external input block and the "Data" terminal of the SSI encoder block is deleted, the "Filter Time" of the external input block returns to the default value.

■"Initial State"

When ON signals are constantly input from external devices during a hardware logic control stop, a rise is detected in an input signal event detection block at a hardware logic control start. To prevent rise detection at a hardware logic control start, set "Initial State" to "High".

Output

The following table shows the output of the external input block.

Variable name	Data type	Linkable block	Output value	Description
Output	Bit	• Parallel encoder • Multi function counter • Logical operation • SSI encoder	0, 1	Outputs the signals that have passed the filter. Selecting "Logic Select" outputs inverted signals.

Y device terminal

Outline

In the first section in the hardware logic outline window, 16 Y device terminals ("Y 10" to "Y 1F") are arranged by default. The ON/OFF states of General command 0 to General command F (Y10 to Y1F) are output as signals and used as inputs in the hardware logic. Select ON or OFF of General command 0 to General command F (Y10 to Y1F) with a program.

Output

The following table shows the output of the Y device terminal.

Variable name	Data type	Linkable block	Output value	Description
Input	Bit	• Multi function counter • Logical operation*1	0, 1	Outputs the ON/OFF states of General command 0 to General command F (Y10 to Y1F) as signals.

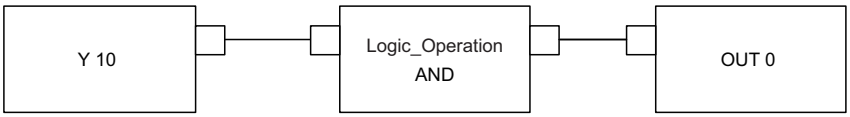
*1 A logical operation block can be linked only when an OUT terminal is not linked to the logical operation block.

Restriction

The timing of when signals output from Y device terminals are input to the link destination input terminal may delay due to the scan time or other causes. To input the signals to multiple connection destinations at the same time, using an external input block to which an external input signal is assigned is recommended.
For details on the external input block, refer to the following.
☞ Page 106 External input block

Point

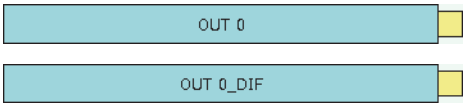
To use the flexible high-speed I/O control module as an output module, link blocks in the hardware logic outline window as shown below.



OUT terminal

Outline

In the first section in the hardware logic outline window, eight OUT terminals for DC output ("OUT 0" to "OUT 7") and six OUT terminals for differential output ("OUT 0_DIF" to "OUT 5_DIF") are arranged by default.
Signals output from external output blocks in the fifth section can be used as inputs in the hardware logic. For details on the external output block, refer to the following.
☞ Page 123 External output block



Output

The following table shows the output of the OUT terminal.

Variable name	Data type	Linkable block	Valid range	Description
Input	Bit	• Multi function counter • Logical operation*1	0, 1	When no external output blocks are linked, no signals are output from this terminal.

*1 Any of OUT 0 to OUT 7 or OUT 0_DIF to OUT 5_DIF can be linked to a logical operation block when a Y device terminal is not linked to the logical operation block.

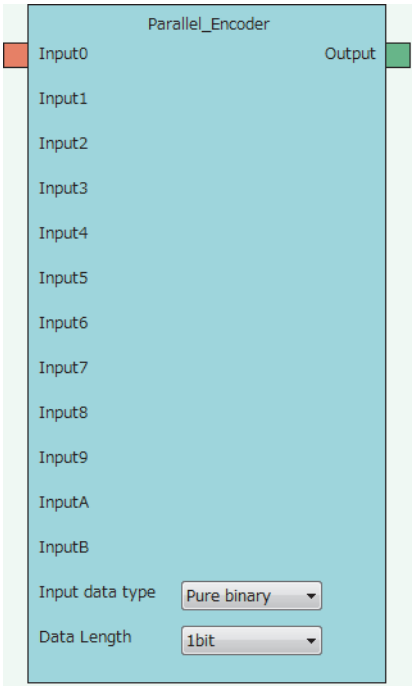
Restriction

When "Logic Select" of an external output block is set to "Inversion", signals input to the external output block are inverted and output from the OUT terminal.
For details on the external output block, refer to the following.
☞ Page 123 External output block

Parallel encoder block

Outline

In the second section in the hardware logic outline window, one parallel encoder block ("Parallel_Encoder") can be arranged. The parallel encoder block transmits data with the encoder for parallel transmission and receives the data of the bit points set in the data length setting as the data of Input Data Type to convert this data into word data.



Input

The following table shows the inputs of the parallel encoder block.

Variable name	Data type	Linkable block	Valid range	Description
Input 0	Bit	External input	0, 1	These are input terminals of the parallel encoder. When the data length is changed, the number of displayed Input terminals is changed according to the data length. Then, the Input terminals are automatically linked to external input blocks in order from the first one ("IN 0"). The order of linking the Input terminals and the external input blocks cannot be changed.
Input 1				
Input 2				
Input 3				
Input 4				
Input 5				
Input 6				
Input 7				
Input 8				
Input 9				
Input A				
Input B				

Parameter

The following table shows the parameters of the parallel encoder block.

Variable name	Data type	Valid range	Default value	Description
Input Data Type	Word	Pure binary Gray code BCD	Pure binary	Set the input data type of the parallel interface. • Pure binary • Gray code • BCD
Data Length	Word	1 bit to 12 bit	1bit	Set the input data length for the parallel encoder. When the trigger for transfer timing is used for BCD or pure binary, only input data of up to 11 bits can be used.

■Link for using the parallel encoder block

The input from an encoder is stored as a preset value of the counter timer block. Because the preset value is not automatically applied to "Count Value", performing the preset function is required. Thus, when using the parallel encoder block, always link it to the "PRESET" terminal of the counter timer block.

For details on the counter timer block, refer to the following.

☞ Page 145 Counter timer block

Restriction

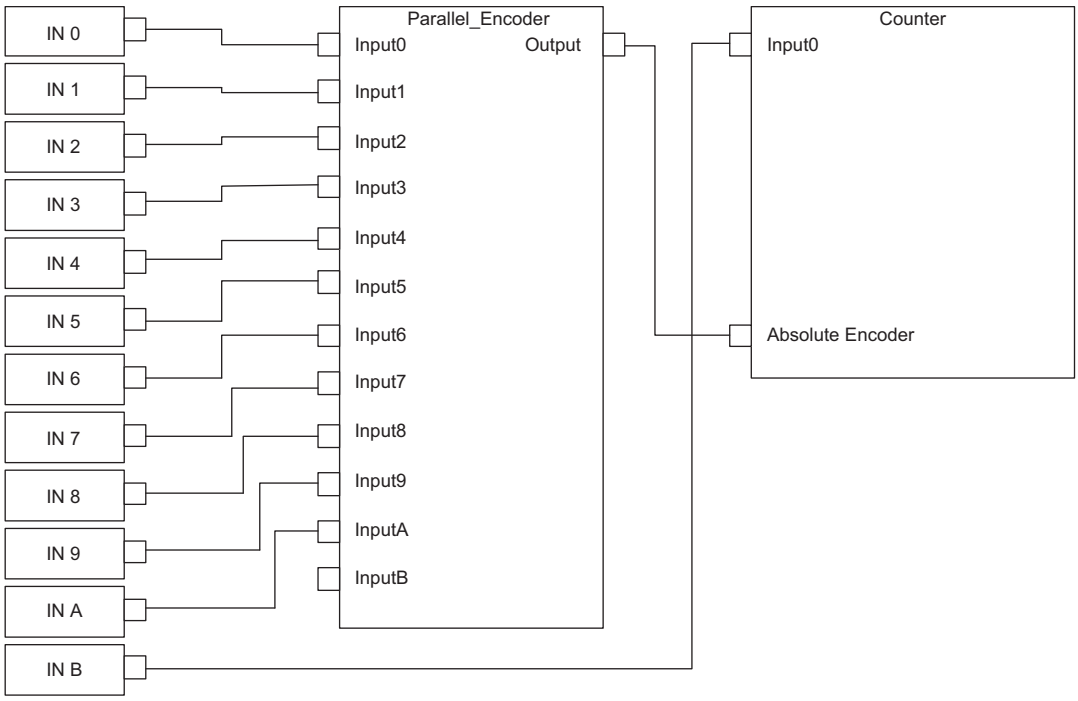
- There are the following types of multi function counter block which is linked from a parallel encoder block: 16 bits and 32 bits. When the parallel encoder block is linked to the "Absolute Encoder" terminal of a 16-bit multi function counter block, "Preset Value" of "Counter_Timer_0", out of two counter timer blocks in the multi function counter block detail window, is updated. Make sure to link the parallel encoder block to the "PRESET" terminal of "Counter_Timer_0". For details on the multi function counter block, refer to ☞ Page 127 Multi Function Counter Block.
- When the parallel encoder block is linked to the "Absolute Encoder" terminal of a 32-bit multi function counter block, do not change the preset value of "Counter_Timer_0" in the Multi function counter block detail window from 0 (default value). In addition, do not set "User Address" of the preset value of "Counter_Timer_0". When these settings are configured, the input from an encoder is not normally stored as a preset value.

■Setting and link of the encoder for which Input Data Type is set to Pure binary or BCD

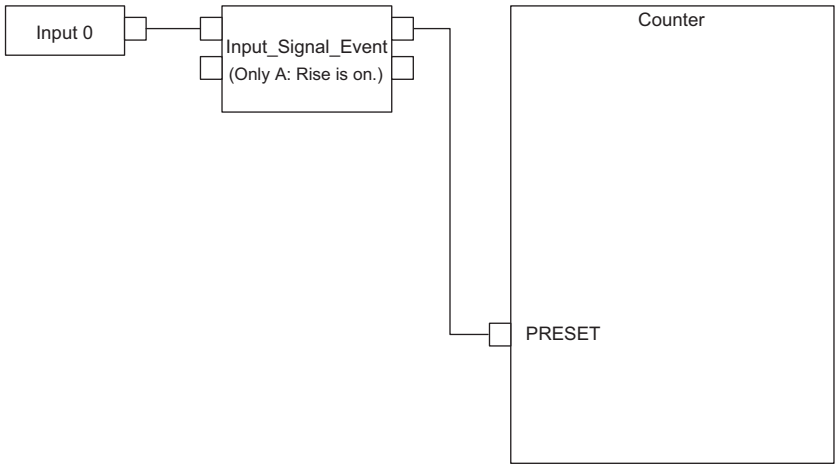
When data is input from the encoder for which Input Data Type is set to Pure binary or BCD, an error of 2 bits or more is generated depending on the timing of reading data. Because of this, when data is input from the encoder for which Input Data Type is set to Pure binary or BCD, specifying the read timing using a trigger signal for transfer timing is recommended.
To specify the read timing, follow the instructions below.

- Set "Data Length" to 11 bits or less.
- Link the terminal outputting the transfer timing signal to the "PRESET" terminal of the counter timer block.

■Link diagram of the hardware logic outline window



■Link diagram of the multi function counter block detail window



Output

The following table shows the output of the parallel encoder block.

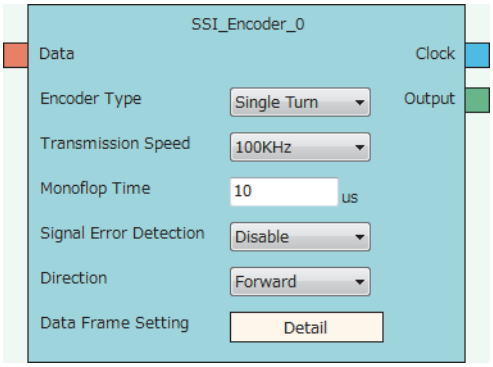
Variable name	Data type	Linkable block	Output value	Description
Output	Word	Multi function counter	0 to 4095	Inputs the value from the parallel encoder to the "Absolute Encoder" terminal to use the value as a preset value of the multi function counter.

SSI encoder block

Outline

In the second section in the hardware logic outline window, two SSI encoder blocks (SSI_Encoder_☐) can be arranged. The SSI encoder blocks perform serial communication with the absolute encoder having the SSI (Synchronous Serial Interface) output and acquire position data. The acquired position data is stored as a count value of the multi function counter block linked to this block.

- When "Signal Error Detection" is set to "Enable", a signal error detection processing is performed. If an error occurs on the external wiring to the SSI encoder, the SSI encoder block ☐ DATA signal wire reverse error (error code: 109☐H) or the SSI encoder block ☐ DATA signal error (error code: 10A☐H) is output.
- When "Parity" of "Data Frame Setting" is set to "Even" or "Odd", a parity check is performed. If an error is detected by the parity check, the SSI encoder block ☐ parity error (error code: 10B☐H) is output.
- If any of the above errors (error code: 109☐H to 10B☐H) is output during data receipt from the absolute encoder, the count value of the multi function counter block linked to this block does not change. The position data is reflected to the count value when data has been received properly at next transmission.



Input

The following table shows the input of the SSI encoder block.

Variable name	Data type	Linkable block	Valid range	Description
Data	Bit	External input	0, 1	Inputs data from the SSI encoder.

Parameter

The following table shows the parameters of the SSI encoder block.

Variable name	Data type	Valid range	Default value	Description
Encoder Type	Word	Single Turn Multi Turn	Single Turn	Set the type of the SSI encoder. • Single Turn • Multi Turn
Transmission Speed	Word	100KHz 200KHz 300KHz 400KHz 500KHz 1.0MHz 1.5MHz 2.0MHz	100KHz	Set the frequency of the clock signal to perform synchronous data communication with the SSI encoder.
Monoflop Time	Word	10 to 10000 (µs)	10 (µs)	Indicates the time until the next communication is ready to start after the output of the last clock signal. Set the monoflop time according to the specifications of the SSI encoder to be connected. For details on the monoflop time, refer to the following. ☞ Page 120 Monoflop time
Signal Error Detection	Word	Disable Enable	Disable	Set whether to detect an error (disconnection, short-circuit) of the data signal wire externally connected to the SSI encoder. • Error detection disabled: Disable • Error detection enabled: Enable For details on the signal error detection, refer to the following. ☞ Page 121 Signal error detection
Direction	Word	Forward Reverse	Forward	The counting direction of received data from the SSI encoder can be changed by setting this item. • Forward • Reverse For details on the counting direction setting, refer to the following. ☞ Page 120 Counting direction setting
Data Frame Setting	—	—	—	Click the [Detail] button to open the "Data Frame Setting" window in which the details of a data frame can be set.

• Parameters of "Data Frame Setting"

Variable name	Data type	Valid range	Default value	Description
Input Data Type	Word	Pure binary Gray code	Pure binary	Set the type of input data from the SSI encoder. • Pure binary • Gray code*3
Data Frame Length	Word	1 to 32 (bit)	1 (bit)	Specify the effective bit length of a received data frame from the SSI encoder.*1
Multi Turn Data Length	Word	0 to 32 (bit)	0 (bit)	Specify the effective bit length of multi turn data.*1 When "Encoder Type" is set to "Multi Turn", this setting is enabled. When this setting is disabled, a default value is set.
Multi Turn Start Bit	Word	0 to 31 (bit)	0 (bit)	Specify the start bit position of multi turn data. When "Encoder Type" is set to "Multi Turn", this setting is enabled. When this setting is disabled, a default value is set.
Encoder Resolution	Word	0 to 4294967295	0	Set the encoder resolution to use the encoder with its resolution of single turn data not equal to 2^n (n: single turn data length).*2 When the resolution is equal to 2^n, the setting change from the initial value (0) is not required. (When 0 is set, the resolution is regarded as equal to 2^n.) When "Encoder Type" is set to "Multi Turn" and "Input Data Type" is set to "Gray code", this setting is disabled. When this setting is disabled, a default value is set.
Single Turn Data Length	Word	0 to 32 (bit)	0 (bit)	Specify the effective bit length of single turn data.*1
Single Turn Start Bit	Word	0 to 31 (bit)	0 (bit)	Specify the start bit position of single turn data. When "Encoder Type" is set to "Single Turn", this setting is enabled. When this setting is disabled, a default value is set.
Parity	Word	None Even Odd	None	Set whether to perform the parity check or the type of the parity check (even or odd) according to the SSI encoder to be connected. • No parity check: None • Even parity: Even • Odd parity: Odd

*1 Set values so that the total of set values for "Multi Turn Data Length" and "Single Turn Data Length" is equal to or smaller than the value set for "Data Frame Length". Note that the parity bit length is not included in these values.

*2 A value larger than the maximum value representable by "Single Turn Data Length" cannot be set for "Encoder Resolution".

*3 When using the encoder with the encoder type being multi turn and the input data type being gray code, make sure that its resolution of single turn data is equal to 2^n.

Output

The following table shows the outputs of the SSI encoder block.

Variable name	Data type	Linkable block	Output value	Description
Clock	Bit	External output	0, 1	Outputs the clock signal to perform synchronous data communication with the SSI encoder. When an SSI encoder block is arranged in the hardware logic outline window, the "Clock" terminal of the SSI encoder block and the "Input" terminal of an external output block are automatically linked. The link cannot be deleted or changed. The following are the link destinations. • Serial_Encoder0: OUT 0_DIF • Serial_Encoder1: OUT 1_DIF
Output	Word	Multi function counter*1	0 to 4294967295	Sets the position data acquired from the SSI encoder to a count value of the multi function counter block linked.

*1 The "Absolute Encoder" terminal of a 32-bit unsigned multi function counter block can be linked.

Restriction

The refreshing cycle of a count value is calculated by the following formula because the module processing time fluctuates within the range of 0 to 100μs.

Refreshing cycle = (Data frame length + P + 1) × Clock cycle + Monoflop time + Module processing time (0 to 100μs)

• P: 1 (for with parity) or 0 (for without parity)

• Clock cycle: Inverse of the transmission speed (for the transmission speed of 100kHz: 1/100000s = 10μs)

Note that if an SI device terminal is used, up to 200μs may be added to the refreshing cycle above as a delay time of the refreshing.

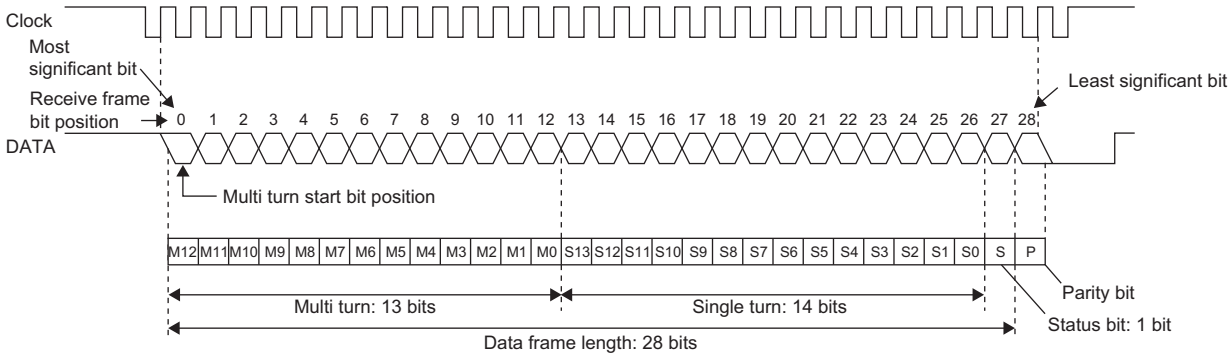
Setting examples of the SSI encoder block

This section shows setting examples of the SSI encoder block suitable for a receive frame from the SSI encoder and communication specifications.

■Multi turn

The following example is for the receive frame of a multi turn encoder. The receive frame consists of the elements below.

- Multi turn: 13 bits
- Single turn: 14 bits
- Status bit: 1 bit
- Parity bit: 1 bit



- Parameter

Encoder specifications[*1]		SSI encoder block setting		Remarks
		Item	Setting value	
Encoder type	Multi turn	Encoder Type	Multi Turn	—
Transmission speed	1MHz	Transmission Speed	1.0MHz	—
Monoflop time	16µs	Monoflop Time	16	—
—	—	Signal Error Detection	Enable	Set "Enable" to use the signal error detection. Set "Disable" not to use it.
—	—	Direction	Forward	Set "Forward" to count a position data from the SSI encoder in the forward direction. Set "Reverse" to reverse the counting direction.

*1 For details on the encoder specifications, refer to the manual for the encoder used.

- Parameters of "Data Frame Setting"

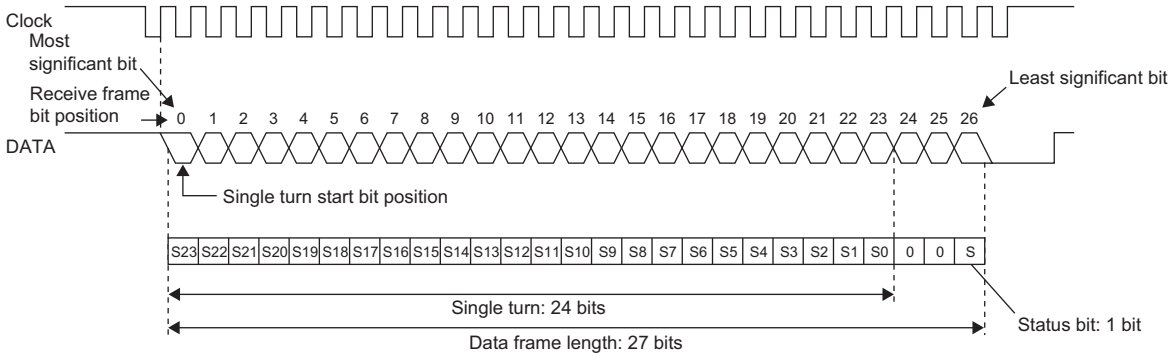
Encoder specifications[*2]		SSI encoder block setting		Remarks
		Item	Setting value	
Data type	Gray	Input Data Type	Gray code	—
Data frame length	28 bits	Data Frame Length	28	The parity bit is not included.
Multi turn data length	13 bits	Multi Turn Data Length	13	—
Multi turn data start bit position	0	Multi Turn Start Bit	0	Specify the receive frame bit position where multi turn data starts.
Encoder resolution	16384	Encoder Resolution	0	Changing the setting value from its default (0) is not required because the single turn data length is 14 bits and the encoder resolution is 16384 (= 2^{14}).
Single turn data length	14 bits	Single Turn Data Length	14	—
Single turn data start bit position	13	Single Turn Start Bit	0	Setting is not required.
Parity check	Odd parity	Parity	Odd	—

*2 For details on the encoder specifications, refer to the manual for the encoder used.

■Single turn

The following example is for the receive frame of a single turn encoder. The receive frame consists of the elements below.

- Single turn: 24 bits
- Status bit: 1 bit
- Parity bit: None



- Parameter

Encoder specifications*1		SSI encoder block setting		Remarks
		Item	Setting value	
Encoder type	Single turn	Encoder Type	Single Turn	—
Transmission speed	2MHz	Transmission Speed	2.0MHz	—
Monoflop time	10µs	Monoflop Time	10	—
—	—	Signal Error Detection	Disable	Set "Enable" to use the signal error detection. Set "Disable" not to use it.
—	—	Direction	Reverse	Set "Forward" to count a position data from the SSI encoder in the forward direction. Set "Reverse" to reverse the counting direction.

*1 For details on the encoder specifications, refer to the manual for the encoder used.

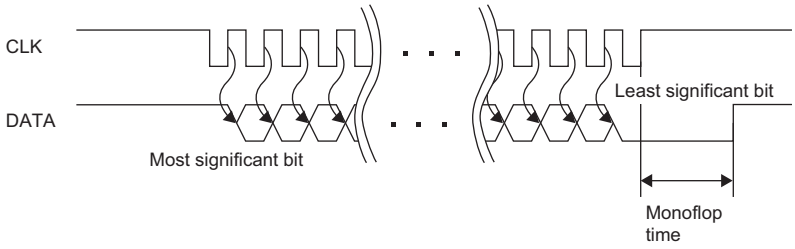
- Parameters of "Data Frame Setting"

Encoder specifications*2		SSI encoder block setting		Remarks
		Item	Setting value	
Data type	Pure binary	Input Data Type	Pure binary	—
Data frame length	27 bits	Data Frame Length	27	—
Multi turn data length	—	Multi Turn Data Length	0	Setting is not required.
Multi turn data start bit position	—	Multi Turn Start Bit	0	Setting is not required.
Encoder resolution	16777216	Encoder Resolution	0	Changing the setting value from the initial value (0) is not required because the single turn data length is 24 bits and the encoder resolution is 16777216 (= 2^{24}).
Single turn data length	24 bits	Single Turn Data Length	24	—
Single turn data start bit position	0	Single Turn Start Bit	0	Specify the receive frame bit position where single turn data starts.
Parity check	—	Parity	None	—

*2 For details on the encoder specifications, refer to the manual for the encoder used.

Monoflop time

The monoflop time indicates the time set aside to refresh position data of the SSI encoder. The time is stipulated by an encoder type. If the monoflop time is set to be shorter than the stipulated time, correct position data cannot be received.
When CLK transmission from the connected device is stopped by the monoflop time, the DATA signal from the SSI encoder returns to High. This state indicates that the SSI encoder waits to start communication. At the timing the first fall of CLK from this state is detected, position data is refreshed to the latest value. And then, at a rise of CLK, data transmission resumes in order from the most significant bit.
With SSI communication specifications, after the receipt of the last bit of the receive frame, if CLK transmission resumes before the encoder-wait-to-start-communication state is established, the position data of the previous receive frame is sent from the encoder and received in the flexible high-speed I/O control module. In other words, if CLK transmission resumes before the monoflop time elapsed, the latest position data is not latched in the encoder, and thus the latest position data cannot be received in the flexible high-speed I/O control module.

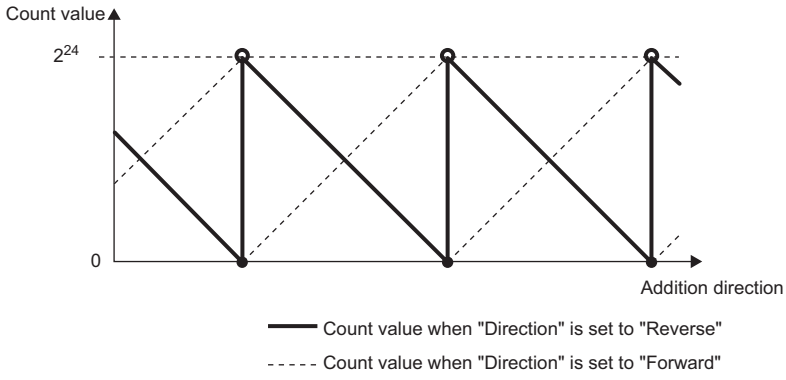


Counting direction setting

Set the counting direction of received position data from the SSI encoder.
When "Direction" is set to "Reverse", the position data from the encoder is processed using the calculation formulas in the table below.

Encoder type	Calculation formula
Multi turn	Count value = ($2^m \times$ Encoder resolution - 1) - Position data (m: Multi turn data length)
Single turn	Count value = (Encoder resolution - 1) - Position data

Ex.
The following is the example of using the encoder with multi turn data length of 12 bits and encoder resolution of 4096 (= 12 bits) and counting in the addition direction.
Count value = ($2^{12} \times 4096$ - 1) - Position data = (2^{24} - 1) - Position data



Receive data monitor

Out of the data frame received from the SSI encoder, the information for the number of bits specified with "Data Frame Length" is stored in the following buffer memory areas. (The parity bit is not included.)

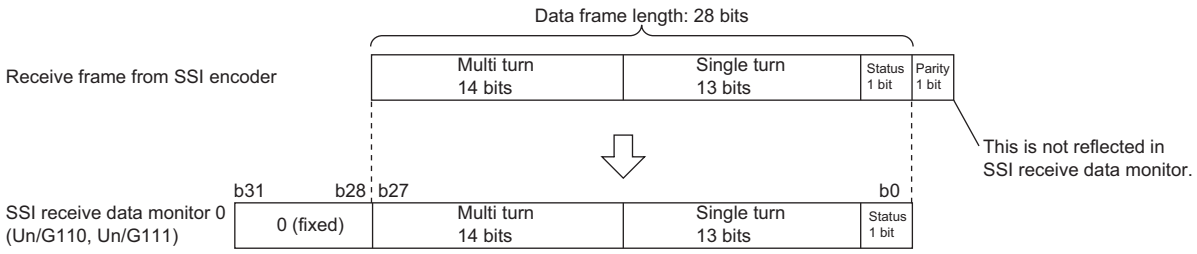
Buffer memory address	SSI encoder block
Un\G110, Un\G111	SSI_Encoder_0
Un\G114, Un\G115	SSI_Encoder_1

Some SSI encoders output not only position data (multi turn data, single turn data) but also status data in the data frame. The status of encoder can be checked by reading out values of above buffer memory areas with a program.
In addition, when a count value is not refreshed properly, its cause (whether it is a receive data error or a parameter setting error) can be identified by checking multi turn data and single turn data contained in the receive data monitor.

Ex.

The example shows the receive data monitor of when the SSI encoder with the data frame of the following configuration is used.

- Data frame length: 28 bits
- Multi turn data: 14 bits
- Single turn data: 13 bits
- Status: 1 bit
- Parity bit: 1 bit



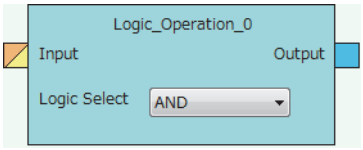
Signal error detection

An error of the external wiring to the SSI encoder can be detected.
When "Signal Error Detection" is set to "Enable", a signal error detection processing is performed. If an error occurs on the external wiring to the SSI encoder, the SSI encoder block ☐ DATA signal wire reverse error (error code: 109☐H) or the SSI encoder block ☐ DATA signal error (error code: 10A☐H) is output.
In addition, in the cycle where data is received from the SSI encoder with an error detected, the count value of the multi function counter block linked to the SSI encoder block is not refreshed.

Logical operation block

Outline

In the fourth section in the hardware logic outline window, 14 logical operation blocks ("Logic_Operation_0" to "Logic_Operation_D") can be arranged.
Any logical operation of AND operation, OR operation, or XOR operation is executed for all signals input to the "Input" terminal.



Restriction

Even though a project including an unlinked logical operation block for which Logic Select is set to AND (default) is saved, the arrangement status is not saved. When the saved project is opened, the logical operation block is not displayed. In addition, verifying with the module is executed on the assumption that the block is not arranged.

Input

The following table shows the input of the logical operation block.

Variable name	Data type	Linkable block	Valid range	Description
Input	Bit	• External input • OUT*1*2 • Y device*2	0, 1	Multiple signals can be input to the "Input" terminal. Operations are executed for all input signals.

*1 When a logical operation block is linked with an OUT terminal, any of OUT 0 to OUT 7 or OUT 0_DIF to OUT 5_DIF can be used.
*2 Either of an OUT terminal or Y device terminal can be linked with a logical operation block.

Parameter

The following table shows the parameter of the logical operation block.

Variable name	Data type	Valid range	Default value	Description
Logic Select	Word	AND OR XOR	AND	Set the operation type for input signals.

Output

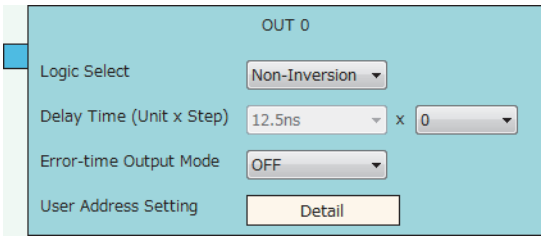
The following table shows the output of the logical operation block.

Variable name	Data type	Linkable block	Output value	Description
Output	Bit	External output	0, 1	Outputs the operation results of input signals.

External output block

Outline

In the fifth section in the hardware logic outline window, eight external output blocks for DC output ("OUT 0" to "OUT 7") and six external output blocks for differential output ("OUT 0_DIF" to "OUT 5_DIF") are arranged by default.
The result of the operation from the first to the fourth section in the hardware logic is output from the connector for external devices (OUT 0 to OUT 7, OUT 0_DIF to OUT 5_DIF).



The external output block has the following functions.

- When "Logic Select" is set to "Inversion", inverted signals are output.
- A delay between signals caused by different external interface circuits can be adjusted by setting a delay time.
- When an error occurs in the CPU module, signals are output according to the output setting specified with "Error-time Output Mode".

Input

The following shows the input of the external output block.

Variable name	Data type	Linkable block	Description
Input	Bit	• Multi function counter • Logical operation	Executes OR processing for all signals input to the "Input" terminal.
	Bit	SSI encoder	Only OUT 0_DIF and OUT 1_DIF are automatically linked with "Clock" of the SSI encoder block.

Parameter

The following table shows the parameters of the external output block.

Variable name	Data type	Valid range	Default value	Description
Logic Select	Bit	Non-Inversion Inversion	Non-Inversion	Set Non-Inversion or Inversion for input signals.
Delay Time (Step)	Word	0 to 64	0	Adjust the signal output timing. A delay time can be set with the combination of "Delay Time (Step)" and "Delay Time (Unit)". Setting the number of steps to 0 disables the delay.
Delay Time (Unit)	Word	12.5ns 25ns 50ns 0.1µs 1µs 10µs 100µs 1ms	12.5ns	Adjust the signal output timing. A delay time can be set with the combination of "Delay Time (Unit)" and "Delay Time (Step)".
Error-time Output Mode	Word	OFF ON HOLD	OFF	Set output signals at occurrence of an error in the CPU module to OFF fixed, ON fixed, or holding output status. This setting is also applied to output signals at a hardware logic control stop.
User Address Setting	—	—	—	Set the buffer memory addresses used in the external output block. Click the [Detail] button to open the "User Address Setting" window.

- Parameters of "User Address Setting"

Variable name	Data type	Valid range	Description
Enable Forced Output	Word	1000 to 1099	Specify the buffer memory address to enable or disable the forced output.*1 Whether the forced output is enabled or disabled can be set by setting the following values for the specified buffer memory.*2 0: Forced output disabled 1: Forced output enabled
Forced Output	Word	1000 to 1099	Specify the buffer memory address to set the status of the forced output signal.*1 Whether the signal status is set to off or on can be set by setting the following values for the specified buffer memory. 0: OFF output 1: ON output
External terminal monitor	Word	1000 to 1099	Specify the buffer memory address to store the external terminal status.*1 0: OFF output 1: ON output

*1 The available buffer memory addresses are common in OUT 0 to OUT 7 and OUT 0_DIF to OUT 5_DIF. Each external output block is assigned to the bits of the specified buffer memory as follows.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00		OUT 5_DIF	OUT 4_DIF	OUT 3_DIF	OUT 2_DIF	OUT 1_DIF	OUT 0_DIF	OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

*2 The external output block where Forced output enabled (1) is set outputs a signal according to the setting value (forced output value) of the buffer memory area specified with "Forced Output". The input from "Input" terminal is not reflected to the external output.

■Delay time

A delay time is calculated by multiplying "Delay Time(Unit)" by "Delay Time(Step)".

An error of one unit time may be generated in delay time. However, the error can be reduced by setting the delay time as shown below.

- Change the value of "Delay Time (Unit)" as small as possible.
- Set a large value for "Delay Time (Step)".

Ex.

The following table lists examples of the delay time of 20µs. Compared with example 2, an error is smaller in the setting of example 1.

Example	Delay Time(Step)	Delay Time(Unit)	Error
Example 1	1µs	20 steps	An error of maximum 1µs is generated in the output timing.
Example 2	10µs	2 steps	An error of maximum 10µs is generated in the output timing.

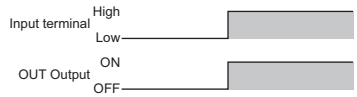
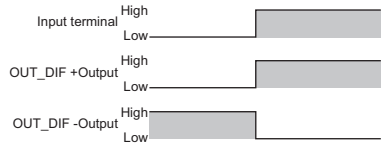
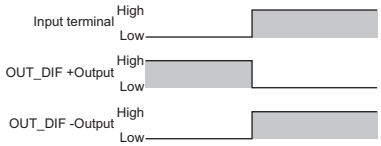
■Link with SSI encoder blocks

When an SSI encoder block is arranged in the hardware logic outline window, the "Clock" terminal of the SSI encoder block and the "Input" terminal of an external output block are automatically linked.

The default value is set for the setting value of the external output block automatically linked and the value cannot be changed.

High/Low states of external output signals

The following table lists the High/Low states of external output signals in each setting combination of input signals to external output blocks and "Logic Select".

Output type	"Logic Select"	
	"Non-Inversion"	"Inversion"
DC		
Differential		

When an error occurs in the CPU module, a signal is output according to the output setting of "Error-time Output Mode" independent of the setting of Inversion or Not-Inversion.

SI device terminal

Outline

In the fifth section in the hardware logic outline window, eight SI device terminals ("SI 0" to "SI 7") are arranged by default. When a signal is input to an SI device terminal, an interrupt request is output to the CPU module to start an interrupt program. The interrupt program corresponding to each SI device terminal needs to be set in GX Works2 in advance.

Output

The following table shows the output of the SI device terminal.

Variable name	Data type	Linkable block	Valid range	Description
Output	Bit	Multi function counter*1	0, 1	For details on interruption, refer to the following. ☞ Page 169 Setting intelligent function module interrupt pointers

*1 An SI device terminal can be linked to any of the Output terminals of the multi function counter block Counter_0 to Counter_7.

Point

When multiple SI device terminals are turned to High at the same time, the interrupt programs are started in order from the program corresponding to the terminal with a smaller number. When multiple SI device terminals are linked, link the terminals so that terminals corresponding to interrupt programs with higher priority have smaller numbers.

9.2 Multi Function Counter Block

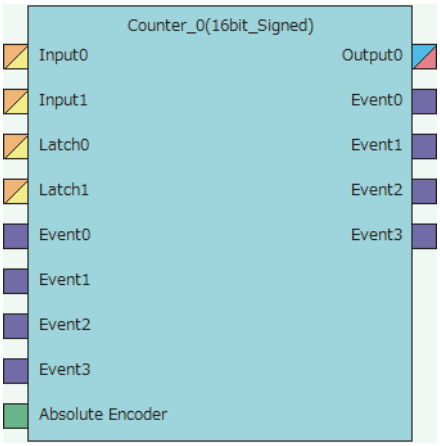
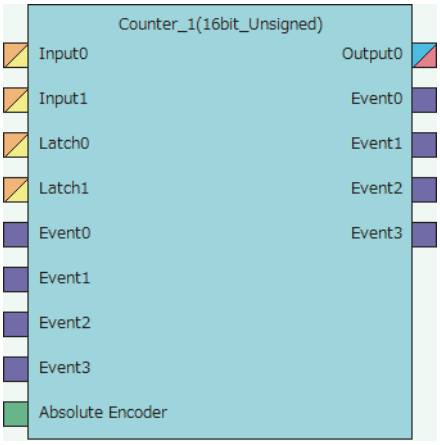
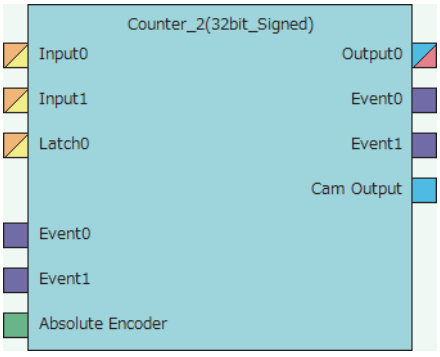
Outline

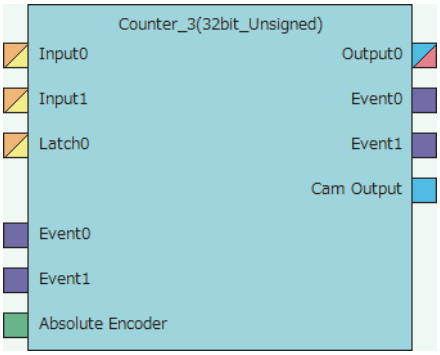
In the third section in the hardware logic outline window, up to eight multi function counter blocks ("Counter_0" to "Counter_7") can be arranged.

Set details on how to count pulses of input signals in a multi function counter block detail window. To shift to a multi function counter block detail window, double-click the corresponding block in the hardware logic outline window.

Type

There are the following four types of multi function counter blocks.

Name	Block diagram	Specifications			
		Available count value	Number of Latch terminals	Number of Event terminals	Availability of "Cam Output" terminal
Counter_☐(16bit_Signed) (16-bit signed multi function counter block)		16-bit signed value	2	4	×
Counter_☐(16bit_Unsigned) (16-bit unsigned multi function counter block)		16-bit unsigned value	2	4	×
Counter_☐(32bit_Signed) (32-bit signed multi function counter block)		32-bit signed value	1	2	○

Name	Block diagram	Specifications			
		Available count value	Number of Latch terminals	Number of Event terminals	Availability of "Cam Output" terminal
Counter_☐(32bit_Unsigned) (32-bit unsigned multi function counter block)		32-bit unsigned value	1	2	○

Input

The following table shows the inputs of the multi function counter block.

Variable name	Data type	Linkable block	Valid range	Description
Input 0 Input1	Bit	• External input • OUT • Y device	0, 1	The input terminals are for external input signals. The terminal executes OR processing for all signals input to the "Input☐" terminal.
Latch 0 Latch 1	Bit	• External input • OUT • Y device	0, 1	• The input terminals are for latch. The terminal executes OR processing for all signals input to the "Latch☐" terminal. • The "Latch 1" terminal can be used in 16-bit multi function counter blocks only.
Event 0 Event 1 Event 2 Event 3	Bit	Multi function counter*1	0, 1	• The input terminals are for events. The terminal executes OR processing for all signals input to the "Event☐" terminal. • The "Event 2" and "Event 3" terminals can be used in 16-bit multi function counter blocks only.
Absolute Encoder	Word	Parallel encoder	0 to 4095	Inputs the encoder value of the absolute encoder (parallel encoder block). The input encoder value is used as a preset value of the counter timer block in the multi function counter block detail window.
		SSI encoder	0 to 4294967295	Inputs the encoder value of the absolute encoder (SSI encoder block). The input encoder value is stored as a count value of the counter timer block in the multi function counter block detail window.

*1 Only the "Event☐" terminals of multi function counter blocks can be linked.

Output

The following table shows the outputs of the multi function counter block.

Variable name	Data type	Linkable block	Output value	Description
Output 0	Bit	• External output • SI device*2	0, 1	The output terminal is for external output signals and interruption.
Event 0	Bit	Multi function counter*1	0, 1	The output terminals are for events. The "Event 2" and "Event 3" terminals can be used in 16-bit multi function counter blocks only. The linkable blocks differ for each Event terminal in the multi function counter block detail window. (☞ Page 167 Event output terminal)
Event 1				
Event 2				
Event 3				
Cam Output	Bit	External output	0, 1	The output terminals are for external output signals. These terminals can be used in 32-bit multi function counter blocks only.

*1 Only the "Event☐" terminals of multi function counter blocks can be linked.
*2 Any of "SI ☐" terminals can be linked.

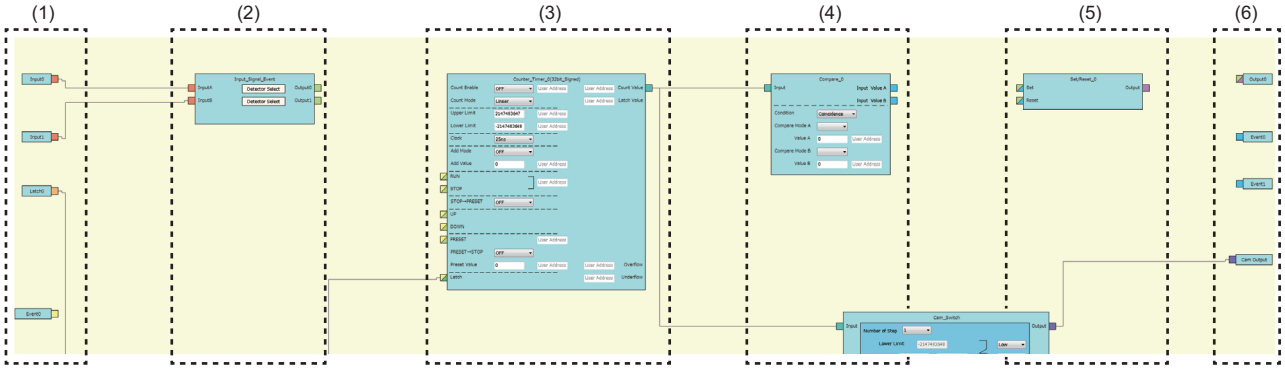
Point

When a 16-bit multi function counter block is arranged in the hardware logic outline window, two 16-bit counter timer blocks are arranged in the multi function counter block detail window. These two counter timer blocks can be simultaneously used. However, OR processing is executed on the outputs of these two counter timer blocks because a multi function counter block has only one output terminal.

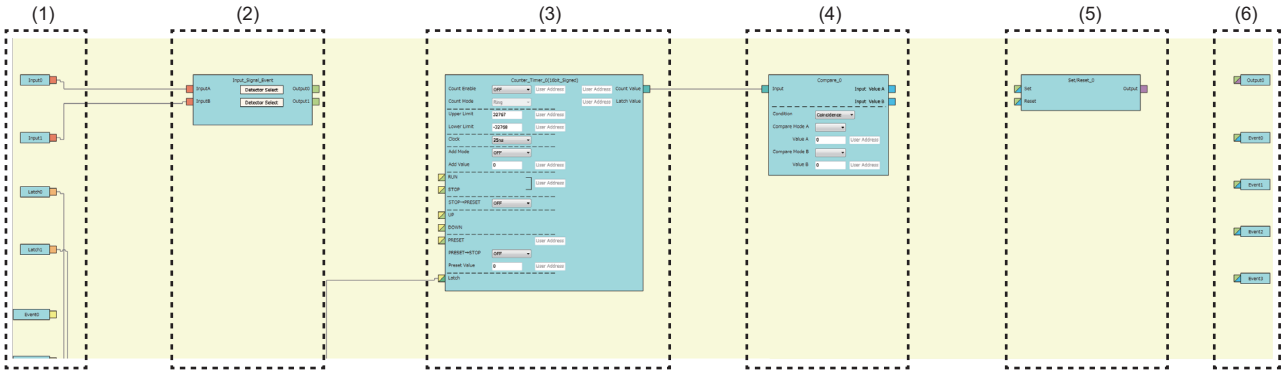
Internal blocks of multi function counter blocks

There are 12 types of internal blocks in a multi function counter block. Control operations can be freely customized by linking the internal blocks. When a multi function counter block is arranged in the hardware logic outline window, all internal blocks are arranged in the multi function counter block detail window.

- 32-bit multi function counter block detail window



- 16-bit multi function counter block detail window



Internal block list

The multi function counter internal blocks are as follows.

Section	Block name	Number of arranged items		Reference
		16-bit counter	32-bit counter	
First section	Input terminal	2	2	☞ Page 134 Input terminal
	Latch input terminal	2	1	☞ Page 134 Latch input terminal
	Event input terminal	4	2	☞ Page 135 Event input terminal
Second section	Input signal event detection block	1	1	☞ Page 136 Input signal event detection block
	Latch event detection block	1	1	☞ Page 143 Latch event detection block
Third section	Counter timer block	2	1	☞ Page 145 Counter timer block
Fourth section	Comparison block	2	1	☞ Page 158 Comparison block
	Cam switch block*1	0	1	☞ Page 161 Cam switch block
Fifth section	Set/reset block	2	1	☞ Page 165 Set/reset block
Sixth section	Output terminal	1	1	☞ Page 166 Output terminal
	Event output terminal	4	2	☞ Page 167 Event output terminal
	Cam switch output terminal	0	1	☞ Page 168 Cam switch output terminal

*1 The cam switch block is arranged across the fourth and fifth sections.

Link combination

An input terminal and output terminal in the same color can be linked among the internal blocks. Input terminals or output terminals cannot be linked each other.

The following table lists the combinations.

Output side		Input side		Color
Block name	**Terminal name**	**Block name**	**Terminal name**	
Input terminal	Input	Input signal event detection block	Input*1	Coral
Latch input terminal	Latch	Latch event detection block	Input*1	Pale orange
Event input terminal	Event	Counter timer block	RUN	Butterfly yellow
			STOP	
			UP	
			DOWN	
			PRESET	
			Latch	
Input signal event detection block	Output	Counter timer block	RUN	Hop green
			STOP	
			UP	
			DOWN	
			PRESET	
		Set/reset block	Set	
			Reset	
		Output terminal	Output	
		Event output terminal	Event*2	
Latch event detection block	Output	Counter timer block	Latch*1	Celadon
Counter timer block	Count Value	Comparison block	Input*1	Cyan blue
		Cam switch block	Input*1	
Comparison block	Output	Set/reset block	Set	Vermeer
			Reset	
		Event output terminal	Event	
Cam switch block	Output	Cam switch output terminal	Cam Output*1	Columbine blue
Set/reset block	Output	Output terminal	Output	Lilac

*1 The terminals are linked by default. The links cannot be deleted.

*2 The terminals can be linked when a 16-bit multi function counter block is used. They cannot be linked when a 32-bit multi function counter block is used.

If multiple output terminals are linked to one input terminal, OR processing is executed on all input signals. If one output terminal is linked to multiple input terminals, the same signals are output for all the input terminals.

■Restrictions on linking the same-color terminals for 16-bit multi function counter blocks

For 16-bit multi function counter blocks, linkable combinations of blocks and terminals are restricted even if the terminals are in the same color.

• Input signal event detection block and event output terminal

Input signal event detection block (output side)		Event output terminal (input side)	
Block name	**Terminal name**	**Block name**	**Terminal name**
Input_Signal_Event	Output 0	Event output terminal	Event 0
			Event 1
	Output 1	Event output terminal	Event 2
			Event 3

• Comparison block and set/reset block

Comparison block (output side)		Set/reset block (input side)	
Block name	**Terminal**	**Block name**	**Terminal name**
Compare_0	Upper terminal	Set/Reset_0	Set
			Reset
	Lower terminal	Set/Reset_0	Set
			Reset
Compare_1	Upper terminal	Set/Reset_1	Set
			Reset
	Lower terminal	Set/Reset_1	Set
			Reset

• Comparison block and event output terminal

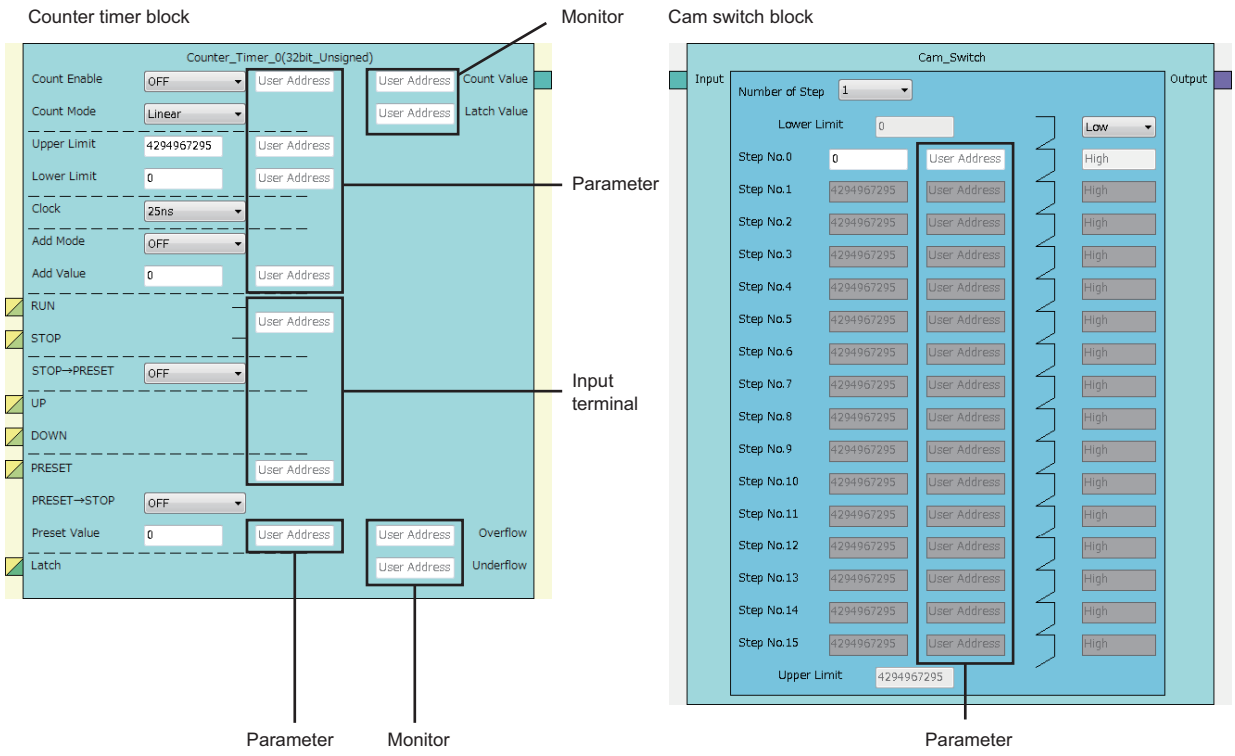
Comparison block (output side)		Event output terminal (input side)	
Block name	**Terminal**	**Block name**	**Terminal name**
Compare_0	Upper terminal	Event output terminal	Event 0
			Event 1
	Lower terminal	Event output terminal	Event 0
			Event 1
Compare_1	Upper terminal	Event output terminal	Event 2
			Event 3
	Lower terminal	Event output terminal	Event 2
			Event 3

• Counter timer block and comparison block (automatically linked in the following combinations by default)

Counter timer block (output side)		Comparison block (input side)	
Block name	**Terminal name**	**Block name**	**Terminal name**
Counter_Timer_0	Count Value	Compare_0	Input
Counter_Timer_1	Count Value	Compare_1	Input

Assignment of "User Address"

"User Address" can be set to particular internal blocks arranged in a multi function counter block detail window. By assigning buffer memory addresses to "User Address", the status of input terminals and parameter setting values can be changed with programs and values of the hardware logic can be monitored during the hardware logic control.



The application varies according to targets to which "User Address" is assigned.

Assignment target	Application	Description
Input terminal	Write	The value of a buffer memory area specified with "User Address" is written to the hardware logic in a high-speed (100μs) or a low-speed (1ms) period. Note that the input terminal status is not read to buffer memory areas. Follow the instructions below. Even if the input terminal status changes due to signals in the hardware logic, the values in the buffer memory areas do not change and they are written in a high-speed (100μs) or a low-speed (1ms) period. Thus, do not assign "User Address" to the terminals linked in the hardware logic. Do not use buffer memory addresses as the monitors of input terminals because the input terminal status is not read.
Parameter	Write	The value of a buffer memory area specified with "User Address" is written to the hardware logic in a high-speed (100μs) or a low-speed (1ms) period.
Monitor	Read	A value of the hardware logic is read in a high-speed (100μs) or a low-speed (1ms) period. The value of a buffer memory area specified with "User Address" cannot be changed by users.

Restriction

- A buffer memory address cannot be assigned to different user addresses.
- Only even addresses can be assigned to parameters and monitors of two words (32 bits).

Input terminal

Multi function

In the first section in a multi function counter block detail window, two input terminals ("Input 0", "Input 1") are arranged by default.
They are used to use signals input to a multi function counter block in the hardware logic outline window ("Input 0", "Input 1") as input signals in the multi function counter block detail window.

Output

The following table shows the output of the input terminal.

Variable name	Data type	Linkable block	Valid range	Description
Input	Bit	Input signal event detection*1	0, 1	Outputs the High/Low states of the Input terminal of a multi function counter block in the hardware logic outline window.

*1 The input terminals and the input signal event detection blocks are automatically linked in the following combinations, and the links cannot be deleted.
· "Input 0" terminal (input terminal) and "Input A" terminal (input signal event detection block)
· "Input 1" terminal (input terminal) and "Input B" terminal (input signal event detection block)

Latch input terminal

Multi function

In the first section in a multi function counter block detail window, latch input terminals are arranged by default. For a 16-bit counter , two latch input terminals ("Latch 0", "Latch 1") are arranged. For a 32-bit counter, one latch input terminal ("Latch 0") is arranged.
They are used to use latch signals input to a multi function counter block in the hardware logic outline window ("Latch 0", "Latch 1") as latch signals in the multi function counter block detail window.

Output

The following table shows the output of the latch input terminal.

Variable name	Data type	Linkable block	Valid range	Description
Latch	Bit	Latch event detection*1	0, 1	Outputs the High/Low states of the Latch terminal of a multi function counter block in the hardware logic outline window.

*1 The latch input terminals and the latch event detection blocks are automatically linked in the following combinations, and the links cannot be deleted.
· "Latch 0" terminal (latch input terminal) and "Input A" terminal (latch event detection block)
· "Latch 1" terminal (latch input terminal) and "Input B" terminal (latch event detection block)

Event input terminal

Multi function

In the first section in a multi function counter block detail window, event input terminals are arranged by default. For a 16-bit counter, four event input terminals ("Event 0" to "Event 3") are arranged. For a 32-bit counter, two event input terminals ("Event 0", "Event 1") are arranged.

They are used to use signals input to a multi function counter block in the hardware logic outline window ("Event 0" to "Event 3") as event signals in the multi function counter block detail window.

Output

The following table shows the output of the event input terminal.

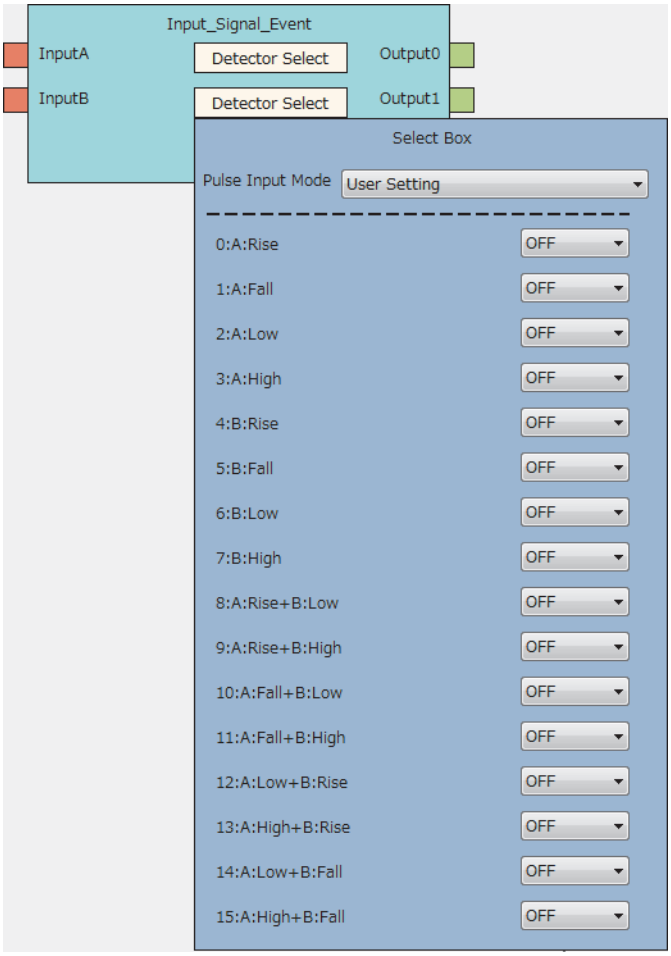
Variable name	Data type	Linkable block	Valid range	Description
Event	Bit	Counter timer*1	0, 1	Outputs the High/Low states of Event terminals of a multi function counter block in the hardware logic outline window.

*1 The event input terminal can link with all the terminals of a counter timer block.

Input signal event detection block

Multi function

In the second section in a multi function counter block detail window, one input signal event detection block ("Input_Signal_Event") is arranged by default.
Set conditions to detect input signals of a multi function counter block. When the detection conditions are satisfied, the Output terminal turns to High. This operation can be utilized for the count-up or other functions of the counter timer block.



Input

The following table shows the inputs of the input signal event detection block.

Variable name	Data type	Linkable block	Valid range	Description
Input A	Bit	Input*1	0, 1	Signals from Input terminals are input. "Input A" is for a phase-A input, and "Input B" is for a phase-B input.
InputB				

*1 The input terminals and the input signal event detection blocks are automatically linked in the following combinations, and the links cannot be deleted.
· "Input 0" terminal (input terminal) and "Input A" terminal (input signal event detection block)
· "Input 1" terminal (input terminal) and "Input B" terminal (input signal event detection block)

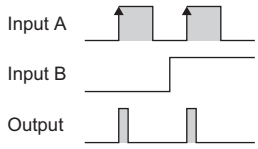
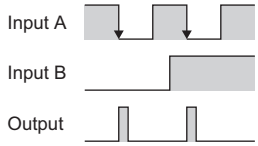
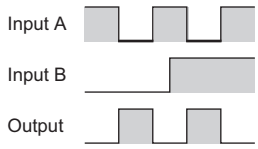
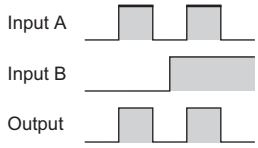
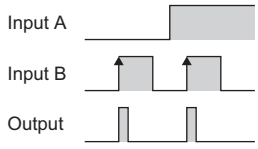
Parameter

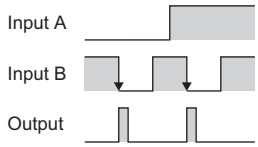
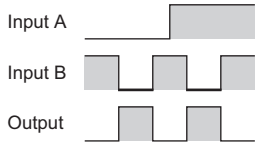
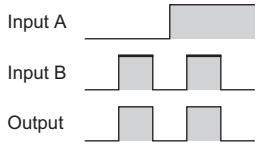
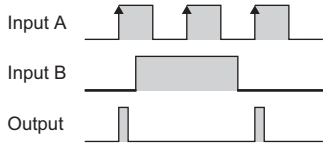
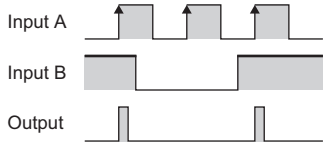
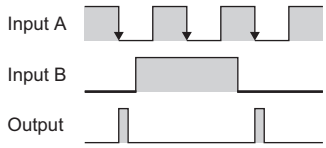
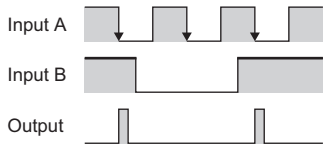
The following tables show the parameters of the input signal event detection block.

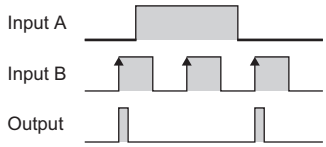
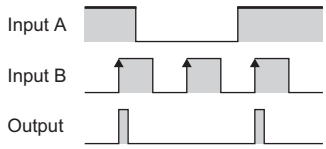
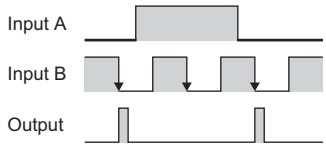
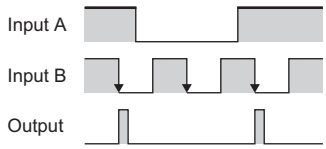
• Parameter of "Detector Select"

Variable name	Data type	Valid range	Default value	Description
Detector Select	Word	—	—	Set the condition to detect signals. Click the [Detector Select] button to open the detection condition setting window ("Select Box").

• Parameters of "Select Box"

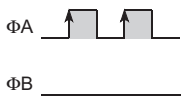
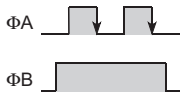
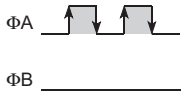
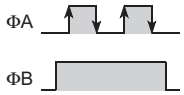
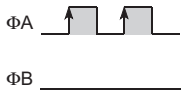
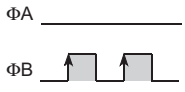
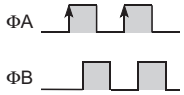
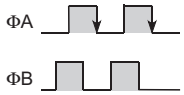
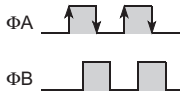
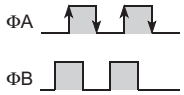
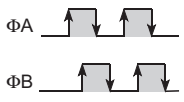
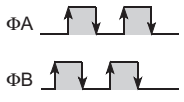
Variable name	Data type	Valid range	Default value	Description
Pulse Input Mode	Word	• User Setting • 1/2-Phase Multiple of 1(CW/CCW)+ • 1-Phase Multiple of 1- • 1-Phase Multiple of 2+ • 1-Phase Multiple of 2- • CW/CCW- • 2-Phase Multiple of 1- • 2-Phase Multiple of 2+ • 2-Phase Multiple of 2- • 2-Phase Multiple of 4+ • 2-Phase Multiple of 4-	User Setting	Set the method to detect input signals. According to the setting of this item, the following 16 settings are changed. If any of the following 16 settings is changed after this item has been set, "User Setting" is set to this item.
A: Rise	Bit	OFF ON	OFF	When the rise of "Input A" has been detected, Output turns to High only for one clock cycle. The status of "Input B" does not affect the status of Output. 
A: Fall	Bit	OFF ON	OFF	When the fall of "Input A" has been detected, Output turns to High only for one clock cycle. The status of "Input B" does not affect the status of Output. 
A: Low	Bit	OFF ON	OFF	While "Input A" is Low, Output is High. The status of "Input B" does not affect the status of Output. 
A: High	Bit	OFF ON	OFF	While "Input A" is High, Output is High. The status of "Input B" does not affect the status of Output. 
B: Rise	Bit	OFF ON	OFF	When the rise of "Input B" has been detected, Output turns to High only for one clock cycle. The status of "Input A" does not affect the status of Output. 

Variable name	Data type	Valid range	Default value	Description
B: Fall	Bit	OFF ON	OFF	When the fall of "Input B" has been detected, Output turns to High only for one clock cycle. The status of "Input A" does not affect the status of Output. 
B: Low	Bit	OFF ON	OFF	While "Input B" is Low, Output is High. The status of "Input A" does not affect the status of Output. 
B: High	Bit	OFF ON	OFF	While "Input B" is High, Output is High. The status of "Input A" does not affect the status of Output. 
A: Rise+B: Low	Bit	OFF ON	OFF	When the rise of "Input A" and the Low state of "Input B" have been detected, Output turns to High only for one clock cycle. 
A: Rise+B: High	Bit	OFF ON	OFF	When the rise of "Input A" and the High state of "Input B" have been detected, Output turns to High only for one clock cycle. 
A: Fall+B: Low	Bit	OFF ON	OFF	When the fall of "Input A" and the Low state of "Input B" have been detected, Output turns to High only for one clock cycle. 
A: Fall+B: High	Bit	OFF ON	OFF	When the fall of "Input A" and the High state of "Input B" have been detected, Output turns to High only for one clock cycle. 

Variable name	Data type	Valid range	Default value	Description
A: Low+B: Rise	Bit	OFF ON	OFF	When the Low state of "Input A" and the rise of "Input B" have been detected, Output turns to High only for one clock cycle. 
A: High+B: Rise	Bit	OFF ON	OFF	When the High state of "Input A" and the rise of "Input B" have been detected, Output turns to High only for one clock cycle. 
A: Low+B: Fall	Bit	OFF ON	OFF	When the Low state of "Input A" and the fall of "Input B" have been detected, Output turns to High only for one clock cycle. 
A: High+B: Fall	Bit	OFF ON	OFF	When the High state of "Input A" and the fall of "Input B" have been detected, Output turns to High only for one clock cycle. 

■Pulse input modes and count timing

The following table shows the relationships between each pulse input mode and count timing.

"Pulse Input Mode"	Count timing		
1-phase multiple of 1 (1-Phase Multiple of 1+, 1-Phase Multiple of 1-)	At up count		The value is counted up at the rise (↑) of ΦA. ΦB is Low.
	At down count		The value is counted down at the fall (↓) of ΦA. ΦB is High.
1-phase multiple of 2 (1-Phase Multiple of 2+, 1-Phase Multiple of 2-)	At up count		The value is counted up at the rise (↑) and fall (↓) of ΦA. ΦB is Low.
	At down count		The value is counted down at the rise (↑) and fall (↓) of ΦA. ΦB is High.
CW/CCW (CW/CCW+, CW/CCW-)	At up count		The value is counted up at the rise (↑) of ΦA. ΦB is Low.
	At down count		ΦA is Low. The value is counted down at the rise (↑) of ΦB.
2-phase multiple of 1 (2-Phase Multiple of 1+, 2-Phase Multiple of 1-)	At up count		When ΦB is Low, the value is counted up at the rise (↑) of ΦA.
	At down count		When ΦB is Low, the value is counted down at the fall (↓) of ΦA.
2-phase multiple of 2 (2-Phase Multiple of 2+, 2-Phase Multiple of 2-)	At up count		When ΦB is Low, the value is counted up at the rise (↑) of ΦA. When ΦB is High, the value is counted up at the fall (↓) of ΦA.
	At down count		When ΦB is High, the value is counted down at the rise (↑) of ΦA. When ΦB is Low, the value is counted down at the fall (↓) of ΦA.
2-phase multiple of 4 (2-Phase Multiple of 4+, 2-Phase Multiple of 4-)	At up count		When ΦB is Low, the value is counted up at the rise (↑) of ΦA. When ΦA is High, the value is counted up at the rise (↑) of ΦB. When ΦB is High, the value is counted up at the fall (↓) of ΦA. When ΦA is Low, the value is counted up at the fall (↓) of ΦB.
	At down count		When ΦA is Low, the value is counted down at the rise (↑) of ΦB. When ΦB is High, the value is counted down at the rise (↑) of ΦA. When ΦA is High, the value is counted down at the fall (↓) of ΦB. When ΦB is Low, the value is counted down at the fall (↓) of ΦA.

■Detection conditions in pulse input modes

The following table shows the detection conditions in each pulse input mode.

Pulse input mode		"Pulse Input Mode"	Detection condition*1															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1-phase multiple of 1	Up count	1-Phase Multiple of 1+	—	—	—	—	—	—	—	—	○	—	—	—	—	—	—	—
	Down count	1-Phase Multiple of 1-	—	—	—	—	—	—	—	—	—	—	—	○	—	—	—	—
1-phase multiple of 2	Up count	1-Phase Multiple of 2+	—	—	—	—	—	—	—	—	○	—	○	—	—	—	—	—
	Down count	1-Phase Multiple of 2-	—	—	—	—	—	—	—	—	—	○	—	○	—	—	—	—
CW/CCW	Up count	CW/CCW+	—	—	—	—	—	—	—	—	○	—	—	—	—	—	—	—
	Down count	CW/CCW-	—	—	—	—	—	—	—	—	—	—	—	—	○	—	—	—
2-phase multiple of 1	Up count	2-Phase Multiple of 1+	—	—	—	—	—	—	—	—	○	—	—	—	—	—	—	—
	Down count	2-Phase Multiple of 1-	—	—	—	—	—	—	—	—	—	—	○	—	—	—	—	—
2-phase multiple of 2	Up count	2-Phase Multiple of 2+	—	—	—	—	—	—	—	—	○	—	—	○	—	—	—	—
	Down count	2-Phase Multiple of 2-	—	—	—	—	—	—	—	—	—	○	○	—	—	—	—	—
2-phase multiple of 4	Up count	2-Phase Multiple of 4+	—	—	—	—	—	—	—	—	○	—	—	○	—	○	○	—
	Down count	2-Phase Multiple of 4-	—	—	—	—	—	—	—	—	—	○	○	—	○	—	—	○

*1 The numbers of Detection condition indicate the following parameters.
1: "A: Rise"
2: "A: Fall"
3: "A: Low"
4: "A: High"
5: "B: Rise"
6: "B: Fall"
7: "B: Low"
8: "B: High"
9: "A: Rise+B: Low"
10: "A: Rise+B: High"
11: "A: Fall+B: Low"
12: "A: Fall+B: High"
13: "A: Low+B: Rise"
14: "A: High+B: Rise"
15: "A: Low+B: Fall"
16: "A: High+B: Fall"

■Links of "Pulse Input Mode"

Link the Output terminal where "Pulse Input Mode" is set "UP count" to the "UP" terminal of a counter timer block. Link the Output□ terminal where "Pulse Input Mode" is set "Down count" to the "DOWN" terminal of a counter timer block. Otherwise, values are not correctly counted.

Output

The following table shows the outputs of the input signal event detection block.

Variable name	Data type	Linkable block	Output value	Description
Output 0	Bit	• Counter timer*1 • Set/reset • Output • Event output*2	0, 1	Outputs signals detected with the detector.
Output 1				

*1 The "RUN", "STOP", "PRESET", "UP", or "DOWN" terminal of counter timer blocks can be linked.

*2 The terminals can be linked when a 16-bit multi function counter block is used, as shown below. They cannot be linked when a 32-bit multi function counter block is used.

· Event output terminals that can be linked with the "Output 0" terminal: "Event 0" terminal, "Event 1" terminal

· Event output terminals that can be linked with the "Output 1" terminal: "Event 2" terminal, "Event 3" terminal

Setting method

Set the input signal event detection block with the following procedure.

1. Click the [Detector Select] button to open "Select Box".
2. Set "Pulse Input Mode" according to the pulse input mode of external devices.
3. Change the settings in "A: Rise" to "A: High+B: Fall" as necessary.

- If any of the settings has been changed, "Pulse Input Mode" is set to "User Setting".
- When the items of "A: Rise" to "A: High+B: Fall" have been set with "Pulse Input Mode" not set and any of the detection conditions of the pulse input mode is satisfied, the corresponding pulse input mode is applied when "Select Box" is opened again.

Restriction

When "User Setting" is set in "Pulse Input Mode", all the items in "A: Rise" to "A: High+B: Fall" are set to "OFF".

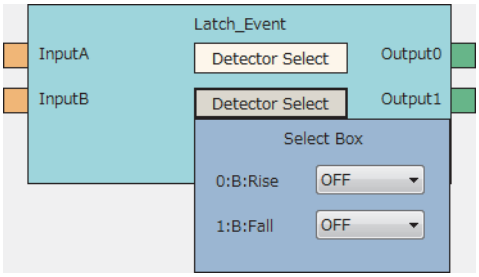
Latch event detection block

Multi function

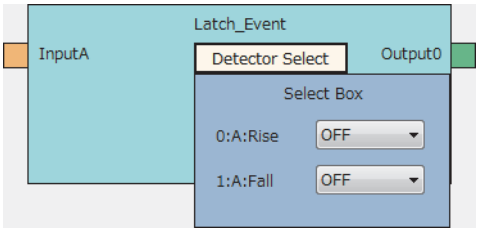
In the second section in a multi function counter block detail window, one latch event detection block ("Latch_Event") is arranged by default.

Set conditions to detect latch input signals of the multi function counter block. When the detection conditions are satisfied, the Output terminal turns to High.

- 16-bit multi function counter block



- 32-bit multi function counter block



Input

The following table shows the inputs of the latch event detection block.

Variable name	Data type	Linkable block	Valid range	Description
Input A	Bit	Latch input*1	0, 1	Signals from Latch terminals are input.
Input B*2				

*1 The latch input terminals and the latch event detection blocks are automatically linked in the following combinations, and the links cannot be deleted.
· "Latch 0" terminal (latch input terminal) and "Input A" terminal (latch event detection block)
· "Latch 1" terminal (latch input terminal) and "Input B" terminal (latch event detection block)

*2 The terminal is not displayed when a 32-bit multi function counter block is used.

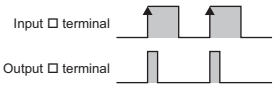
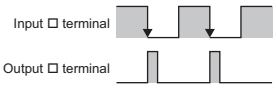
Parameter

The following tables show the parameters of the latch event detection block.

• Parameter of "Detector Select"

Variable name	Data type	Valid range	Default value	Description
Detector Select	Word	—	—	Set the condition to detect signals. Click the [Detector Select] button to open the "Select Box" window. The Detector Select on the upper side is for detecting signals of "Input A". The Detector Select on the lower side is for detecting signals of "Input B".

• Parameters of "Select Box"

Variable name		Data type	Valid range	Default value	Description
A: Rise ("B: Rise" for lower-side Detector Select for a 16-bit multi function counter block)	Rise	Bit	OFF ON	OFF	When the rise of Input has been detected, Output turns to High only for one clock cycle. 
A: Fall ("B: Fall" for lower-side Detector Select for a 16-bit multi function counter block)	Fall	Bit	OFF ON	OFF	When the fall of Input has been detected, Output turns to High only for one clock cycle. 

Output

The following table shows the outputs of the latch event detection block.

Variable name	Data type	Linkable block	Valid range	Description
Output 0	Bit	Counter timer*1	0, 1	Outputs signals detected with the detector.
Output 1*2				

*1 The latch event detection block and the Latch terminals of the counter timer blocks are automatically linked in the following combinations, and the links cannot be deleted.
· "Output 0" terminal (latch event detection block) and "Latch" terminal ("Counter_Timer_0")
· "Output 1" terminal (latch event detection block) and "Latch" terminal ("Counter_Timer_1") (This combination cannot be used for 32-bit multi function counter blocks.)

*2 The terminal is not displayed when a 32-bit multi function counter block is used.

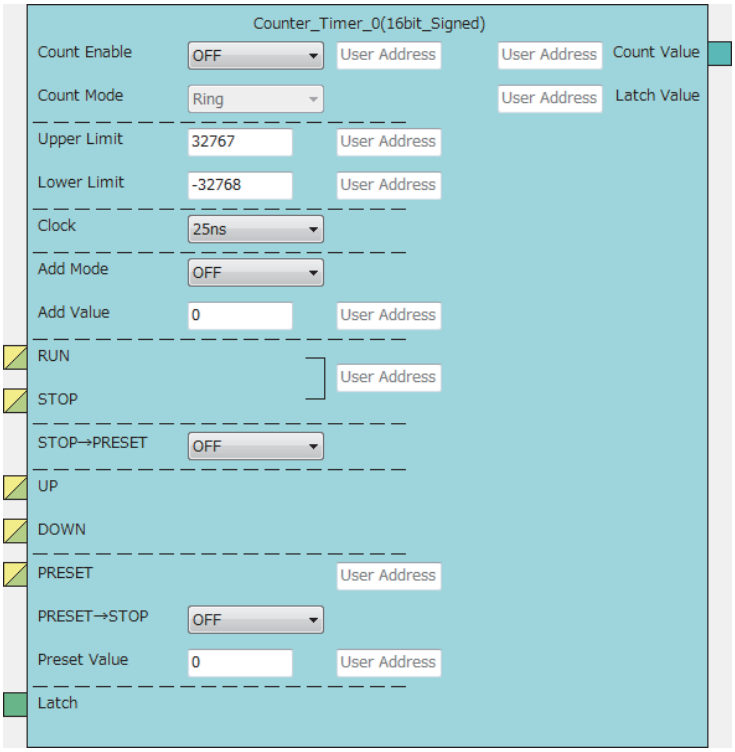
Counter timer block

Multi function

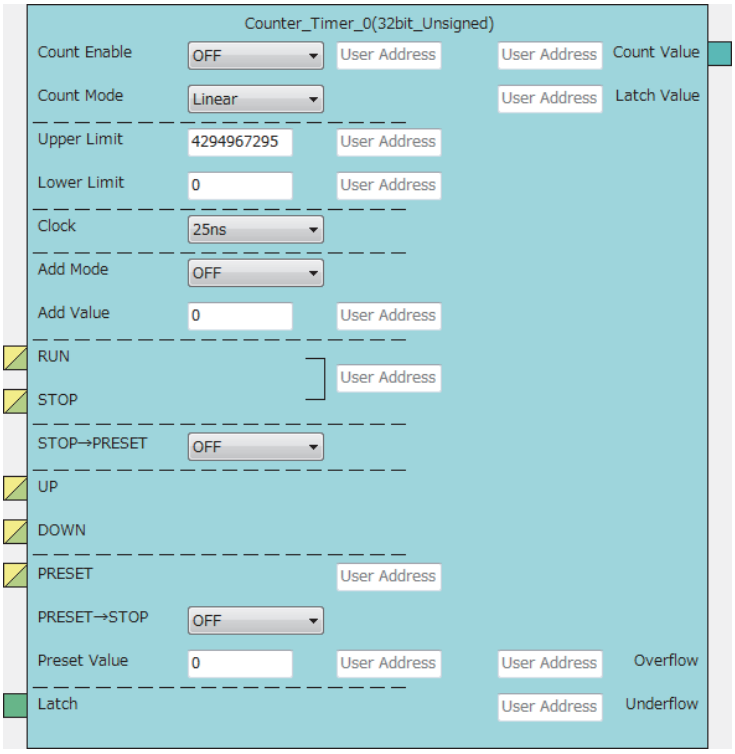
In the third section in a multi function counter block detail window, counter timer blocks are arranged by default. For a 16-bit counter timer block, two counter timer blocks ("Counter_Timer_0"(16bit_Unsigned/Signed), "Counter_Timer_1"(16bit_Unsigned/Signed)) are arranged. For a 32-bit counter timer block, one counter timer block ("Counter_Timer_0"(32bit_Unsigned/Signed)) is arranged.

The counter operates according to the signals of the event input terminals, the input signal event detection block, and the latch event detection block and the count values are output.

- 16-bit multi function counter block



- 32-bit multi function counter block



The counter timer block has the following functions.

- Input pulses are counted.
- Input pulses are counted per clock cycle.
- Either of the ring counter mode or the linear counter mode can be selected (For 16-bit counter timer blocks, only the ring counter mode can be selected).
- Count values can be preset and latched.
- Addition values can be set (addition mode).
- For 32-bit counter timer blocks, an overflow and an underflow can be detected.

Input

The following table shows the inputs of the counter timer block.

Variable name	Data type	Linkable block	Valid range	Description
RUN[*1*6]	Bit	• Event input • Input signal event detection	0, 1	Adds 1 to the count value per preset clock cycle.[*2] Multiple signals can be input to the terminal. OR processing is executed for all input signals.
STOP[*1*6]	Bit	• Event input • Input signal event detection	0, 1	Stops the counter. Multiple signals can be input to the terminal. OR processing is executed for all input signals.
UP[*3*6]	Bit	• Event input • Input signal event detection	0, 1	Adds an addition value to the count value when a signal generated in the previous block is input to the terminal. When the addition mode is off, 1 is added to the count value.[*2] Multiple signals can be input to the terminal. OR processing is executed for all input signals.
DOWN[*3*6]	Bit	• Event input • Input signal event detection	0, 1	Subtracts an addition value from the count value when a signal generated in the previous block is input to the terminal. When the addition mode is off, 1 is subtracted from the count value.[*2] Multiple signals can be input to the terminal. OR processing is executed for all input signals.
PRESET[*1*3]	Bit	• Event input • Input signal event detection	0, 1	Presets the count value. Multiple signals can be input to the terminal. OR processing is executed for all input signals.
Latch[*4]	Bit	• Latch event detection • Event input[*5]	0, 1	Latches the count value to a register.
User Address	Word	—	1000 to 1099	Assign a buffer memory address to change the terminal status with a program during operation. Changing the value of the buffer memory area whose address is assigned changes the set value in the hardware logic.

*1 When a buffer memory address is assigned to "User Address", control can be performed with a program without link. Assign the same buffer memory address to the "RUN" terminal and the "STOP" terminal. (bit 0: RUN, bit 1: STOP)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	STOP	RUN

*2 When the addition mode is on, the addition value is added or subtracted.

*3 Event detection is performed for every clock cycle setting of the counter timer block. Thus, while a High-state signal is input to an event input terminal, an event occurs per clock setting.

*4 The latch event detection block and the Latch terminals of the counter timer blocks are automatically linked in the following combinations, and the links cannot be deleted.
· "Output 0" terminal (latch event detection block) and "Latch" terminal ("Counter_Timer_0")
· "Output 1" terminal (latch event detection block) and "Latch" terminal ("Counter_Timer_1")

*5 On the rising edge (Low state → High state) of the event input terminal, the count value is latched.

*6 Do not link these terminals when an SSI encoder block is linked with a multi function counter block in the hardware logic outline window. Otherwise, correct encoder values may not be acquired.

Point

The High/Low states of the input terminals are detected per clock cycle. When the High states of multiple terminals are detected, only the input of the terminal with the highest priority becomes valid. The inputs of terminals with lower priority become invalid. Link the terminals so that multiple signals are not input at the same time. (Creating a hardware logic where the input to the STOP terminal is detected during the High state is recommended.)

The following shows the priority of the terminals.

1. "PRESET" terminal
2. "STOP" terminal
3. "RUN" terminal
4. "UP" terminal
5. "DOWN" terminal

The RUN terminal holds an event. Thus, when the High states of the PRESET terminal and the RUN terminal for one clock cycle are detected, the PRESET terminal becomes valid. The RUN terminal becomes valid in the next clock cycle.

Parameter

The following table shows the parameters of the counter timer block.

Variable name	Data type	Valid range		Default value	Description
Count Enable	Bit	OFF ON		OFF	Set the count enable to valid or invalid. OFF: Invalid ON: Valid
Count Mode	Bit	Linear Ring		Linear	Set the counter mode to the ring counter or the linear counter. The counter mode is fixed to "Ring" for 16-bit counter timer blocks. Linear: Linear counter Ring: Ring counter
Upper Limit	Word	16-bit signed counter*1	-32768 to 32767	32767	Set the upper limit value of the counter timer.
		16-bit unsigned counter*1	0 to 65535	65535	
		32-bit signed counter*1	-2147483648 to 2147483647	2147483647	
		32-bit unsigned counter*1	0 to 4294967295	4294967295	
Lower Limit	Word	16-bit signed counter*1	-32768 to 32767	-32768	Set the lower limit value of the counter timer.
		16-bit unsigned counter*1	0 to 65535	0	
		32-bit signed counter*1	-2147483648 to 2147483647	-2147483648	
		32-bit unsigned counter*1	0 to 4294967295	0	
Clock	Word	25ns 50ns 0.1µs 1µs 10µs 100µs 1ms		25ns	Set the clock cycle. To count input pulses, set "25ns" for "Clock". Setting a value other than "25ns" may not count the input pulses correctly.
Add Mode	Bit	OFF ON		OFF	Set the addition mode to valid or invalid. OFF: Invalid ON: Valid
Add Value	Word	16-bit signed counter*1	0 to 65535	0	Set the value of addition/subtraction for count.
		16-bit unsigned counter*1			
		32-bit signed counter*1	0 to 4294967295		
		32-bit unsigned counter*1			
STOP → PRESET	Bit	OFF ON		OFF	Set whether to perform the preset function or not at an occurrence of a STOP event. OFF: The preset function is not performed. ON: The preset function is performed.
PRESET → STOP	Bit	OFF ON		OFF	Set whether to stop counting or not at an occurrence of a PRESET event. OFF: Counting is continued. ON: Counting is stopped.
Preset Value	Word	16-bit signed counter*1	-32768 to 32767	0	Set the preset value.
		16-bit unsigned counter*1	0 to 65535		
		32-bit signed counter*1	-2147483648 to 2147483647		
		32-bit unsigned counter*1	0 to 4294967295		

*1 The valid range is determined by the type of the multi function counter block arranged in the hardware logic outline window.

Restriction

The settings of "Clock" of two 16-bit counter timer blocks must be the same. When one "Clock" setting is changed, the other "Clock" setting is changed automatically.

The following table shows "User Address" used for the parameters.

Variable name	Data type	Valid range	Setting range	Description
User Address	Word	—	1000 to 1099	Only even addresses can be assigned to the parameters of two words (32 bits).

Output

The following table shows the output of the counter timer block.

Variable name	Data type	Linkable block	Output value	Description
Count Value	Word	• Comparison*3 • Cam switch*2	• -32768 to 32767 (16-bit signed counter)*1 • 0 to 65535 (16-bit unsigned counter)*1 • -2147483648 to 2147483647 (32-bit signed counter)*1 • 0 to 4294967295 (32-bit unsigned counter)*1	Outputs the value counted by the counter timer.

*1 The valid range is determined by the type of the multi function counter block arranged in the hardware logic outline window.

*2 The cam switch block can be linked only when a 32-bit counter timer block is used. The 32-bit counter timer block and the cam switch block are linked automatically and the link cannot be deleted.

*3 Counter timer blocks and Comparison blocks are linked automatically in the following combinations, and the links cannot be deleted.
· "Count Value" terminal of "Counter_Timer_0" and "Input" terminal of "Compare_0"
· "Count Value" terminal of "Counter_Timer_1" and "Input" terminal of "Compare_1" (This combination cannot be used for 32-bit multi function counter blocks.)

Restriction

The count value is cleared to 0 when the hardware logic control is stopped.
To stop the count operation without clearing the count value, set "Count Enable" to "OFF". To switch the on/off of "Count Enable" during the hardware logic control, assign a buffer memory address to "User Address" of "Count Enable".

Monitor

The following table shows the monitors of the counter timer block.

Variable name	Data type	Description
Count Value	Word	A count value is stored in the buffer memory area specified with "User Address".
Latch Value	Word	A latched count value is stored in the buffer memory area specified with "User Address".
Overflow	Word	When an overflow is detected, 1 is stored in the buffer memory address specified with "User Address".*1
Underflow	Word	When an underflow is detected, 1 is stored in the buffer memory address specified with "User Address".*1

*1 Even when no "User Address" is assigned, an overflow and an underflow are detected and the multi function counter block □ overflow error (error code: 100□H) and the multi function counter block □ underflow error (error code: 101□H) occur. These errors are detected only when the linear counter mode is set for 32-bit counter timer blocks.

The following table shows "User Address" used for the monitors.

Variable name	Data type	Linkable block	Valid range	Description
User Address	Word	—	1000 to 1099	Only even addresses can be assigned to monitors of two words (32 bits).

Counting method

In the flexible high-speed I/O control module, the following counting methods are provided: counting addition pulses and subtraction pulses from external devices and performing up count per clock cycle. The counting method can be set by linking blocks in the hardware logic.

Counting method	Link in hardware logic
Counting the input pulses from external devices	Link the "Output" terminals of the input signal event detection block where the pulse input mode is set according to the external input pulse to the "UP" terminal and "DOWN" terminal of the counter timer block.
Counting based on the clock cycle inside the module	Link terminals to the "RUN" terminal and the "STOP" terminal.

In a counter timer block where the "UP" terminal, "DOWN" terminal, "RUN" terminal, and "STOP" terminal are linked, either of the above counting methods can be used.

■Operation of when input pulses from external devices are counted

When the High state of the "UP" terminal is detected, the addition value is added to the count value. When the High state of the "DOWN" terminal is detected, the addition value is subtracted from the count value. When the High states of the "UP" terminal and the "DOWN" terminal are detected at the same time, the addition value is added to the count value and the detection of the High state of the "DOWN" terminal is ignored.

Point

While input pulses are counted, the count operation can be stopped externally because the "STOP" terminal has higher priority than the "UP" terminal and the "DOWN" terminal.

■Operation of when counting is performed based on the clock cycle inside the module

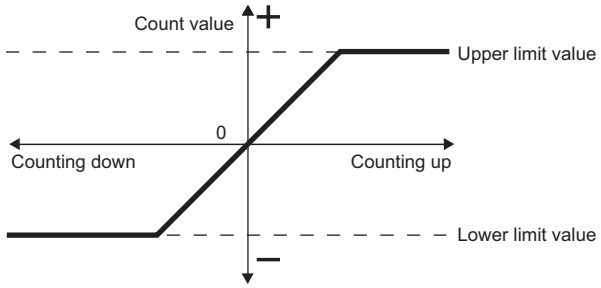
The count operation is performed as a timer. When the High state of the "RUN" terminal is detected, counting up the count value is started. Set the up count cycle with "Clock". When the High state of the "STOP" terminal is detected, counting up the count value is stopped. When the High states of the "RUN" terminal and the "STOP" terminal are detected at the same time, only the High state of the "STOP" terminal becomes valid. The detection of the High state of the "RUN" terminal is ignored.

Linear counter mode

When the linear counter mode is selected, the count operation is performed between the lower limit value and the upper limit value. The following table shows the setting ranges (lower limit value and upper limit value).

Multi function counter block	Setting range
32-bit unsigned	0 to 4294967295
32-bit signed	-2147483648 to 2147483647

The linear counter mode can be set only for a 32-bit counter timer block.

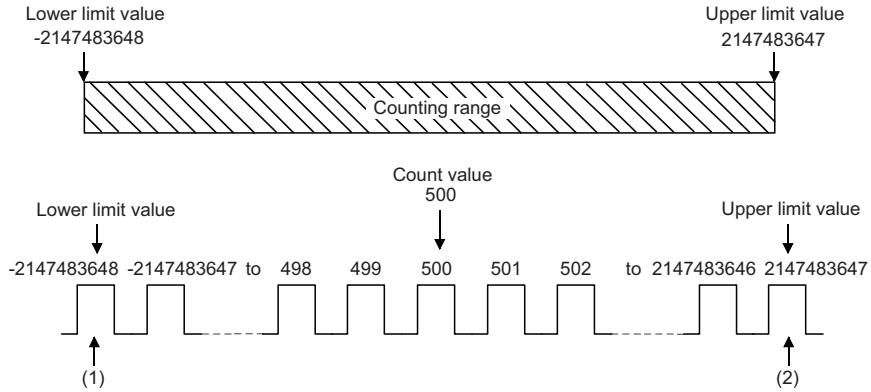


If "Count Value" has reached the upper limit value in up count, "Count Value" does not change in the next up count and the overflow error (error code: 100☐H) occurs. "Count Value" does not change until the preset function is performed even if down count is performed.

If "Count Value" has reached the lower limit value in down count, "Count Value" does not change in the next down count and the underflow error (error code: 101☐H) occurs. "Count Value" does not change until the preset function is performed even if up count is performed.

Ex.

The following figure shows how the counting range and the count value change in a 32-bit signed counter timer block when the preset function is performed with the following settings: the upper limit value is 2147483647, the lower limit value is -2147483648, and "Preset Value" is 500.



(1) If "Count Value" has reached the lower limit value, an underflow occurs when a subtraction pulse is counted.

(2) If "Count Value" has reached the upper limit value, an overflow occurs when an addition pulse is counted.

■Overflow/underflow error

- In a 32-bit counter timer block with the linear counter mode setting, when "Count Value" exceeds the upper limit value in up count, the overflow error (error code: 100□H) is stored in Latest error code (Un\G100). When "Count Value" falls below the lower limit value in down count, the underflow error (error code: 101□H) is stored in Latest error code (Un\G100).
- When the overflow error or underflow error has occurred, the count stops and "Count Value" does not change even if up count or down count is performed.
- These errors can be cleared by performing the preset function. Performing the preset function stores a preset value in "Count Value" and restarts the count. The value stored in Latest error code (Un\G100) is held until the error is reset. Clear the error using Error clear request (YF).

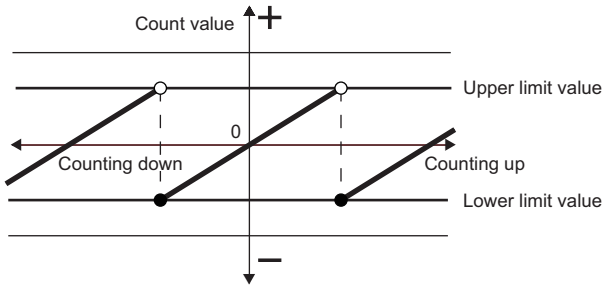
Restriction

In the linear counter mode, set the values as follows.

- Set the upper limit value and the lower limit value so that the lower limit value is smaller than the upper limit value. When the upper limit value is equal to or smaller than the lower limit value, the overflow error or underflow error occurs and the count operation is not performed.
- Set the preset value so that the preset value is larger than or equal to the lower limit value, and smaller than or equal to the upper limit value.

Ring counter mode

When the ring counter mode is selected, the count operation is performed between "Lower Limit" and "Upper Limit" repeatedly. The overflow error and underflow error do not occur.

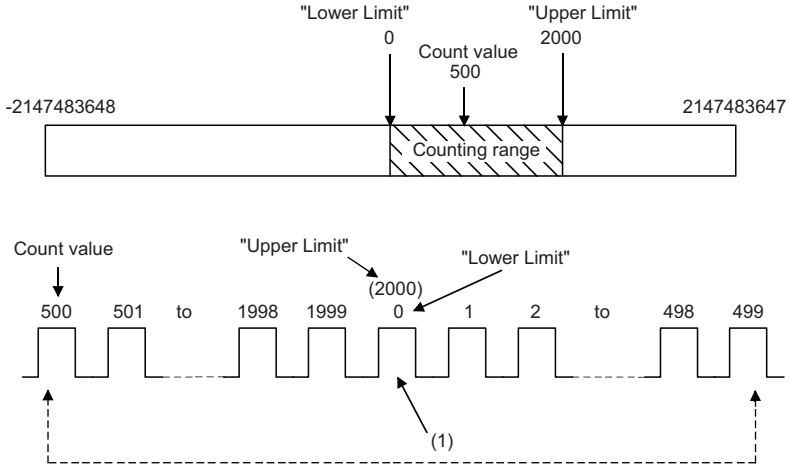


■Lower limit value ≤ Count value < Upper limit value

In up count, when "Count Value" has reached "Upper Limit", the value of "Lower Limit" is stored in "Count Value" automatically. In down count, the count value is held at the value of "Lower Limit" even if "Count Value" has reached "Lower Limit", and the value obtained by subtracting 1 from "Upper Limit" is stored in the count value in the next down count.
In both up count and down count, the value of "Upper Limit" is not stored in "Count Value". However, this excludes the case where "Count Enable" is turned on from off or the values of "Count Value" and "Upper Limit" are the same when the preset function is performed.

Ex.

The following figure shows how the counting range and the count value change when the preset function is performed with the following settings: "Lower Limit" is 0, "Upper Limit" is 2000, and "Preset Value" is 500.



(1) The value 2000 of "Upper Limit" is not stored in "Count Value".

Point

When the same values are set for "Upper Limit" and "Lower Limit", the ring counter operation can be performed with the maximum valid range.
The following show examples for a 32-bit signed counter timer block.

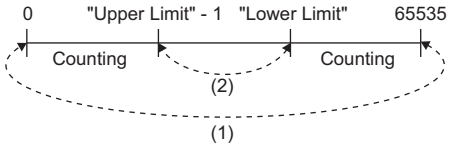
- When up count is performed with the count value 2147483647, the count value becomes -2147483648.
- When down count is performed with the count value -2147483648, the count value becomes 2147483647.

When up count is performed from 2147483646 with "Upper Limit" = 2147483647 and "Lower Limit" = -2147483648, the count value becomes -2147483648. Thus, the count range is one less than that of when the same value is set to the "Upper Limit" and the "Lower Limit".

■Upper limit value ≤ Lower limit value

When "Count Value" has reached the value of "Upper Limit" -1, "Lower Limit" is stored in "Count Value" in the next up count. When "Count Value" has reached the "Lower Limit", the value of "Upper Limit" - 1 is stored in "Count Value" in the next down count. When the same values are set to "Upper Limit" and "Lower Limit", pulses can be counted within the entire range of 32-bit signed/unsigned and the 16-bit signed/unsigned values

The following figure shows a count operation example for a 16-bit unsigned counter block.



(1) When the count value is counted down from 0, the value becomes 65535. When the count value is counted up from 65535, the value becomes 0.

(2) When the count value is counted down from "Lower Limit", the value becomes "Upper Limit" - 1. When the count value is counted up from "Upper Limit" - 1, the value becomes "Lower Limit".

Restriction

In the ring counter mode, set the values as follows.

- Make sure that the count value is within the count range set with the upper limit value and lower limit value. If the count value exceeds the count range, set the preset value within the count range and perform the preset function. If the count operation is continued with the count value out of the count range, the operation cannot be guaranteed.
- Set the preset value within the count range set with the upper limit value and lower limit value.

Addition mode

When "Add Mode" is set to "ON", the following operations are performed.

- For the count in clock cycles, a value set as the addition value is added per clock cycle.
- For counting input pulses, a value set with "Add Value" is added when an addition pulse is input and a value set with "Add Value" is subtracted when a subtraction pulse is input.

■When the addition mode is on in the linear counter mode

When the addition mode is on in the linear counter mode, the count value does not change even if the count operation is performed with the following status.

"Count Value" + "Add Value" > "Upper Limit"

Ex.

When "Add Value" is 5, "Upper Limit" is 1000, and "Count Value" is 998 in a 32-bit signed counter timer block, "Count Value" remains 998 even if up count is performed, and an overflow occurs.

■When the addition mode is on in the ring counter mode

When the addition mode is on in the ring counter mode and up count is performed in the status in which the total of "Count Value" and "Add Value" exceeds "Upper Limit", the count value is as follows.

Count value after addition = "Lower Limit" + ("Add Value" - ("Upper Limit" - Current count value))

Ex.

When "Add Value" is 5, "Upper Limit" is 1000, "Lower Limit" is 0, "Count Value" is 998, and up count is performed, the current count value becomes 3.

Restriction

To turn on the addition mode in the ring counter mode, set a value which satisfies the following condition for "Add Value". When a value which does not satisfy the following condition is set, "Count Value" may exceed "Upper Limit" or fall below "Lower Limit".

- "Add Value" < ("Upper Limit" - "Lower Limit")

■When a buffer memory address is assigned to the addition value

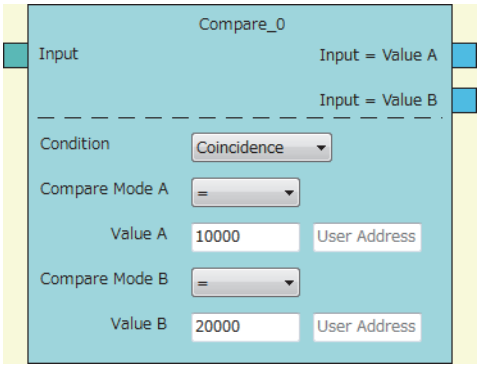
When a buffer memory address is assigned to the addition value and the buffer memory address is changed with a program, handle the buffer memory value in hexadecimal to change the value with a program.

Comparison block

Multi function

In the fourth section in a multi function counter block detail window, comparison blocks are arranged by default. For a 16-bit counter, two comparison blocks ("Compare_0", "Compare_1") are arranged. For a 32-bit counter, one comparison block ("Compare_0") is arranged.

"Count Value" in a counter timer block is compared with the value set with the parameter. If a condition is satisfied, the state of the "Output" terminal turns to High. Two comparison conditions can be set for one counter timer block.



Input

The following table shows the input of the comparison block.

Variable name	Data type	Linkable block	Valid range	Description
Input	Word	Counter timer	• -32768 to 32767 (16-bit signed counter)*1 • 0 to 65535 (16-bit unsigned counter)*1 • -2147483648 to 2147483647 (32-bit signed counter)*1 • 0 to 4294967295 (32-bit unsigned counter)*1	Inputs the count value of the counter timer block.

*1 The valid range is determined by the type of the multi function counter block arranged in the hardware logic outline window.

■Automatic link

Counter timer blocks and comparison blocks are linked automatically in the following combinations, and the links cannot be deleted.

Multi function counter block	Counter timer block	Comparison block
16-bit multi function counter block	"Count Value" terminal of "Counter_Timer_0"	"Input" terminal of "Compare_0"
	"Count Value" terminal of "Counter_Timer_1"	"Input" terminal of "Compare_1"
32-bit multi function counter block	"Count Value" terminal of "Counter_Timer_0"	"Input" terminal of "Compare_0"

Parameter

The following table shows the parameters of the comparison block.

Variable name	Data type	Valid range	Default value	Description
Condition	Word	Coincidence Range	Coincidence	Specify a comparison method. • Coincidence • Range
Compare Mode A Compare Mode B	Word	(Blank) = > < >= <= <>	(Blank)	Select a mode for comparing the count value and the compare value. When "Condition" is set to "Range", this setting is disabled.
Compare Value A Compare Value B	Word	• -32768 to 32767 (16-bit signed counter)*1 • 0 to 65535 (16-bit unsigned counter)*1 • -2147483648 to 2147483647 (32-bit signed counter)*1 • 0 to 4294967295 (32-bit unsigned counter)*1	0	Set the value to be compared with the count value.

*1 The valid range is determined by the type of the multi function counter block arranged in the hardware logic outline window.

The following table shows "User Address" used for the parameters.

Variable name	Data type	Valid range	Setting range	Description
User Address	Word	—	1000 to 1099	Only even addresses can be assigned to the parameters of two words (32 bits).

Ex.

The following table shows examples of comparison with "Count Value" of the counter timer block when "Compare Value" is set to 1000 and "Compare Mode" is set to >.

"Count Value"	Comparison result
900	The comparison fails because "Count Value" is equal to or smaller than "Compare Value". Thus, the "Output" terminal status is turned to Low.
1100	The comparison succeeds because "Count Value" is larger than "Compare Value". Thus, the "Output" terminal status is turned to High.

Output

The following table shows the output of the comparison block.

■When "Condition" is set to "Coincidence"

Variable name	Data type	Linkable block	Output value	Description
Input ☐ Value A *1	Bit	• Set/reset • Event output	0, 1	Outputs the comparison result between "Count Value" and "Compare Value A".
Input ☐ Value B*1	Bit	• Set/reset • Event output	0, 1	Outputs the comparison result between "Count Value" and "Compare Value B".

*1 The setting of "Compare Mode" is reflected to ☐.

Point

A value other than 0 is recommended for the compare value. When the compare value is set to 0, the status of the Output terminal turns to High soon after the hardware logic control starts because the count value soon after the hardware logic control starts is 0.

■When "Condition" is set to "Range"

Variable name	Data type	Linkable block	Output value	Description
Value A <= Input <= Value B	Bit	• Set/reset • Event output	0, 1	Compares "Count Value" with the range using "Compare Value A" and "Compare Value B" and outputs the result. • Within range: High • Out of range: Low
Input < Value A, Value B < Input	Bit	• Set/reset • Event output	0, 1	Compares "Count Value" with the range using "Compare Value A" and "Compare Value B" and outputs the result. • Within range: Low • Out of range: High

Restriction

Set the comparison value so that "Compare Value A" is equal to or smaller than "Compare Value B". When "Compare Value A > Compare Value B" is set, values are output as follows.

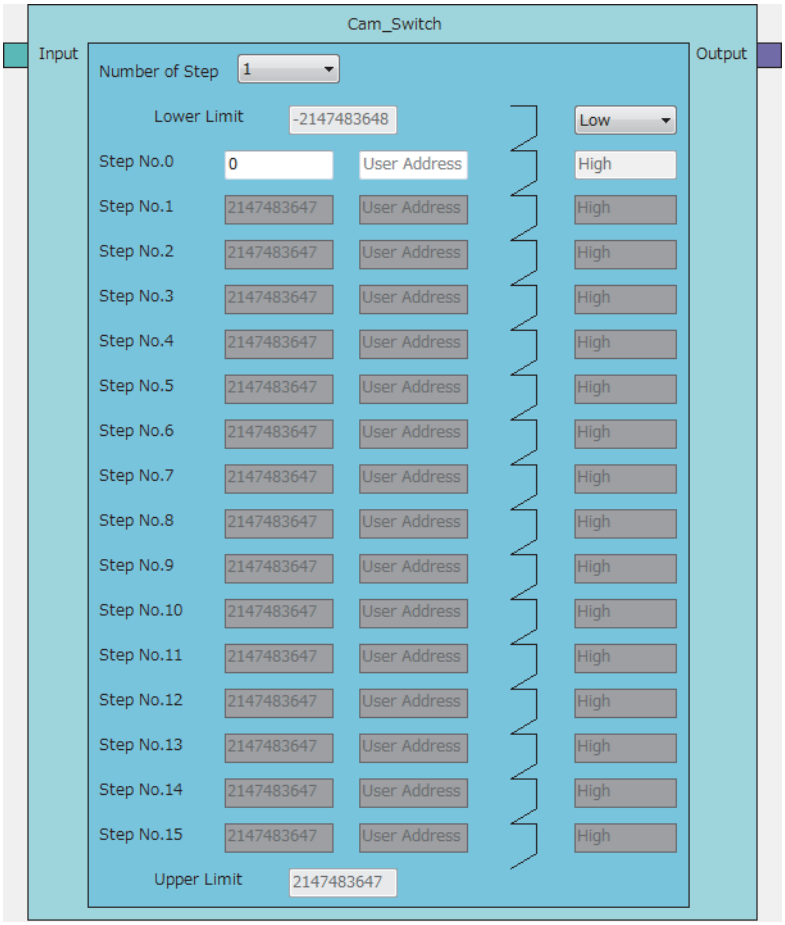
- Output of "Value A <= Input <= Value B" is always Low.
- Output of "Input < Value A, Value B < Input" is always High.

Cam switch block

Multi function

In a multi function counter block detail window, one cam switch block ("Cam_Switch") linked to a counter timer block is arranged across the fourth and fifth sections. However, no cam switch block is arranged in a 16-bit multi function counter block.

The values in the cam switch block are compared with "Count Value" in the counter timer block and the High/Low signals are output.



Input

The following table shows the input of the cam switch block.

Variable name	Data type	Linkable block	Valid range	Description
Input	Word	Counter timer*1	• -2147483648 to 2147483647 (32-bit signed counter)*2 • 0 to 4294967295 (32-bit unsigned counter)*2	Inputs the compare value of the counter timer block. When "User Address" of the step No. is not used, set the refreshing cycle of the count value to 0.1µs or more. When "User Address" is used, set it to 0.2µs or more.*3

*1 "Count Value" in the counter timer block and the cam switch block is linked automatically and the link cannot be deleted.
*2 The valid range is determined by the type of the multi function counter block arranged in the hardware logic outline window.
*3 When "User Address" is used, variability of 100ns or less occurs when the output turns to High or Low.

Parameter

The following table shows the parameters of the cam switch block.

Variable name	Data type	Valid range	Default value	Description
Number of Step	Word	1 to 16	1	Set the number of steps of the cam switch. A step indicates the point in which the Low state is switched to the High state or the High state is switched to the Low state. The valid Step No.☐ is determined according to the set value of "Number of Step".
Lower Limit	Word	—	—	The value set with "Lower Limit" in the counter timer block is applied. Change the setting value in the counter timer block.
Lower Limit Output State	Word	Low High	Low	Set the initial state of output. When "Count Value" of the counter timer block is less than the input value of "Step No.0", the output status turns to the initial state. The output status of "Step No.0" or later inverts to the High state or the Low state for every step No.
Step No.0	Word	• -2147483648 to 2147483647 (32-bit signed counter)*1 • 0 to 4294967295 (32-bit unsigned counter)*1	0	Compares the values of step numbers with "Count Value" in the counter timer block. When "Count Value" is equal to or larger than the input value, the previous status is inverted.
Step No.1			Maximum value in the valid range	
Step No.2				
Step No.3				
Step No.4				
Step No.5				
Step No.6				
Step No.7				
Step No.8				
Step No.9				
Step No.10				
Step No.11				
Step No.12				
Step No.13				
Step No.14				
Step No.15				
Upper Limit	Word	—	—	The value set with "Upper Limit" in the counter timer block is applied. Change the setting value in the counter timer block.

*1 The valid range is determined by the type of the multi function counter block arranged in the hardware logic outline window.

The following table shows "User Address" used for the parameters.

Variable name	Data type	Valid range	Default value	Description
User Address	Word	1000 to 1098	User Address	Only even addresses can be assigned to the parameters of two words (32 bits).

Output

The following table shows the output of the cam switch block.

Variable name	Data type	Linkable block	Output value	Description
Output	Bit	Cam switch output*1	0, 1	Outputs signals created in the cam switch block. Only the "Cam Output" terminal can be linked to the "Output" terminal.

*1 The cam switch block and "Cam Output" terminal are linked automatically and the link cannot be deleted.

Operation examples

The following describes operation examples of the cam switch block.

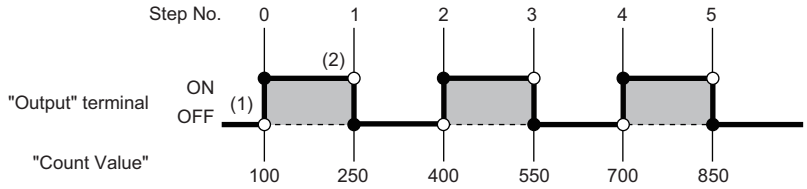
■When the number of steps is set to 6

• Setting details

Item	Setting value
Number of Step	6
Lower Limit*1	-2147483648
Lower Limit Output State	Low
Step No.0	100
Step No.1	250
Step No.2	400
Step No.3	550
Step No.4	700
Step No.5	850
Upper Limit*1	2147483647

*1 Set it in the counter timer block.

• Operation



No.	Description
(1)	For "Lower Limit" ≤ Count value < "Step No.0", the output status set with "Lower Limit Output State" is applied. When the count value is equal to or larger than the set value of "Step No.0", the output status turns to High.
(2)	When the count value is equal to or larger than the set value of "Step No.1", the output status turns to Low. After that, the output status turns to High or Low depending on the magnitude relationship between the count value and "Step No.□".

■When the number of steps is set to 2

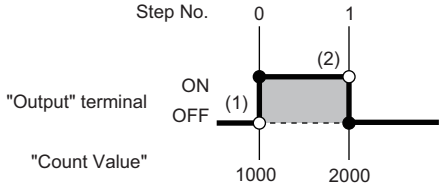
• Setting details

Item	Setting value
Number of Step	2
Lower Limit*1	-2147483648
Lower Limit Output State	Low*2
Step No.0	1000
Step No.1	2000
Upper Limit*1	2147483647

*1 Set it in the counter timer block.

*2 When "Low" is set, operations of output within the range are performed. When "High" is set, operations of output out of the range are executed.

• Operation



No.	Description
(1)	For "Lower Limit" ≤ Count value < "Step No.0", the output status set with "Lower Limit Output State" is applied. When the count value is equal to or larger than the set value of "Step No.0", the output status turns to High.
(2)	When the count value is equal to or larger than the set value of "Step No.1", the output status turns to Low.

Setting method

Set the cam switch block with the following procedure.

1. Set the number of steps of the cam switch for "Number of Step".
2. Set "Step No.0" to "Step No.15" so that the setting values in "Lower Limit", "Step No.0" to "Step No.15", and "Upper Limit" are arranged in ascending order.

Restriction

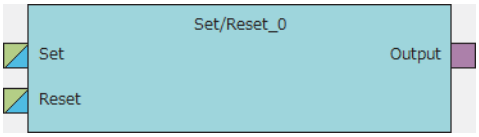
When the setting values in "Lower Limit", "Step No.0" to "Step No.15", and "Upper Limit" are not arranged in ascending order, the control for the cam switch block is not normally performed.

Set/reset block

Multi function

In the fifth section in the multi function counter block detail window, set/reset blocks are arranged by default. For a 16-bit counter, two set/reset blocks ("Set/Reset_0" and "Set/Reset_1") are arranged. For a 32-bit counter, one set/reset block is arranged.

The signal input to the "Set" terminal is used as a trigger to output High fixed signals or the signal input to the "Reset" terminal is used as a trigger to output Low fixed signals.



Input

The following table shows the inputs of the set/reset block.

Variable name	Data type	Linkable block	Valid range	Description
Set	Bit	• Input signal event detection • Comparison	0, 1	Outputs the High fixed signal when an input signal is detected. Even if the input signal turns to Low, output continues until a signal is input to "Reset".
Reset	Bit	• Input signal event detection • Comparison	0, 1	Outputs the Low fixed signal when an input signal is detected.

Restriction

- When both the "Set" terminal status and "Reset" terminal status turn to High at the same time, the "Reset" terminal becomes valid.

■Link of the set/reset block

- The set/reset block in a 16-bit counter can be linked to the following comparison blocks.

Set/reset block	Comparison block
"Set/Reset_0"	"Compare_0"
"Set/Reset_1"	"Compare_1"

Output

The following table shows the output of the set/reset block.

Variable name	Data type	Linkable block	Output value	Description
Output	Bit	Output	0, 1	Outputs High fixed or Low fixed signals.

Output terminal

Multi function

In the sixth section in the multi function counter block detail window, one output terminal ("Output 0") is arranged by default. When terminals have been linked to the output terminal, the signals input to the output terminal can be output from the "Output" terminal in the multi function counter block arranged in the hardware logic outline window.

Output

The following table shows the output of the output terminal.

Variable name	Data type	Linkable block	Valid range	Description
Output	Bit	• Input signal event detection • Set/reset	0, 1	Outputs the High/Low states of the "Output 0" terminal of a multi function counter block in the hardware logic outline window. This terminal is used for link in the multi function counter block detail window. Multiple signals can be input to the terminal. OR processing is executed for all input signals.

Event output terminal

Multi function

In the sixth section in a multi function counter block detail window, event output terminals are arranged by default. For a 16-bit counter timer block, four event output terminals ("Event 0" to "Event 3") are arranged. For a 32-bit counter timer block, two event output terminals ("Event 0", "Event 1") are arranged.

Event output terminals output the input signals from "Event☐" terminals in the multi function counter block.

- 16-bit multi function counter block

- 32-bit multi function counter block

Output

The following table shows the output of the event output terminal.

Variable name	Data type	Linkable block	Valid range	Description
Event	Bit	• Input signal event detection • Comparison	0, 1	Outputs the High/Low states of Event ☐ terminals of a multi function counter block in the hardware logic outline window. This terminal is used for link in the multi function counter block detail window. Multiple signals can be input to the terminal. OR processing is executed for all input signals.

■Link of event output terminals

- The event output terminals in a 16-bit counter can be linked to the following comparison blocks.

Event output terminal	Comparison block
• "Event 0" • "Event 1"	"Compare_0"
• "Event 2" • "Event 3"	"Compare_1"

- For event output terminals in a 16-bit counter, linkable "Output" terminals of the input signal event detection block are different as shown below. Event output terminals are not linkable in a 32-bit counter.

Event output terminal	Input signal event detection block
• "Event 0" • "Event 1"	"Output 0"
• "Event 2" • "Event 3"	"Output 1"

Cam switch output terminal

Multi function

In the sixth section in a 32-bit multi function counter block detail window, one cam switch output terminal ("Cam Output") is arranged by default. No cam switch output terminal is arranged in a 16-bit multi function counter block.
The arranged cam switch output terminal is linked with the cam switch block.
The signals input to the cam switch output terminal can be output from the "Cam Output" terminal in the multi function counter block arranged in the hardware logic outline window.

Output

The following table shows the output of the cam switch output terminal.

Variable name	Data type	Linkable block	Valid range	Description
Cam Output	Bit	Cam switch*1	0, 1	Outputs the High/Low states of the "Cam Output" terminal of a multi function counter block in the hardware logic outline window.

*1 The cam switch block and the cam switch output terminal are linked automatically and the link cannot be deleted.

9.3 Intelligent Function Module Interrupt

This function outputs an interrupt request to the CPU module and starts an interrupt program when a signal is input to an SI device terminal.

Operation

When an input signal event is detected or a comparison condition is satisfied, a signal is input from the "Output" terminal of a multi function counter block to an SI device terminal. The interrupt program corresponding to the SI device terminal to which the signal has been input is executed.

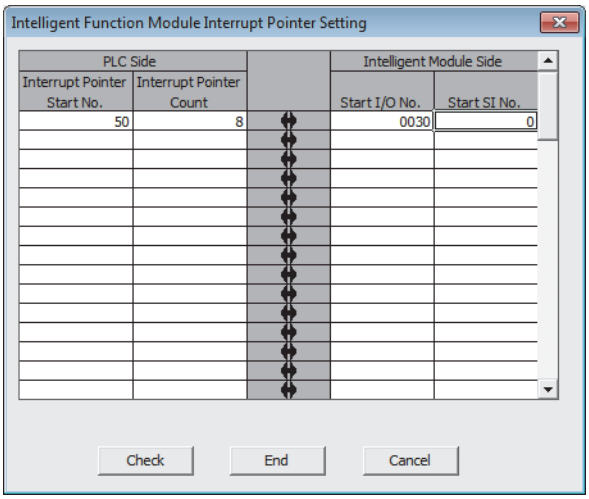
Setting method

To use the intelligent function module interrupt, intelligent function module interrupt pointers and a hardware logic are required to be set in advance.

■Setting intelligent function module interrupt pointers

Set interrupt factors (SI) and interrupt pointers of the CPU module in the intelligent function module interrupt pointer setting.

Project window ⇨ [PLC Parameter] ⇨ [PLC System] ⇨ [Interrupt Pointer Setting]



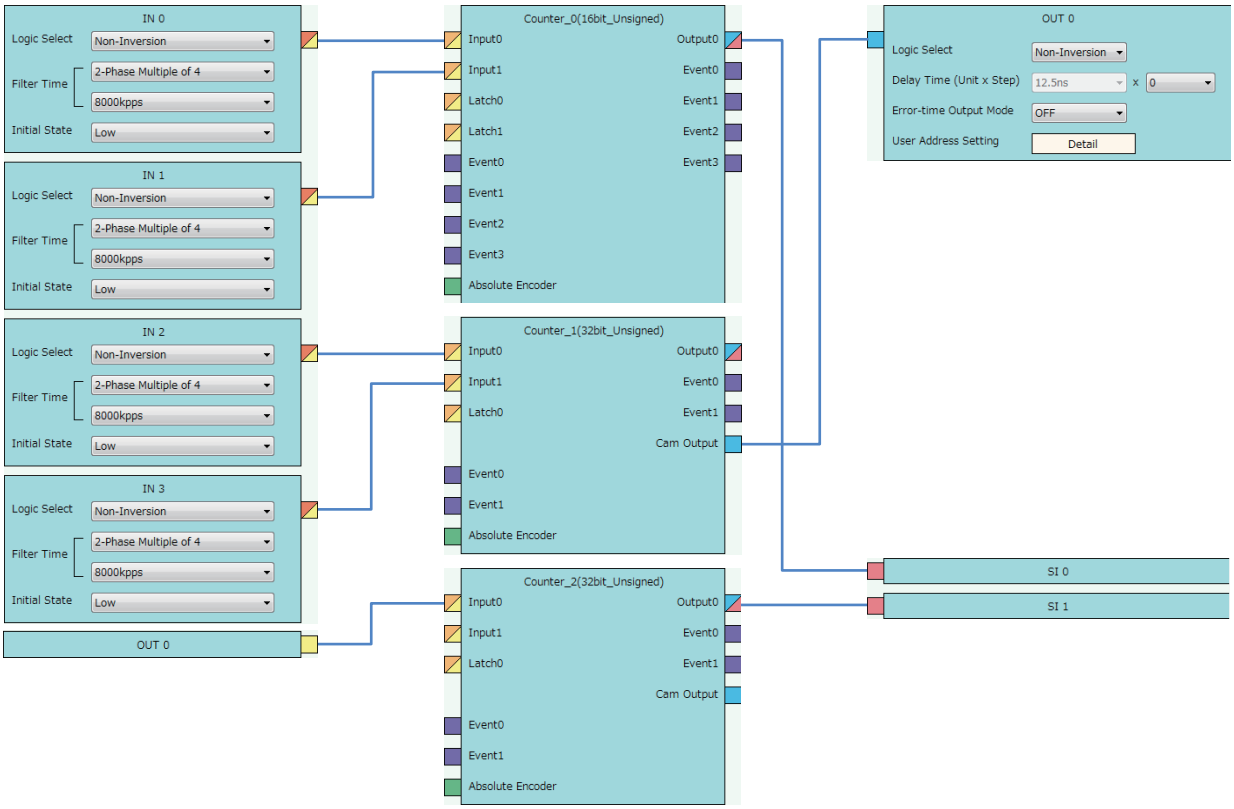
Item	Setting range
Interrupt Pointer Start No.	50 to 248
Interrupt Pointer Count	8 (fixed)*1
Start I/O No.	0000 to 0FE0
Start SI No.	0 (fixed)*1

*1 Always set the described value.

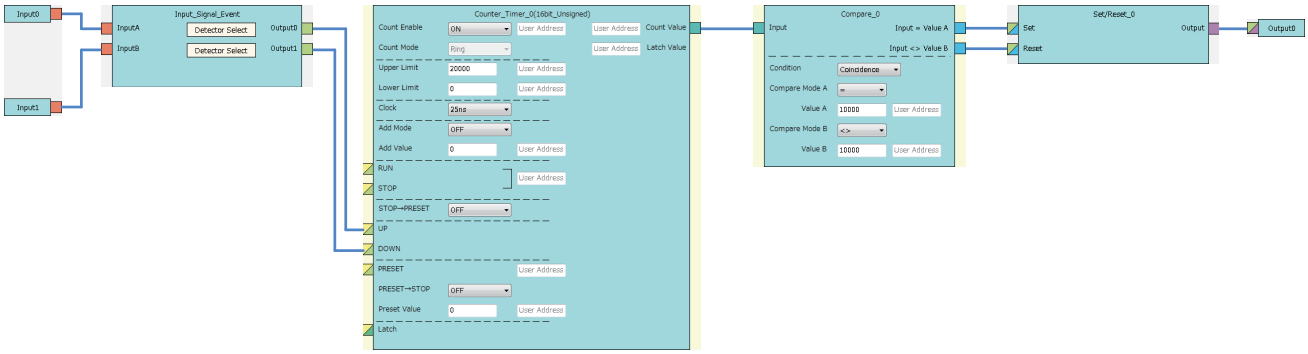
■Setting the hardware logic

The following figure shows link examples of the hardware logic.

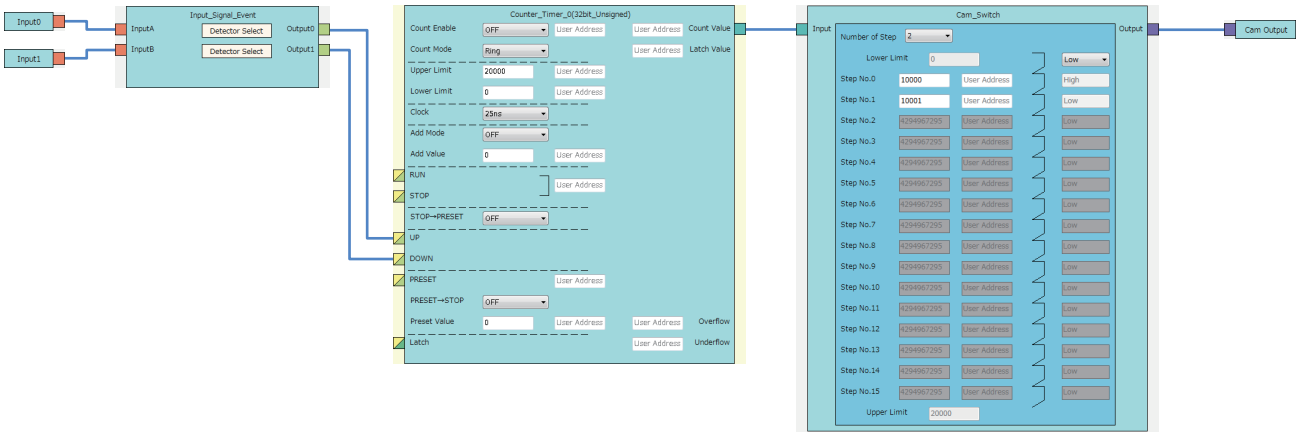
- Hardware logic outline window



- Multi function counter block detail window (Counter_0(16bit_Unsigned))



• Multi function counter block detail window (Counter_1(32bit_Unsigned))

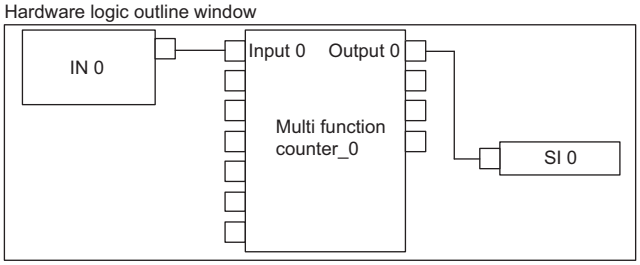


• Multi function counter block detail window (Counter_2(32bit_Unsigned))

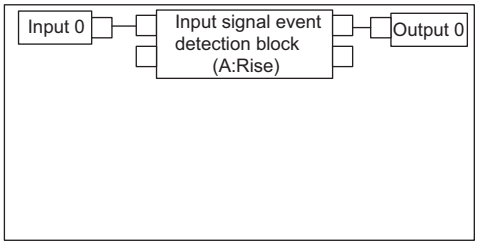
Point

- An SI device terminal linked in the hardware logic must be assigned to an interrupt pointer of the CPU module. If an unassigned SI device terminal turns to High, an error occurs in the CPU module.
- An interrupt request to the CPU module can also be output using a detection in the input signal event detection block as a trigger. The following figure shows a link example in the hardware logic outline window and the multi function counter block detail window.

Hardware logic outline window



Multi function counter block detail window



- For the linking of the multi function counter block detail window (Counter_0(16bit_Unsigned)), a value other than 0 is recommended for "Compare Value". If 0 is set in "Compare Value", an interrupt request is output to the CPU module when the operation of the hardware logic starts (when the count value starts to be counted from 0).

Restriction

An interrupt request to the CPU module is output every 50µs.
If the same interrupt factor (SI) occurs several times within 50µs, the second and later factors (SI) are ignored.

10 BLOCK LINK EXAMPLES

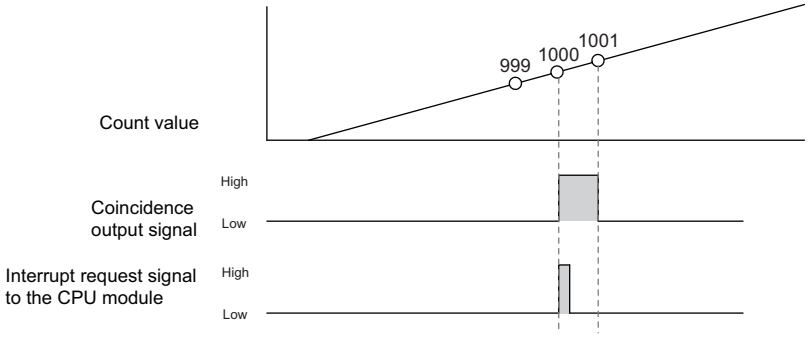
Various controls can be performed with the combinations of various blocks. This chapter shows link examples to perform the following controls.

Control name	Description	Reference
Coincidence detection	Turns on the output of the multi function counter block at coincidence detection.	☞ Page 173 Coincidence Detection
One-shot timer	Turns on the output of the multi function counter block for the specified time period. After the specified time period, the output is turned off until the next event detection.	☞ Page 178 One-shot Timer
Event generation	Outputs an external input signal as an event signal. The output signal can be linked as an event signal of other multi function counter blocks.	☞ Page 182 Event Generation
Cam switch	Turns on or off the output when a count value within the upper and lower limit value range becomes equal to or larger than the setting value of the corresponding steps.	☞ Page 184 Cam Switch
PWM output	Outputs a PWM wave with the specified cycle and duty ratio.	☞ Page 187 PWM Output
Fixed cycle output	Outputs one pulse at every specified cycle.	☞ Page 190 Fixed Cycle Output
Latch counter	Latches (holds) a count value.	☞ Page 193 Latch Counter
Ratio conversion	Outputs an input signal multiplied with the set ratio (x/y).	☞ Page 196 Ratio Conversion
Pulse measurement	Measures the ON width and OFF width of an input pulse.	☞ Page 201 Pulse Measurement

10.1 Coincidence Detection

The output of the multi function counter block is turned on when a count value matches with a compare value. The compare value is required to be set in advance as a coincidence detection value.

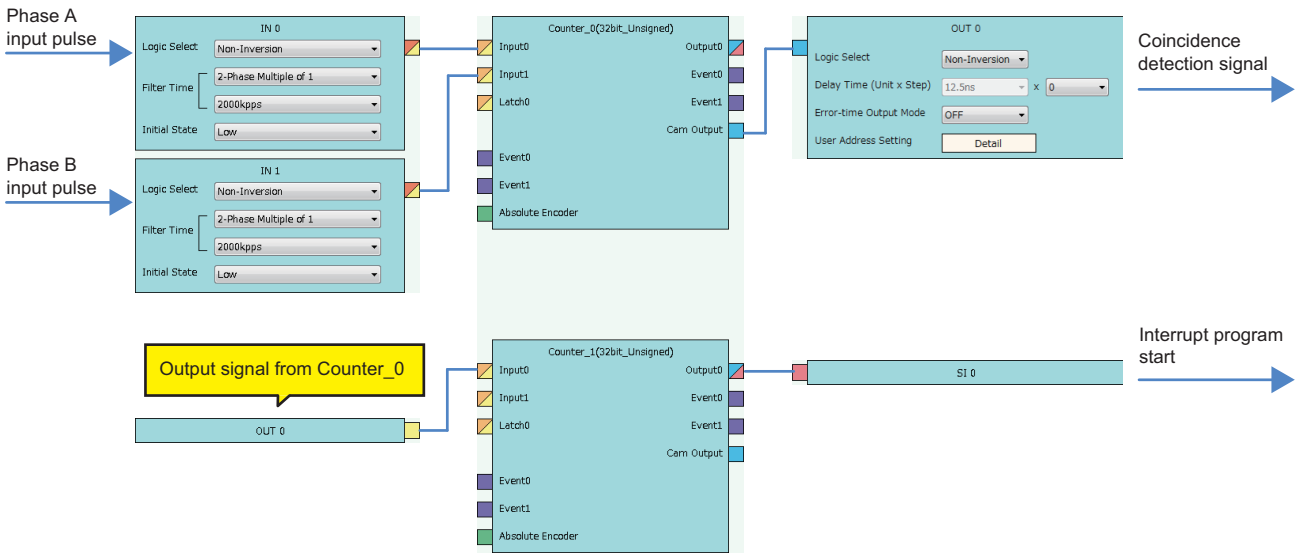
The following describes a link and parameter example of coincidence detection. With the example setting, an external output signal turns on when the count value becomes 1000 and an interrupt request is sent to the CPU module. Note that this link example is for when a 32-bit unsigned multi function counter block is used.



Link and parameter

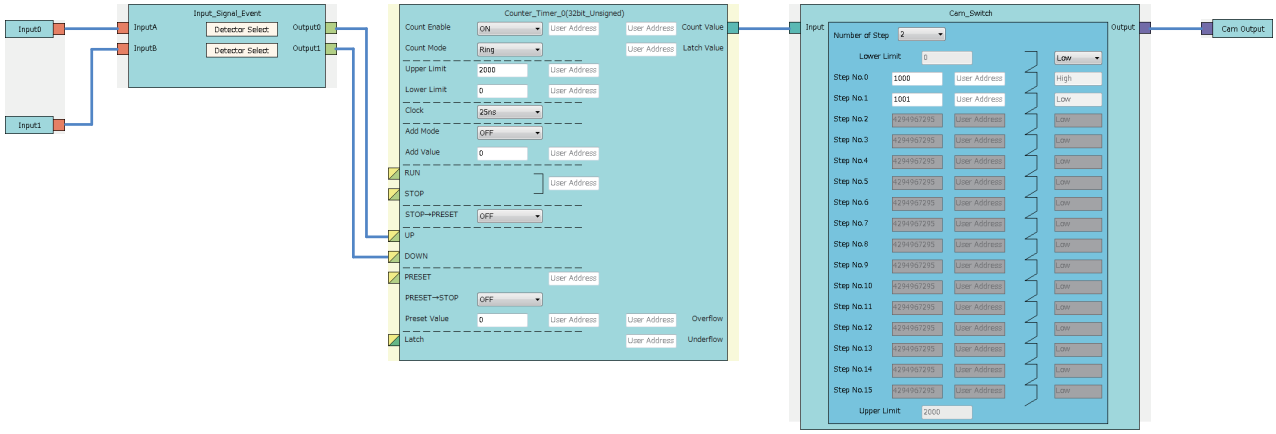
The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window

- Counter_0 (32bit_Unsigned)



Block	Variable name	Setting value	Description
Input 0	—	—	—
Input 1	—	—	—
Input_Signal_Event	Detector Select	2-Phase Multiple of 1+	Set this parameter to detect an addition pulse.
	Detector Select	2-Phase Multiple of 1-	Set this parameter to detect a subtraction pulse.
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Ring	Set this parameter according to the control.
	Upper Limit	2000	Set this parameter according to the control.
	Lower Limit	0	Set this parameter according to the control.
	Clock	25ns	Set this parameter to "25ns". (to prevent input pulses from missing)
	Add Mode	OFF	Set this parameter to "OFF", because the addition mode is not used in this link example.
	Add Value	0	
Cam_Switch	Number of Step	2	Set this parameter to "2".
	Lower Limit Output State	Low	Set this parameter to "Low".
	Step No.0	1000	Set a value used as a "coincidence detection value".
	Step No.1	1001	Set a value of "Step No.0 + 1".
Set/Reset_0	—	—	—
Cam Output	—	—	—

The items other than the above need not to be set.

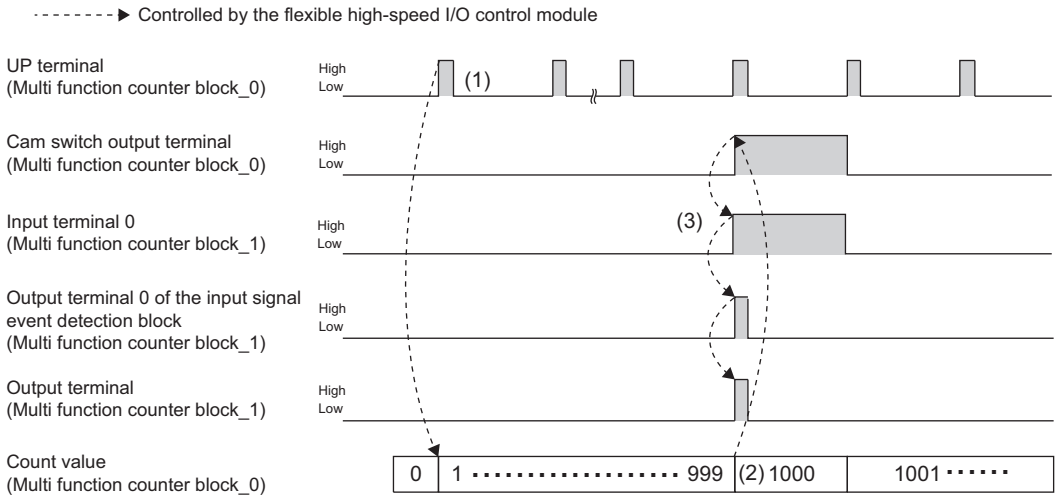
• Counter_1 (32bit_Unsigned)

Block	Variable name	Setting value	Description
Input 0	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: Rise)	Set "Only A: Rise is on".
	Detector Select	—	This parameter is not used in this link example.
Output	—	—	—

The items other than the above need not to be set.

Operation

The following shows operation of coincidence detection when the count value becomes 1000.

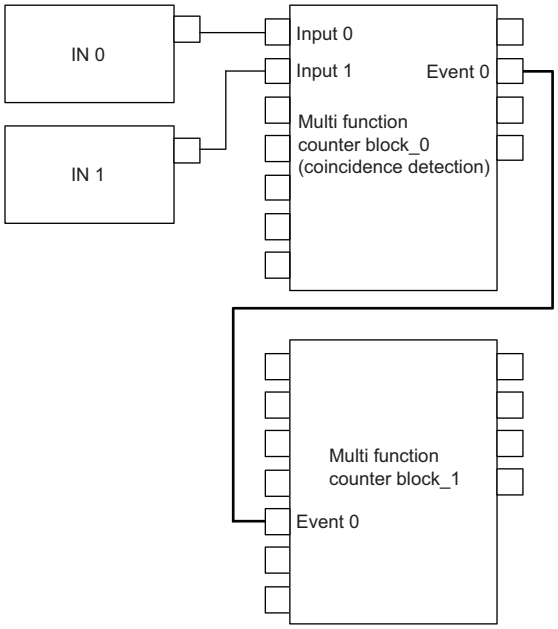


No.	Description
(1)	The count value is increased by one every time the UP terminal of the Counter_0 block turns to High.
(2)	When the count value becomes 1000 (Coincidence detection value), the cam switch output terminal turns to High.
(3)	Through the OUT 0 block in the hardware logic outline window, Input 0 of the multi function counter block_1 turns to High. The input signal event detection block detects the rise of the signal from Input 0, Output 0 turns to High and to Low, and an interrupt request is sent to the CPU module.

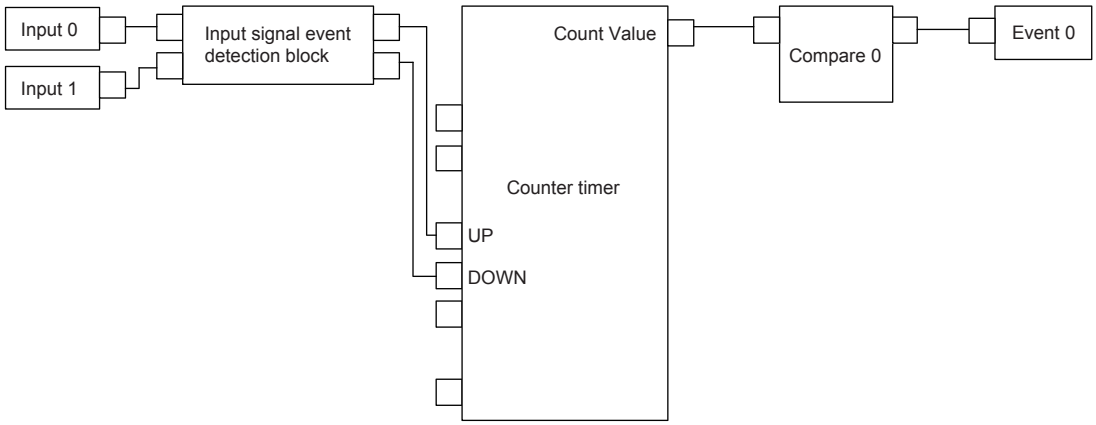
Point

The multi function counter block with a link for coincidence detection can be used as a trigger of other multi function counter blocks. The following shows link examples of the hardware logic outline window and multi function counter block _0 detail window.

• Hardware logic outline window



• Multi function counter block _0 detail window (coincidence detection)



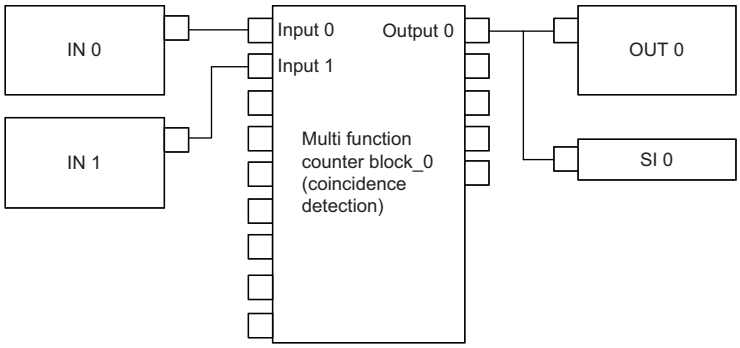
The multi function counter block_0 counts external input signals. When the count value becomes equal to the compare value, an event signal is output to the multi function counter block_1.

Precautions for using 16-bit multi function counter blocks

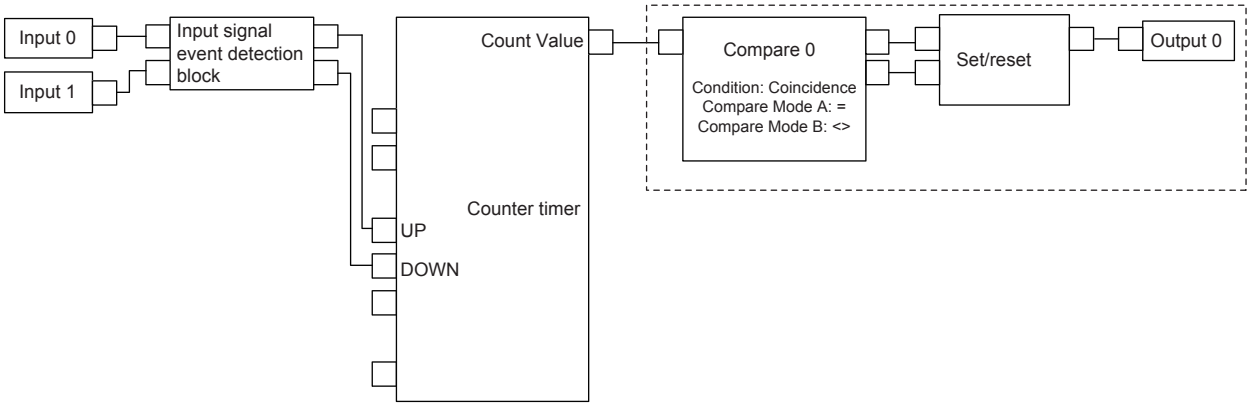
Coincidence detection control can be set even with 16-bit multi function counter blocks. However, usable blocks are different.

The following shows link examples of the hardware logic outline window and multi function counter block detail window.

- Hardware logic outline window



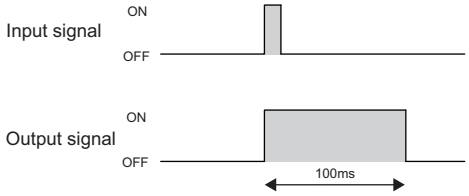
- Multi function counter block _0 detail window (coincidence detection)



Create the hardware logic by using compare blocks and a set/reset block, as shown in the dotted line frame.

10.2 One-shot Timer

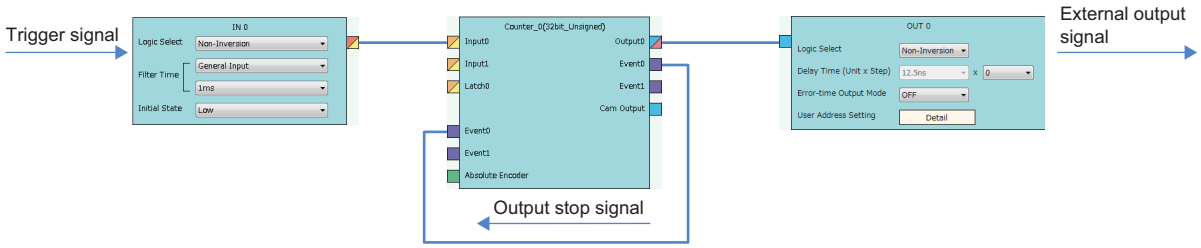
The output signal is turned on for the specified time period using an input signal as a trigger.
The following describes a link and parameter example of a one-shot timer. With the example setting, an output is turned on for 100ms using an external input signal as a trigger. Note that this link example is for when a 32-bit unsigned multi function counter block is used.



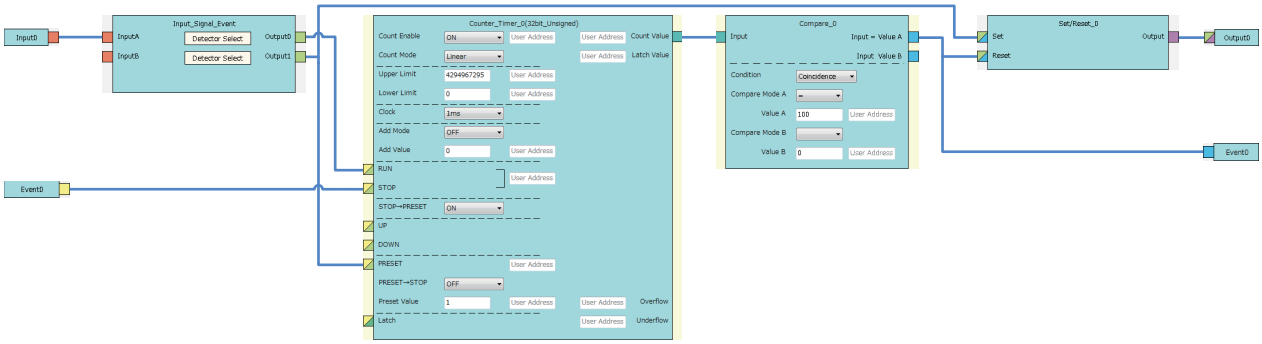
Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window



Block	Variable name	Setting value	Description
Input 0	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: High)	Set this parameter to detect the phase A input signal.
	Detector Select	User Setting (ON only in A: Rise)	
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Linear	Set this parameter according to the control.
	Upper Limit	4294967295	Set this parameter according to the control.
	Lower Limit	0	Set this parameter according to the control.
	Clock	1ms	Set this parameter according to the control.*1
	Add Mode	OFF	Set this parameter according to the control.*2
	Add Value	0	
	STOP → PRESET	ON	Set this parameter to "ON", to perform a preset when a stop event occurs.
	PRESET → STOP	OFF	Set this parameter to "OFF".
	Preset Value	1	Set this parameter according to the control.*1
Compare_0	Condition	Coincidence	Set this parameter to "Coincidence".
	Compare Mode A	=	Set this parameter to "=".
	Compare Value A	100	Set this parameter according to the control.*1
Set/Reset_0	—	—	—
Output	—	—	—

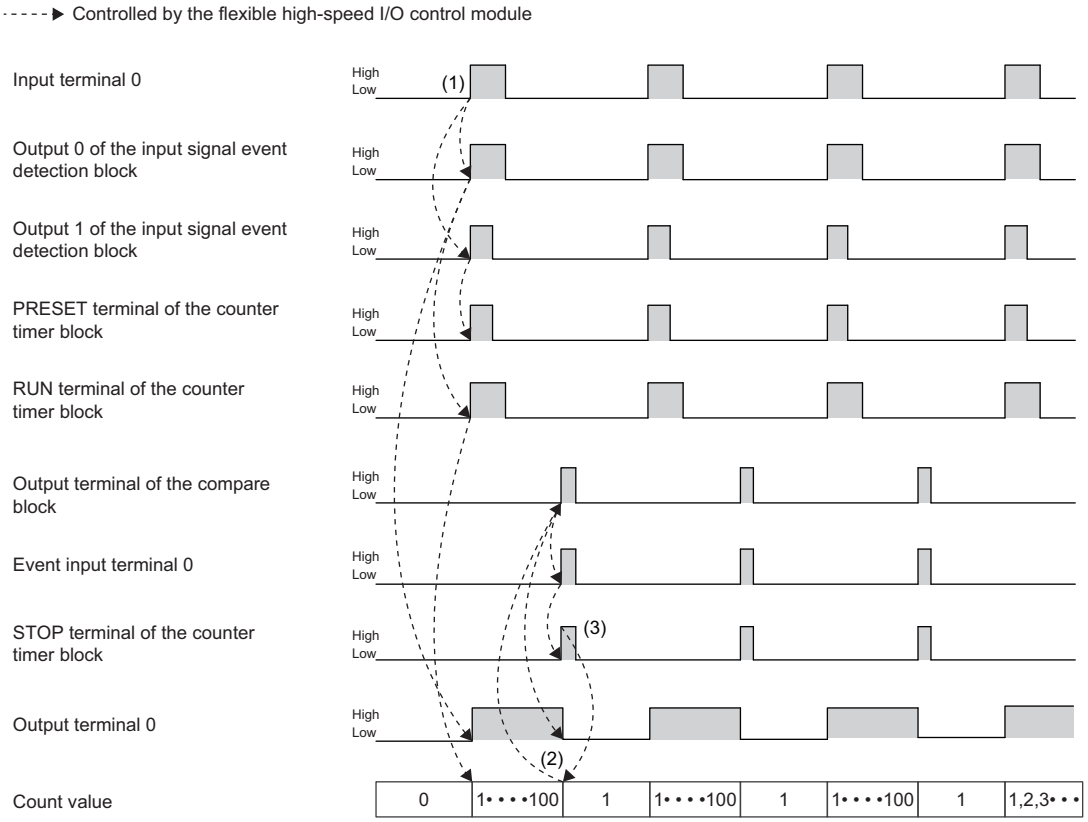
*1 Output ON time = Clock cycle setting × (Compare value - Preset value + 1)

*2 In the addition mode, the output ON time calculated from the following is applied.
Output ON time = (Clock cycle setting × (Compare value - Preset value + 1) ÷ Addition value

The items other than the above need not to be set.

Operation

The following shows operation of the one-shot timer when a trigger signal is input.

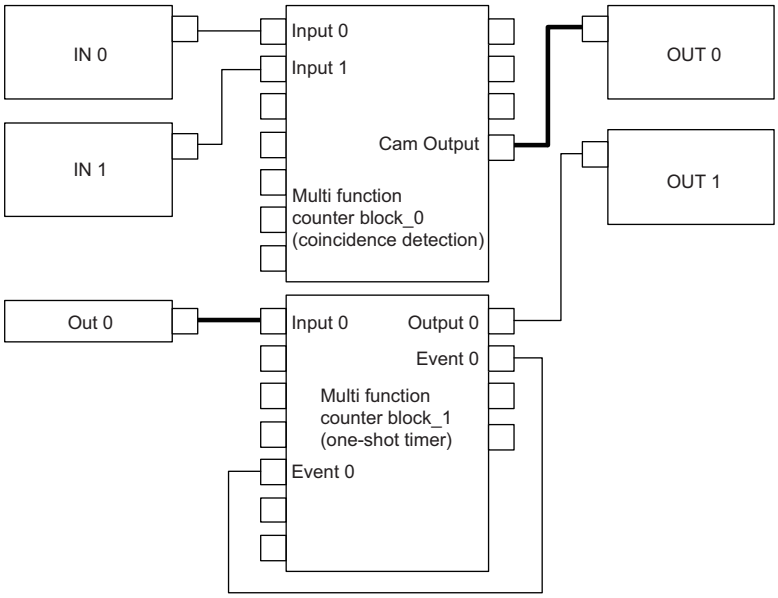


No.	Description
(1)	When a signal is input to the input terminal 0, the signal is output from the output terminal 1 of the input signal event detection block. The output signal turns the PRESET terminal of the counter timer block to High and to Low, performing the preset. (Count value: 0) The signal output from the output terminal 0 of the input signal event detection block turns the RUN terminal of the counter timer block to High, starting counting per clock cycle. In addition, outputs from the output terminal 0 start. (The RUN terminal has a lower priority than the PRESET terminal. Thus, counting per clock cycle starts after the preset.)
(2)	When the count value becomes 100, the Output terminal of the compare block turns to High. The event output terminal 0, event input terminal 0, and the STOP terminal of the counter timer block turn to High in the described order. In addition, outputs from the output terminal 0 stop.
(3)	When the STOP terminal of the counter timer block turns to High, counting per clock cycle stops.

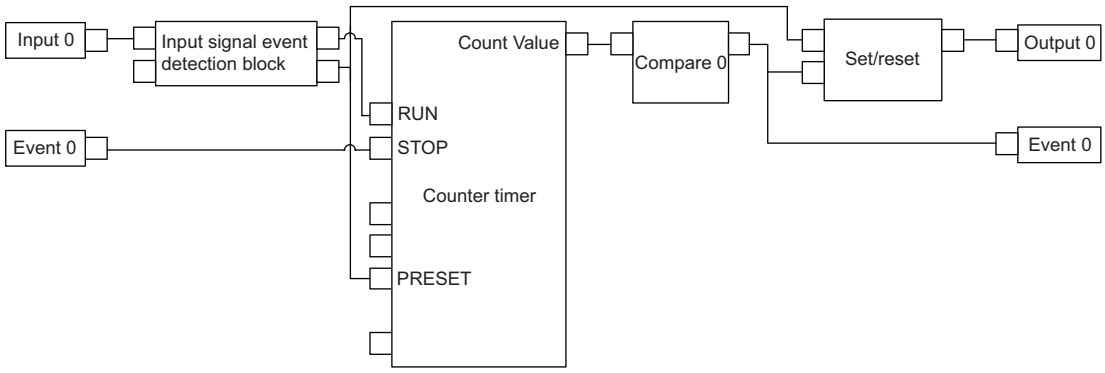
Point

If the multi function counter block with a link for one-shot timer is used together with other blocks with links for coincidence detection or other functions, any output ON time for external devices can be set. The following shows link examples of the hardware logic outline window and multi function counter block_1 detail window.

• Hardware logic outline window



• Multi function counter block_1 detail window (one-shot timer)



10.3 Event Generation

An external input signal is output as an event signal.
Only two event signals can be generated with one multi function counter block. If several multi function counter blocks are used together, three or more event signals can be used with one multi function counter block.
The following describes a link and parameter example of event generation. With the example setting, an event is generated under the following condition and input to the Event terminal of another multi function counter block as an event signal.

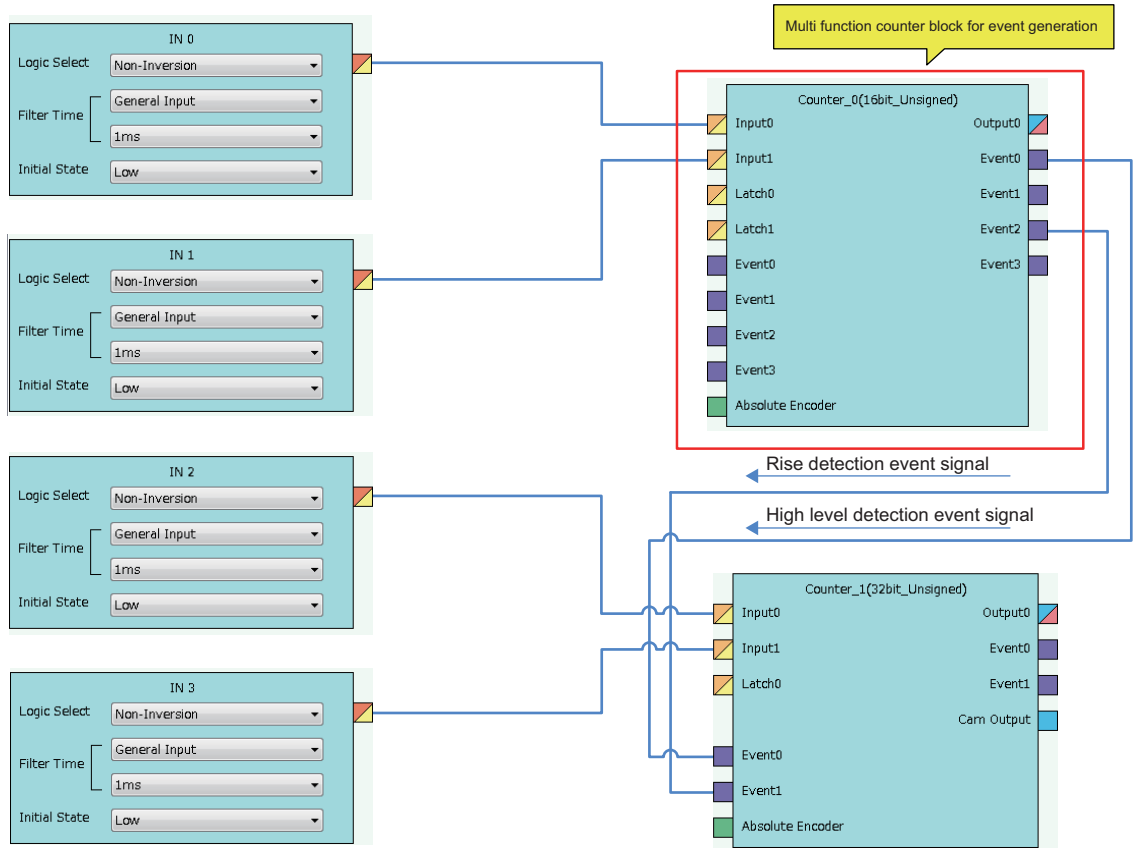
- A signal output from the Event 0 terminal of the multi function counter block _0: Rise of the phase A input
- A signal output from the Event 2 terminal of the multi function counter block _0: High of the phase B input

Note that this link example is for when a 16-bit unsigned multi function counter block is used. Event generation is supported only by 16-bit multi function counter blocks.

Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



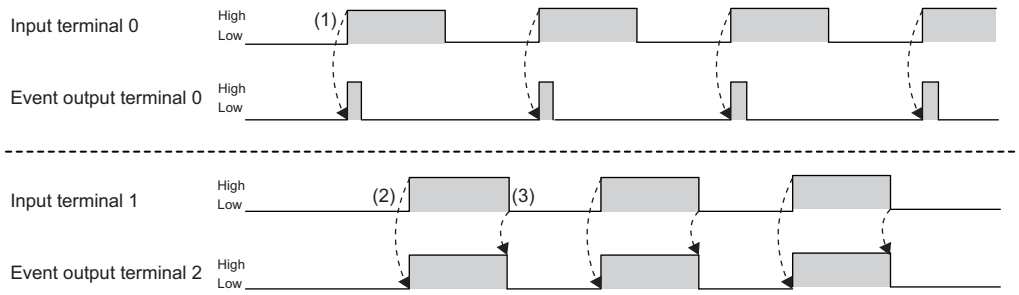
■Multi function counter block detail window

Block	Variable name	Setting value	Description
Input 0	—	—	—
Input 1	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: Rise)	Set conditions to generate an event signal.
	Detector Select	User Setting (ON only in B: High)	
Event 0	—	—	—
Event 2	—	—	—

Operation

The following shows operation where the input signal 1 turns to High when a rise of the input signal 0 is detected.

- - - - - ▶ Controlled by the flexible high-speed I/O control module



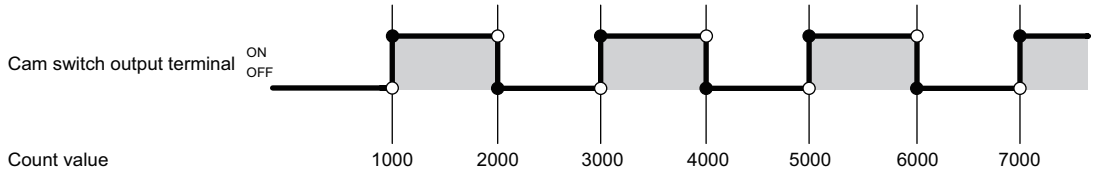
No.	Description
(1)	When a rise of the input terminal 0 is detected, the event output terminal 0 turns to High and to Low.
(2)	When a rise of the input terminal 1 is detected, the event output terminal 2 turns to High.
(3)	When a fall of the input terminal 1 is detected, the event output terminal 2 turns to Low.

10.4 Cam Switch

The preset output status of the coincidence output range is compared with a count value to switch on or off the output of the multi function counter block at each step.

The following is an example assuming that an output is switched by seven steps as follows. Note that this link example is for when a 32-bit unsigned multi function counter block is used. (The cam switch is not supported by 16-bit multi function counter blocks.)

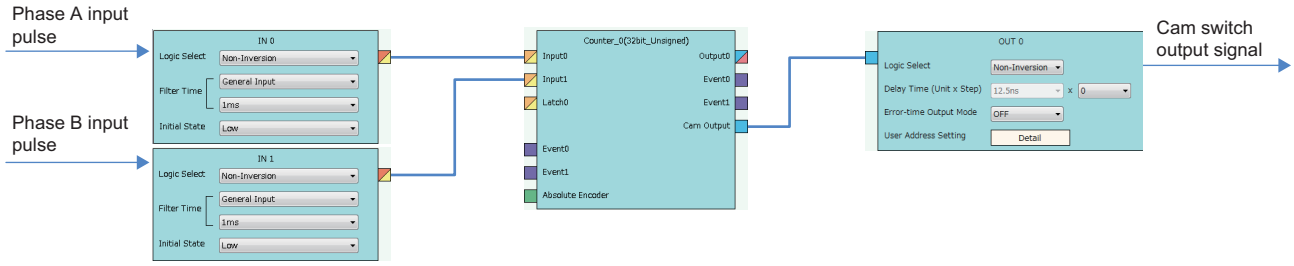
Step No.	Count value	Output
—	0 (lower limit value) to 999	Low
0	1000 to 1999	High
1	2000 to 2999	Low
2	3000 to 3999	High
3	4000 to 4999	Low
4	5000 to 5999	High
5	6000 to 6999	Low
6	7000 to 10000 (upper limit value)	High



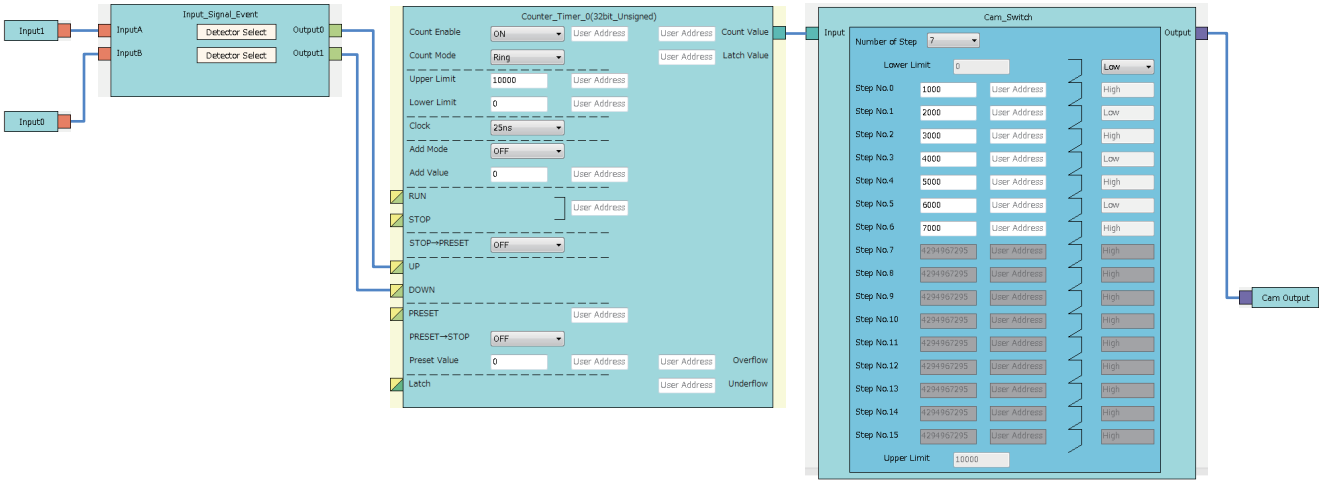
Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window

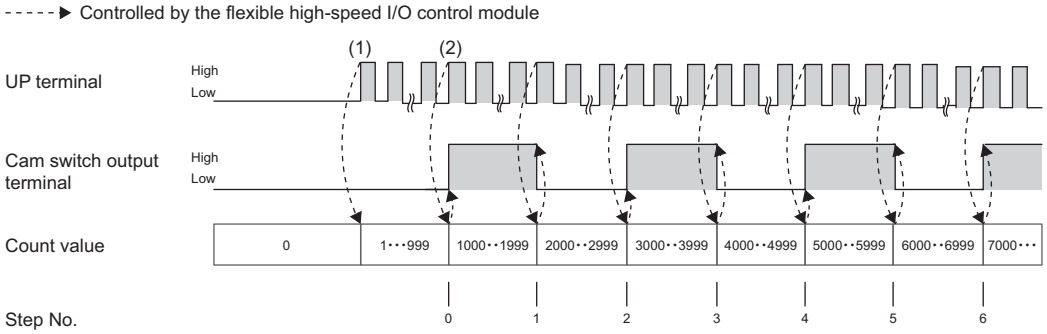


Block	Variable name	Setting value	Description
Input 0	—	—	—
Input 1	—	—	—
Input_Signal_Event	Detector Select	2-phase multiple of 1+	Set this parameter to detect an addition pulse.
	Detector Select	2-phase multiple of 1-	Set this parameter to detect a subtraction pulse.
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Ring	Set this parameter according to the control.
	Upper Limit	10000	Set this parameter according to the control.
	Lower Limit	0	Set this parameter according to the control.
	Clock	25ns	Set this parameter to "25ns". (to prevent input pulses from missing)
	Add Mode	OFF	Set this parameter according to the control.
	Add Value	0	
Cam Switch	Number of Step	7	Set "7", which is the number of steps of the cam switch, to enable the step No. 0 to 6.
	Lower Limit Output State	Low	Set this parameter according to the control.
	Step No.0	1000	Set a count value at which the output status of the subsequent step is enabled.
	Step No.1	2000	
	Step No.2	3000	
	Step No.3	4000	
	Step No.4	5000	
	Step No.5	6000	
	Step No.6	7000	
Cam Output	—	—	—

The items other than the above need not to be set.

Operation

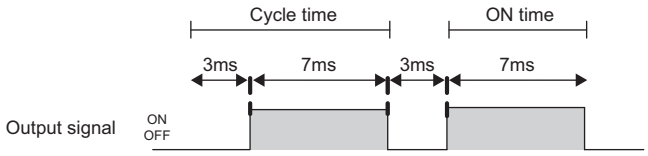
The following shows operation where a count value is compared with the setting value of each step.



No.	Description
(1)	The count value is increased by one every time the UP terminal turns to High.
(2)	When the count value reaches the setting value of the step No. 0, an external output is inversed. Also, every time the count value reaches each setting value of the step No. 1 or later, an external output is inversed.

10.5 PWM Output

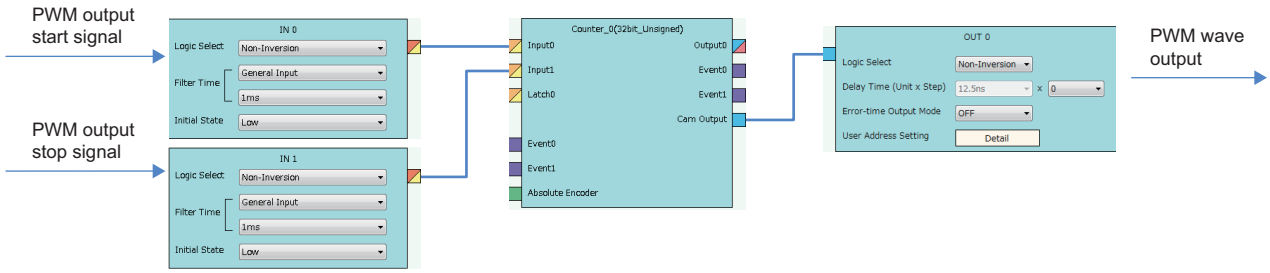
The multi function counter block outputs a PWM wave with a specified duty ratio.
The following describes a link and parameter example of a PWM output. With the example setting, when a rise of the input signal 0 is detected, output of the following PWM wave starts, and when a rise of the input signal 1 is detected, the output stops. Note that this link example is for when a 32-bit unsigned multi function counter block is used.



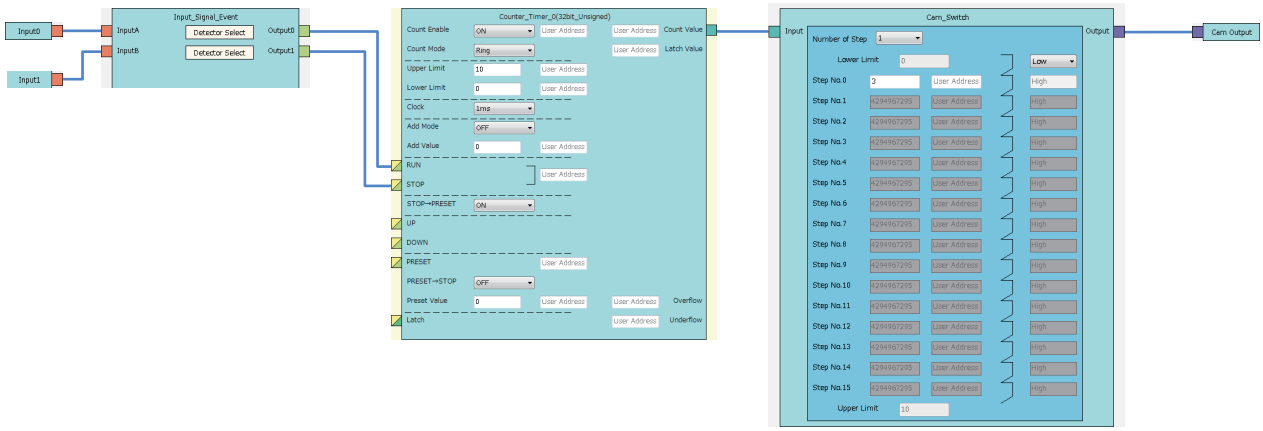
Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window



Block	Variable name	Setting value	Description
Input 0	—	—	—
Input 1	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: Rise)	Set conditions to detect a PWM output start signal.
	Detector Select	User Setting (ON only in B: Rise)	Set conditions to detect a PWM output stop signal.
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Ring	Set this parameter to "Ring".
	Upper Limit	10	Set this parameter according to the control.*1
	Lower Limit	0	Set this parameter according to the control.*1
	Clock	1ms	Set this parameter according to the control.*1*2
	Add Mode	OFF	Set this parameter according to the control.*3
	Add Value	0	
	STOP → PRESET	ON	Set this parameter to "ON", to perform a preset when a stop event occurs.
	Preset Value	0	Set the same value as that in "Lower Limit".
Cam Switch	Number of Step	1	Set "1" to enable the step No. 0.
	Lower Limit Output State	Low	Set this parameter to "Low".
	Step No.0	3	Set this parameter according to the control.*2
Cam Output	—	—	—

*1 Cycle time = (Upper limit value - Lower limit value) × Clock cycle

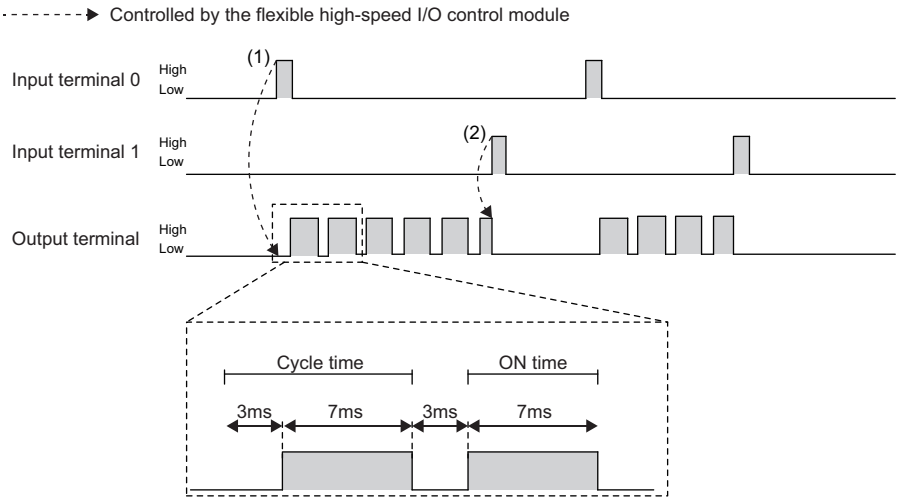
*2 ON time = Cycle time - (Step No. 0 × Clock cycle)

*3 In the addition mode, the cycle time calculated from the following is applied.
Cycle time = (Upper limit value - Lower limit value) ÷ Addition value × Clock cycle

The items other than the above need not to be set.

Operation

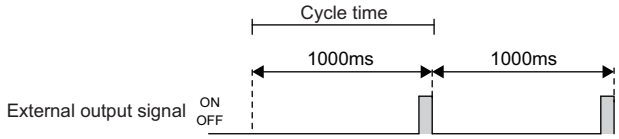
The following shows operation of when the PWM output start signal (input terminal 0) is input and when the PWM output stop signal (input terminal 1) is input.



No.	Description
(1)	When a signal is input to the input terminal 0, output of the PWM wave starts.
(2)	When a signal is input to the input terminal 1, the output of the PWM wave stops.

10.6 Fixed Cycle Output

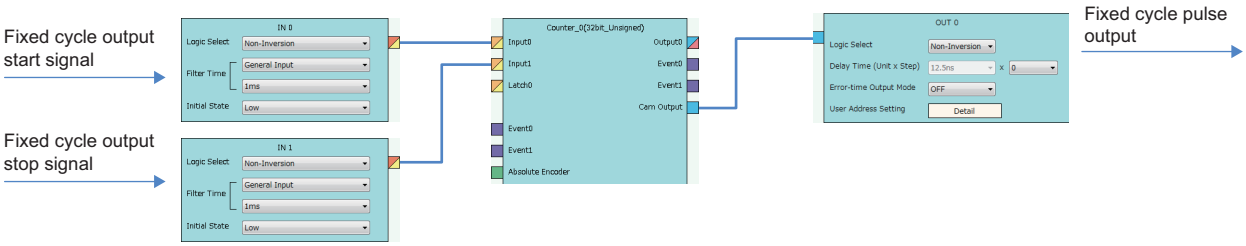
One pulse is output from the multi function counter block at specified cycle time.
The following describes a link and parameter example of a fixed cycle output. With the example setting, when a rise of the input signal 0 is detected, output of the following fixed cycle pulse starts, and when a rise of the input signal 1 is detected, the output stops. Note that this link example is for when a 32-bit unsigned multi function counter block is used.



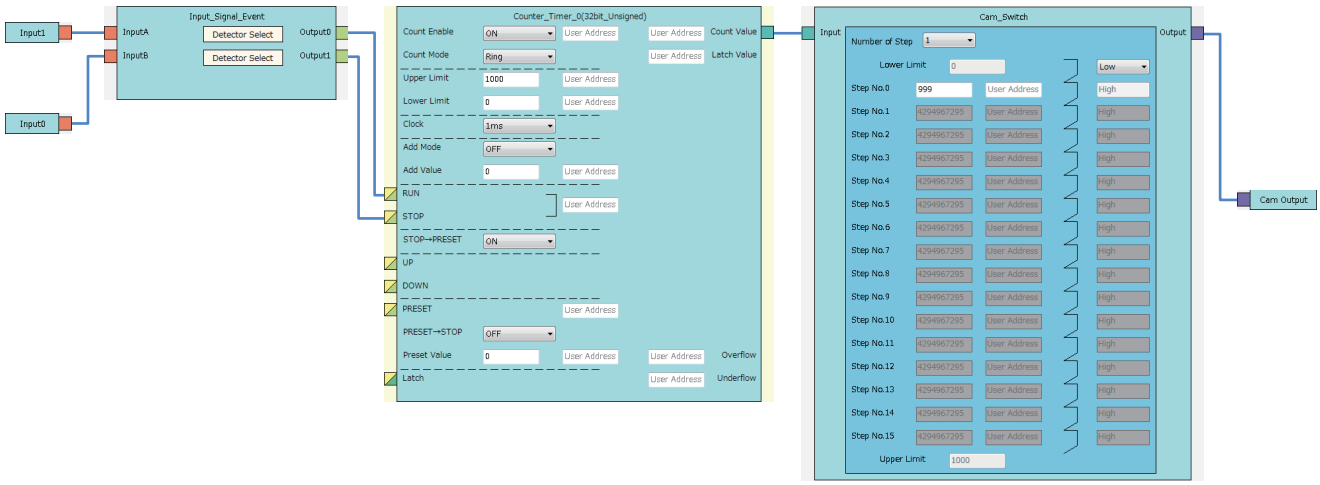
Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window



Block	Variable name	Setting value	Description
Input 0	—	—	—
Input 1	—	—	—
Event 0	—	—	—
Event 1	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: Rise)	Set conditions to detect a fixed cycle output start signal.
	Detector Select	User Setting (ON only in B: Rise)	Set conditions to detect a fixed cycle output stop signal.
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Ring	Set this parameter to "Ring".
	Upper Limit	1000	Set this parameter according to the control.*1
	Lower Limit	0	Set this parameter according to the control.*1
	Clock	1ms	Set this parameter according to the control.*1
	Add Mode	OFF	Set this parameter according to the control.*2
	Add Value	0	
	STOP → PRESET	ON	Set this parameter to "ON", to perform a preset when a stop event occurs.
	Preset Value	0	Set the same value as that in "Lower Limit".
Cam Switch	Number of Step	1	Set "1" to enable the step No. 0.
	Lower Limit Output State	Low	Set this parameter to "Low".
	Step No.0	999	Set a value of "Upper limit value of the counter timer block - 1".
Cam Output	—	—	—

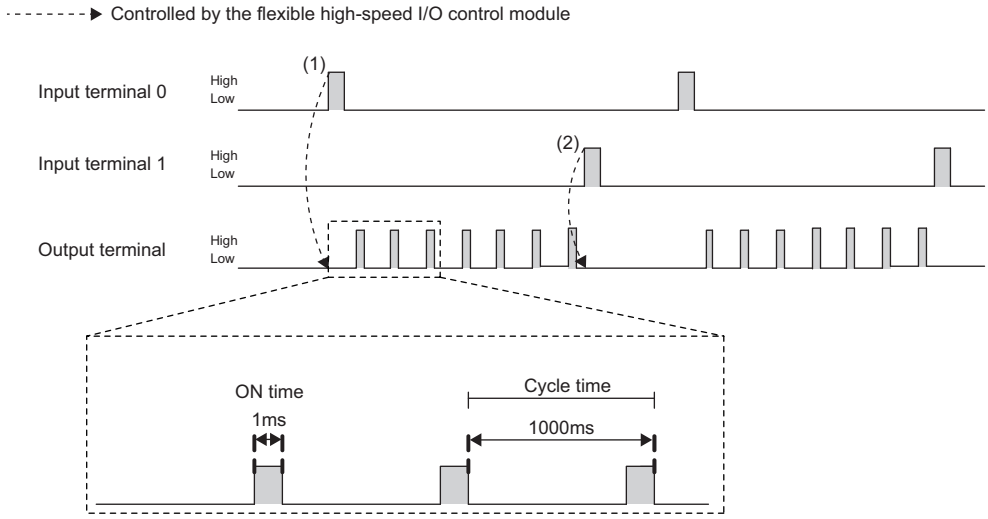
*1 Cycle time = (Upper limit value - Lower limit value) × Clock cycle

*2 In the addition mode, the cycle time calculated from the following is applied.
Cycle time = (Upper limit value - Lower limit value) ÷ Addition value × Clock cycle
However, when the count value and the setting value of Step No. 0 do not match each other with the set addition value, fixed cycle pulses are not output.

The items other than the above need not to be set.

Operation

The following shows operation of when the fixed cycle output start signal (input terminal 0) is input and when the fixed cycle output stop signal (input terminal 1) is input.



No.	Description
(1)	When a signal is input to the input terminal 0, pulse output starts. One pulse is output per cycle.
(2)	When a signal is input to the input terminal 1, the pulse output stops.

10.7 Latch Counter

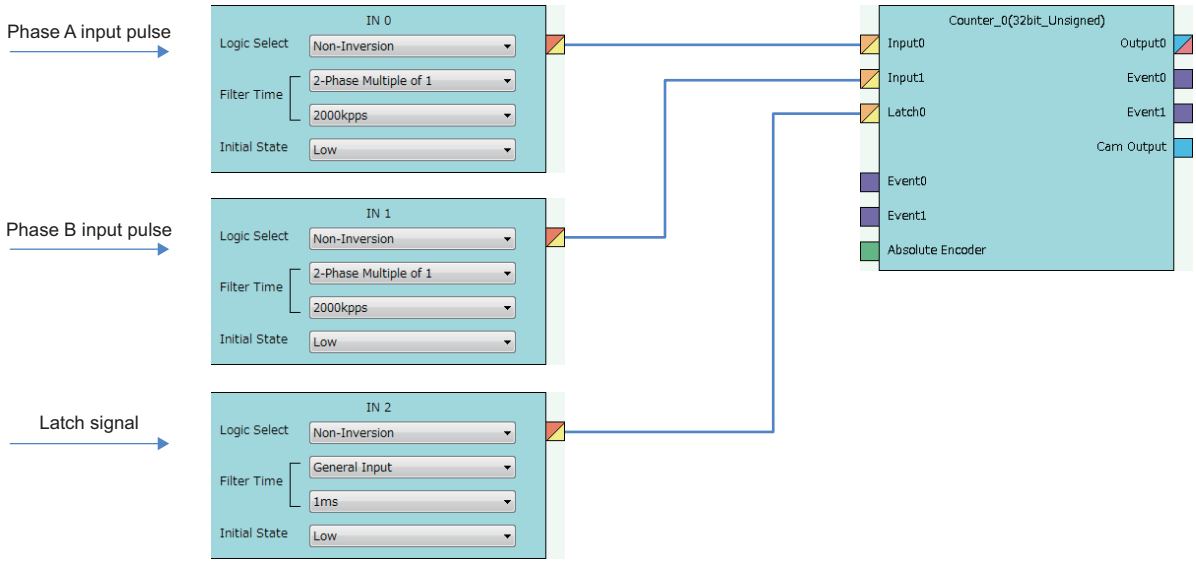
The current value is latched (held) as a latch count value.

The following describes a link and parameter example of a latch counter. With the example setting, when a rise of the latch input signal is detected, the current value is latched. Note that this link example is for when a 32-bit unsigned multi function counter block is used.

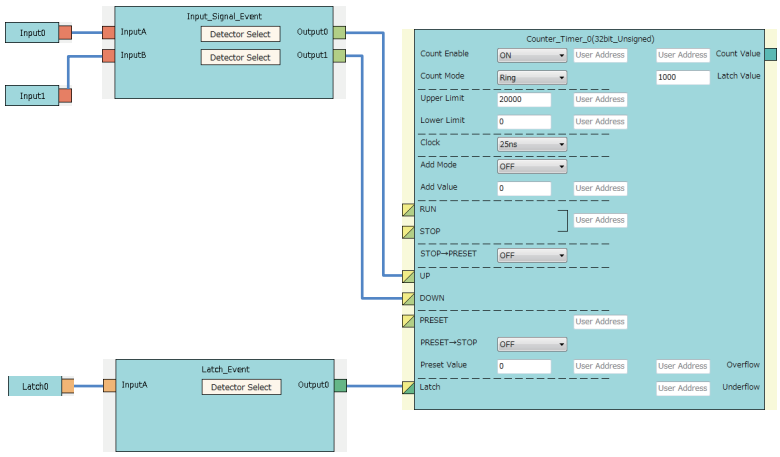
Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window

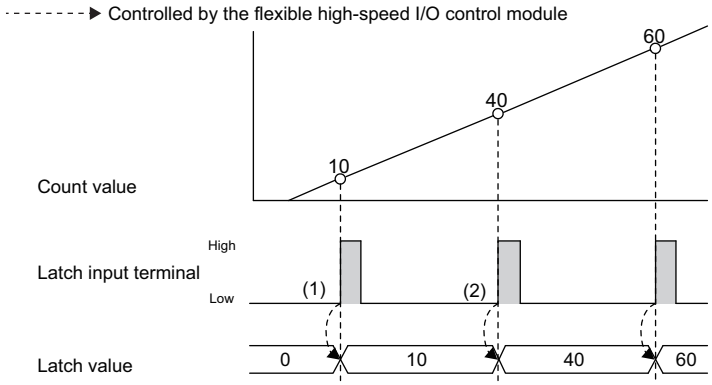


Block	Variable name	Setting value	Description
Input 0	—	—	—
Input 1	—	—	—
Latch 0	—	—	—
Input_Signal_Event	Detector Select	2-phase multiple of 1+	Set this parameter to detect an addition pulse.
	Detector Select	2-phase multiple of 1-	Set this parameter to detect a subtraction pulse.
LatchEvent	Detector Select	A: Rise	Set conditions to detect a latch signal.
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Ring	Set this parameter according to the control.
	Upper Limit	20000	Set this parameter according to the control.
	Lower Limit	0	Set this parameter according to the control.
	Clock	25ns	Set this parameter to "25ns". (to prevent input pulses from missing)
	Add Mode	OFF	Set this parameter according to the control.
	Add Value	0	
	Preset Value	0	Set the same value as that in "Lower Limit".
	Latch Value (User Address)	1000	Assign a buffer memory address.

The items other than the above need not to be set.

Operation

The following shows operation of when a latch signal is input.

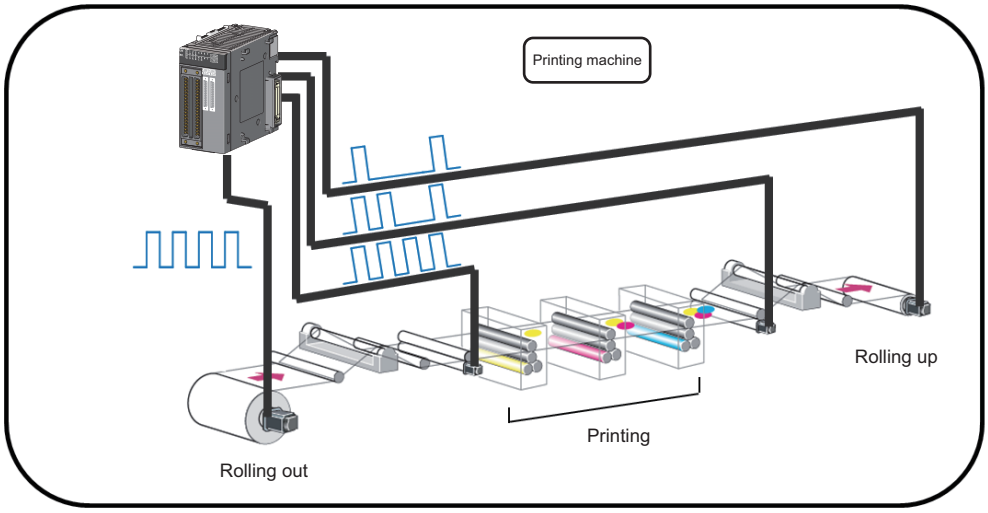


No.	Description
(1)	When a signal is input to the latch input terminal, the current count value is stored in the latch value.
(2)	When a signal is input to the latch input terminal again, the latch value is updated.

10.8 Ratio Conversion

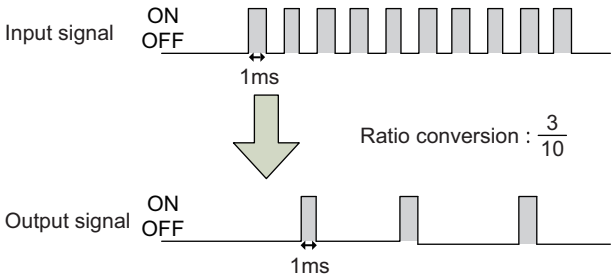
An input signal multiplied with the set ratio (x/y) is output from the multi function counter block.
Ratio conversion enables the following controls.

- An encoder output of the motor at the unwinding part is input to the programmable controller to control the motor speed of lines with distribution output.
- The motor speed of multiple lines, for example, a printer, can be controlled.



The ratio (x/y) used in ratio conversion must be "y ≥ x" when a signal multiplied by x/y is output to an input signal. Conversions with the ratio exceeding one time cannot be performed.

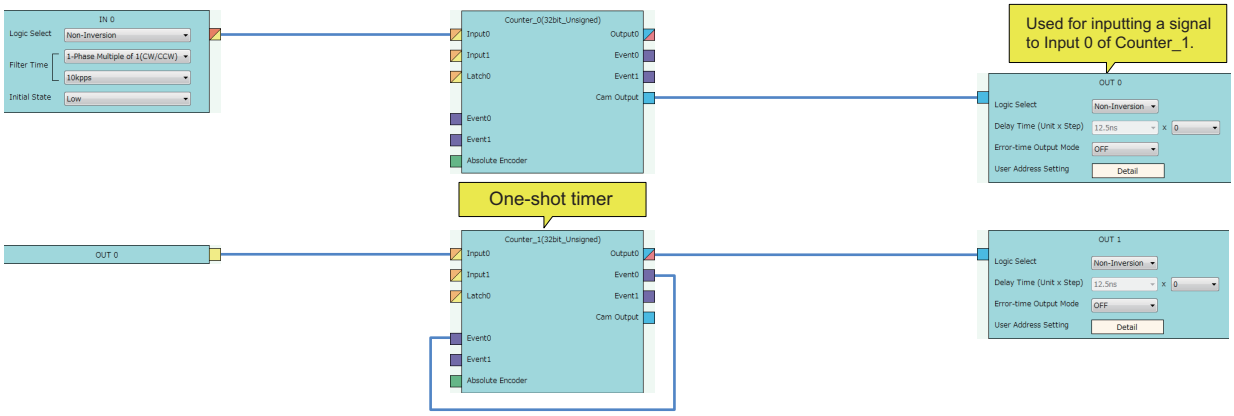
The following describes a link and parameter example of a ratio conversion. With the example setting, when a 1ms input signal is output for 1ms after multiplied with 3/10. Note that this link example is for when a 32-bit unsigned multi function counter block is used.



Link and parameter

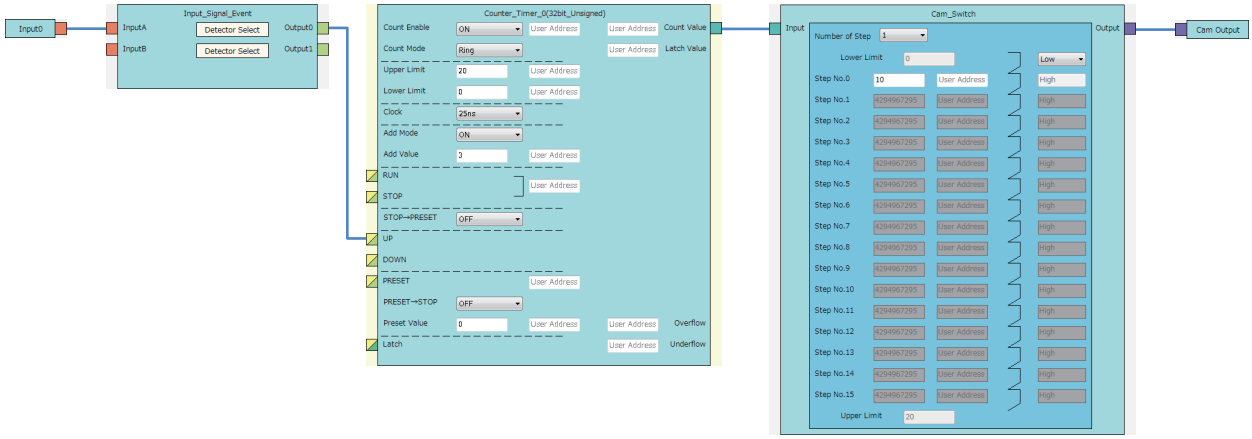
The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window

• Counter_0 (32bit_Unsigned)

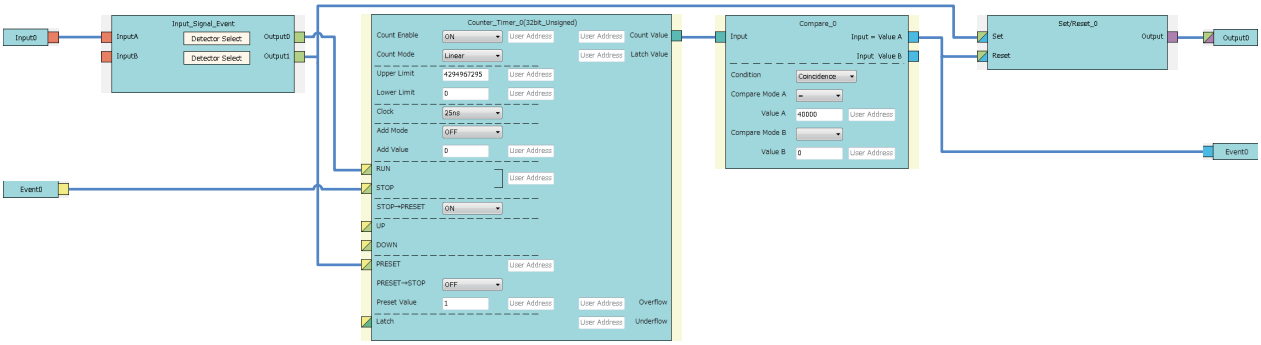


Block	Variable name	Setting value	Description
Input 0	—	—	—
Input_Signal_Event	Detector Select	User Setting (A: Rise ON, A: Fall ON)	Set "A: Rise" and "A: Fall" to "ON" and the others to "OFF".
	Detector Select	—	This parameter is not used in this link example.
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Ring	Set this parameter to "Ring".
	Upper Limit	20	Set this parameter according to the control.*1
	Lower Limit	0	Set "0".
	Clock	25ns	Set this parameter to "25ns". (to prevent input pulses from missing)
	Add Mode	ON	Set this parameter to "ON".
	Add Value	3	Set this parameter according to the control.*1
Cam_Switch	Number of Step	1	Set "1" to enable the step No. 0.
	Lower Limit Output State	Low	Set this parameter to "Low".
	Step No.0	10	Set the value of "Upper limit value of the counter timer block ÷ 2".
Cam Output	—	—	—

*1 Conversion ratio = Addition value ÷ (Upper limit value ÷ 2)

The items other than the above need not to be set.

• Counter_1 (32bit_Unsigned)



Block	Variable name	Setting value	Description
Input 0	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: High)	Set this parameter to detect the phase A input signal.
	Detector Select	User Setting (ON only in A: Rise)	
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Linear	Set this parameter according to the control.
	Upper Limit	4294967295	Set this parameter according to the control.
	Lower Limit	0	Set this parameter according to the control.
	Clock	25ns	Set this parameter according to the control.*2
	Add Mode	OFF	Set this parameter according to the control.*3
	Add Value	0	
	STOP → PRESET	ON	Set this parameter to "ON", to perform a preset when a stop event occurs.
	PRESET → STOP	OFF	Set this parameter to "OFF".
	Preset Value	1	Set this parameter according to the control.*2
Compare_0	Condition	Coincidence	Set this parameter to "Coincidence".
	Compare Mode A	=	Set this parameter to "=".
	Compare Value A	40000	Set this parameter according to the control.*2
Set/Reset_0	—	—	—
Output	—	—	—

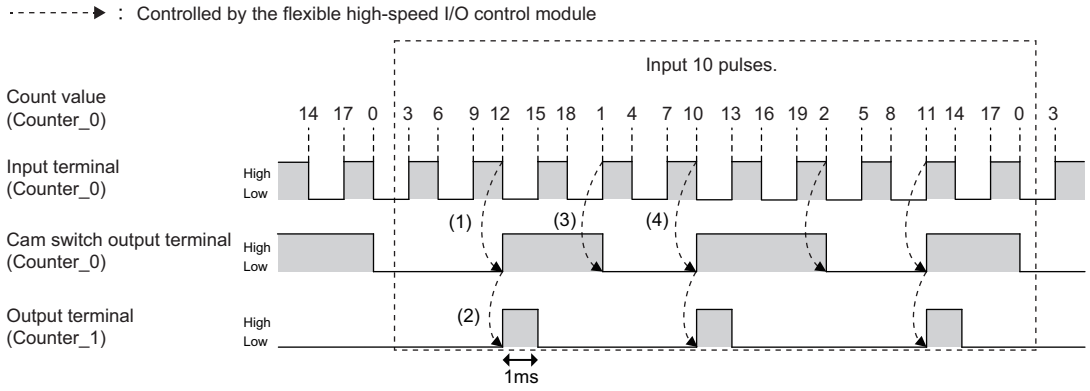
*2 Output ON time = Clock cycle setting × (Compare value - Preset value + 1)

*3 In the addition mode, the output ON time calculated from the following is applied.
Output ON time = (Clock cycle setting × (Compare value - Preset value + 1) ÷ Addition value

The items other than the above need not to be set.

Operation

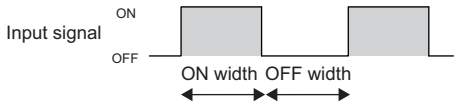
The following shows operation of ratio conversion.



No.	Description
(1)	When the count value (Counter_0) becomes equal to or larger than the setting value of the step No. 0, the cam switch output terminal (Counter_0) turns to High.
(2)	When the rise (Low to High) of the cam switch output terminal (Counter_0) is detected, the output terminal (Counter_1) turns to High and turns to Low in 1ms.
(3)	When the count value (Counter_0) falls below the setting value of the step No. 0, the cam switch output terminal (Counter_0) is turns to Low.
(4)	When the count value (Counter_0) becomes equal to or larger than the setting value of the step No. 0 again, the cam switch output terminal (Counter_0) turns to High. The operations 1) to 3) above are repeated, and signals of 3 pulses are output for inputs of 10 pulses.

10.9 Pulse Measurement

The ON width or OFF width of an input signal is measured.

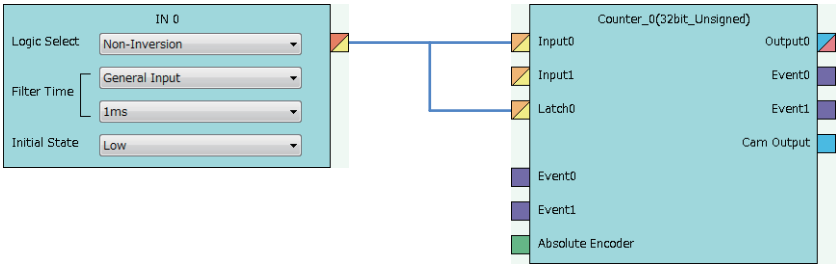


The following describes a link and parameter example of a pulse measurement. With the example setting, the ON width (latch value × 25ns) of the input signal is measured. Note that this link example is for when a 32-bit unsigned multi function counter block is used.

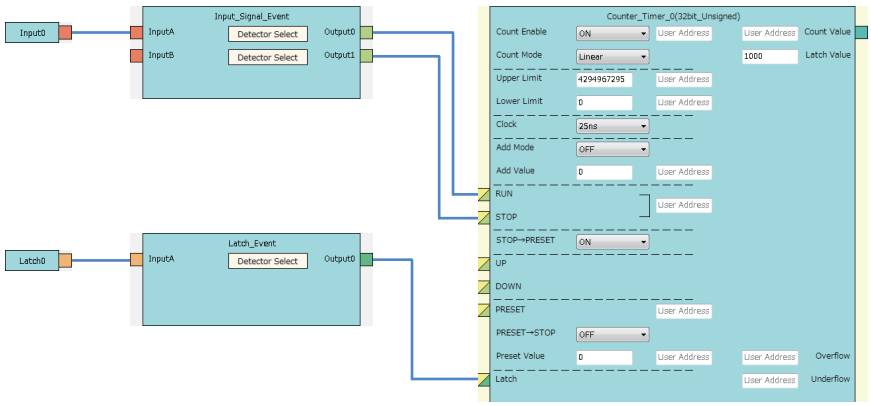
Link and parameter

The following shows a link example of the hardware logic outline window and a link example and parameter setting example of the multi function counter block detail window.

■Hardware logic outline window



■Multi function counter block detail window



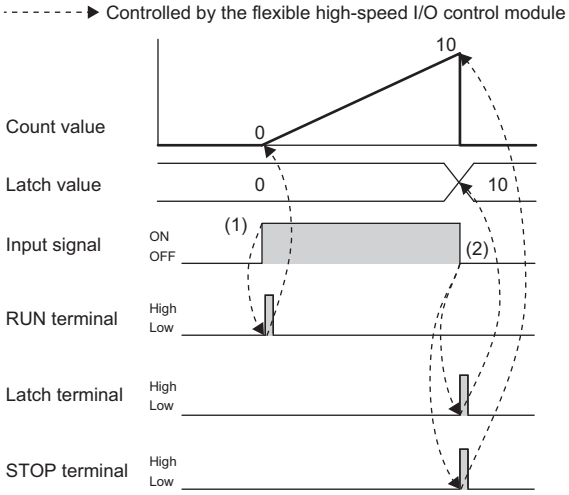
Block	Variable name	Setting value	Description
Input 0	—	—	—
Latch 0	—	—	—
Input_Signal_Event	Detector Select	User Setting (ON only in A: Rise)*1	Set "Only A: Rise is on".
	Detector Select	User Setting (ON only in A: Fall)*1	Set "ON only in A: Fall".
Latch_Event	Detector Select	User Setting (ON only in A: Fall)*1	Set "ON only in A: Fall".
Counter_Timer_0	Count Enable	ON	Set this parameter to "ON".
	Count Mode	Linear	Set this parameter to "Linear".
	Upper Limit	4294967295	Set "4294967295", to widen the pulse measurement width.
	Lower Limit	0	Set "0".
	Clock	25ns	Set this parameter to "25ns". (to prevent input pulses from missing)
	Add Mode	OFF	Set the addition mode to "OFF". (No addition in this example)
	Add Value	0	
	STOP → PRESET	ON	Set this parameter to "ON", to perform a preset when a stop event occurs.
	Preset Value	0	Set this parameter to 0.
	Latch Value (User Address)	1000	Assign a buffer memory address.

*1 Set the following to measure the OFF width.
Detector of Input_Signal_Event linked with the RUN terminal: ON only in A: Fall
Detector of Input_Signal_Event linked with the STOP terminal: ON only in A: Rise
Detector of Latch_Event linked with the Latch terminal: ON only in A: Rise

The items other than the above need not to be set.

Operation

The following shows operation of pulse measurement.



No.	Description
(1)	When the input signal is turned on, the RUN terminal turns to High and counting per clock cycle starts.
(2)	When the input signal is turned off, the following two operations are simultaneously performed. • The Latch terminal turns to High and the current count value is latched. • The STOP terminal turns to High, counting per clock cycle stops and preset is performed.

11 SETTINGS

This chapter describes the setting methods for the flexible high-speed I/O control module.

Point

- To enable the settings of adding a new module and auto refresh, write the changed settings in the CPU module, and reset the CPU module, set the RUN/STOP/RESET switch from STOP to RUN twice, or turn off and on the power.
- To enable the switch setting, write the changed setting in the CPU module, and reset the CPU module or turn off and on the power.

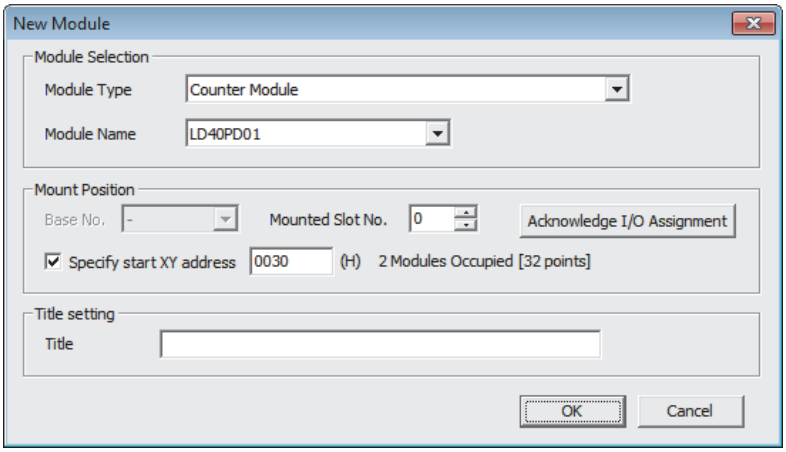
11.1 Adding the Module

Add the model name of the flexible high-speed I/O control module used in the project.

Addition method

Add the model name in "New Module".

[Project window] ⇨ [Intelligent Function Module] ⇨ Right-click ⇨ [New Module]

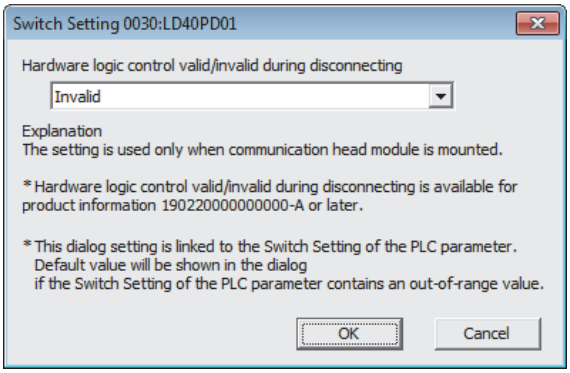


Item		Description
Module Selection	Module Type	Set "Counter Module".
	Module Name	Set the module model name to be connected.
Mount Position	Mounted Slot No.	Set a slot number where the target module is connected.
	Specify start XY address	The start I/O number (hexadecimal) of the target module is set according to the slot number where the module is connected. An arbitrary number can also be set.
Title setting	Title	Set any title.

11.2 Switch Setting

Set whether to invalid or valid the hardware logic control at disconnection.

[Project window] ⇨ [Intelligent Function Module] ⇨ Module model name ⇨ [Switch Setting]



Item	Description	Setting value
Hardware logic control valid/invalid during disconnecting	Set the hardware logic control status of when the own station is disconnected during hardware logic control.	Invalid (default value) Valid

11.3 Auto Refresh

Set the buffer memory areas of the flexible high-speed I/O control module to be refreshed automatically.
The auto refresh setting eliminates the need for reading data by using a program.

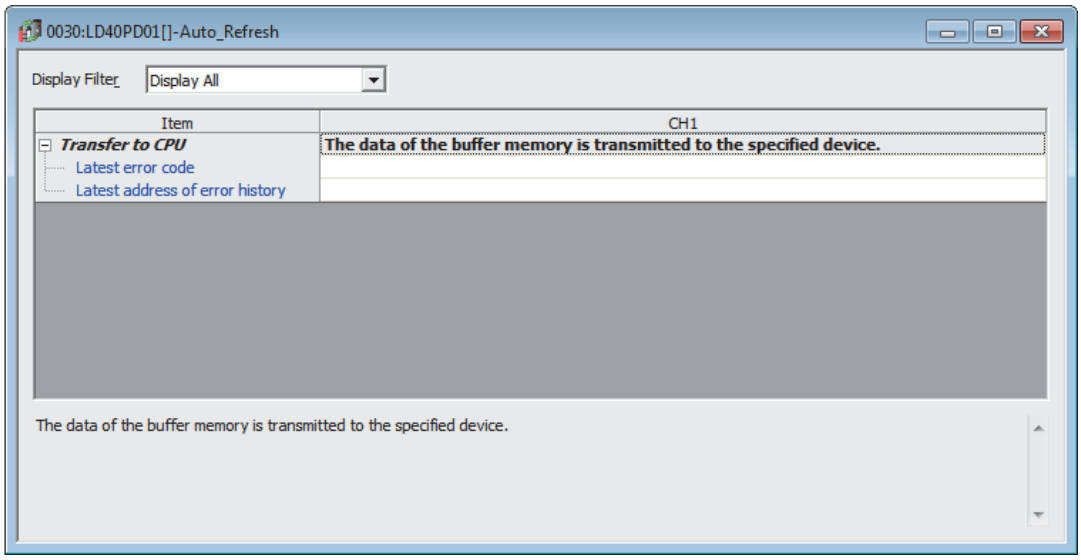
Setting method

Set the auto refresh in "Auto Refresh".

1. Open the "Auto Refresh" window.

[Project window] ⇨ [Intelligent Function Module] ⇨ Module model name ⇨ [Auto Refresh]

2. Click the item to be set to enter the auto refresh target device.



Point

The usable devices are X, Y, M, L, B, T, C, ST, D, W, R, and ZR.
When the bit device X, Y, M, L, or B is used, set a number that is divisible by 16 points, such as X10, Y120, and M16. Buffer memory data of 16 points is stored from the set device number. (Example: When X10 is set, data is stored in X10 to X1F.)

12 DISPLAY UNIT

This chapter describes display unit functions that can be used for the flexible high-speed I/O control module.
For details on operations, functions, and menu structure of the display unit, refer to the following.
MELSEC-L CPU Module User's Manual (Function Explanation, Program Fundamentals)

12.1 Features

The display unit is a liquid crystal display that can be connected to the CPU module. Connecting it to the CPU module allows checking the system status without using software packages.
When a trouble occurs, the display unit displays error information and a cause of the trouble can be specified.

12.2 Checking and Clearing Errors

With operations on the display unit, errors that have occurred in the flexible high-speed I/O control module can be checked. In addition, errors that have occurred and have not been cleared yet can be cleared.

Checking errors

Check errors that have occurred in the flexible high-speed I/O control module by specifying Latest error code (Un\G100) in "BUF MEM MON/TES".

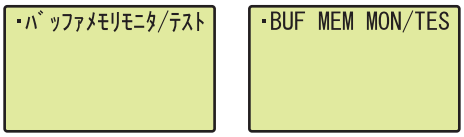
For details on the error codes, refer to the following.

☞ Page 238 List of Error Codes

Ex.

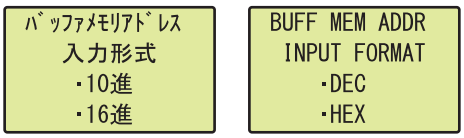
When an error has occurred in the flexible high-speed I/O control module with the start I/O number 10

"BUF MEM MON/TES" window



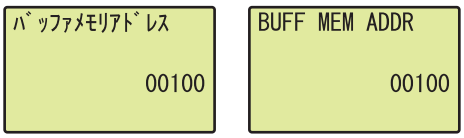
1. Press the OK button.

"BUFF MEM ADDR INPUT FORMAT" window



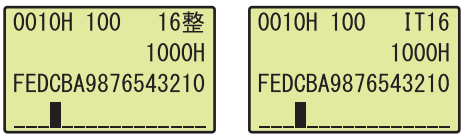
2. Set the buffer memory address input type to "DEC" with the ▲ and ▼ buttons, and press the OK button.

"BUFF MEM ADDR" window



3. Move the cursor with the ◀ and ▶ buttons, and increase or decrease the value selected with the cursor to 100 with the ▲ and ▼ buttons. Press the OK button.

Buffer memory monitor window



4. Check the error that has occurred in the buffer memory monitor window.

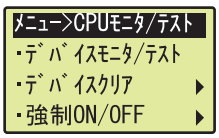
Clearing errors

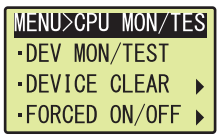
Clear errors by eliminating error causes and turning on and off Error clear request (YF) in "DEV MON/TEST".

Ex.

When an error has occurred in the flexible high-speed I/O control module with the start I/O number 10

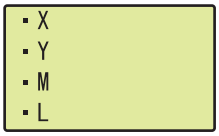
"CPU MON/TES" window

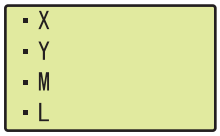




1. Select "DEV MON/TEST" with the ▲ and ▼ buttons, and press the OK button.

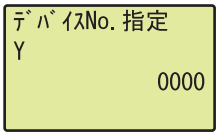
Device selection window

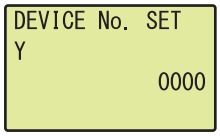




2. Select Y as a target device with the ▲ and ▼ buttons, and press the OK button.

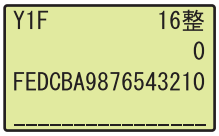
"DEVICE No. SET" window

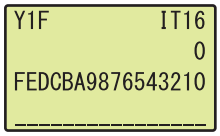




3. Set the target device to Error clear request (Y1F), and press the OK button.

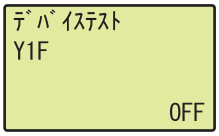
Device monitor window

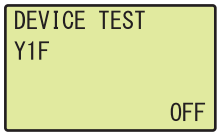




4. Press the OK button.

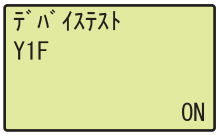
"DEVICE TEST" window

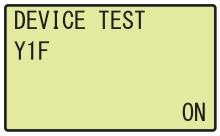




5. Turn on the device with the ▲ and ▼ buttons.

"DEVICE TEST" window





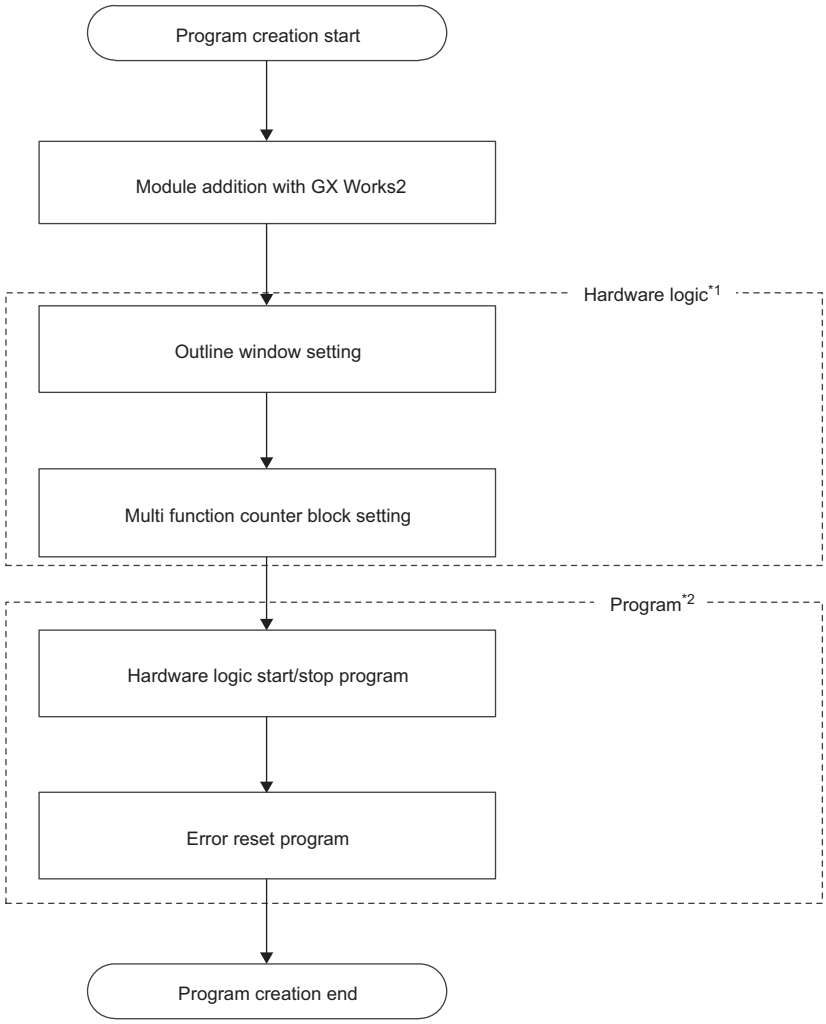
6. Press the OK button.

13 PROGRAMMING

This chapter describes the programming procedure and basic programs of the flexible high-speed I/O control module.

13.1 Programming Procedure

Create programs for executing the flexible high-speed I/O control module with the following procedure.



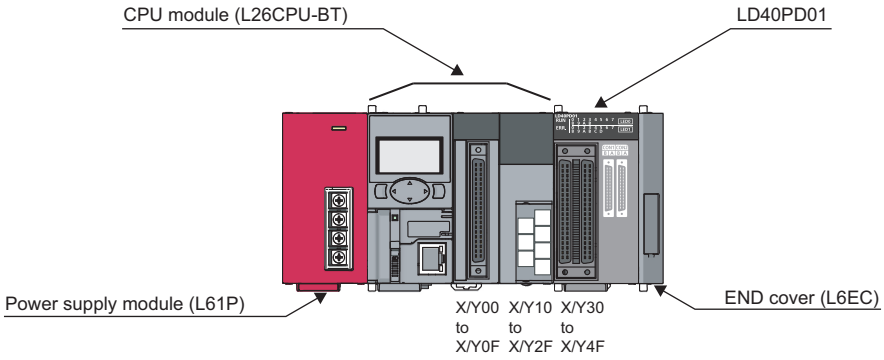
*1 Set the hardware logic with the configuration tool.
*2 Create programs with GX Works2.

13.2 When the Module Is Used with the Standard System Configuration

This section shows a program example with the following system configuration and conditions.

System configuration

The following figure shows a system configuration example.



Programming conditions

The program counts pulses (2-phase multiple of 4) input to the flexible high-speed I/O control module with the multi function counter block.

Adding the module

Add the flexible high-speed I/O control module on GX Works2.

For details on adding the module, refer to the following.

☞ Page 204 Adding the Module

Use the default values for the switch setting and auto refresh setting in these program examples.

Starting the configuration tool

Start the configuration tool with the following procedure.

☞ Page 64 Starting and Exiting the Configuration Tool

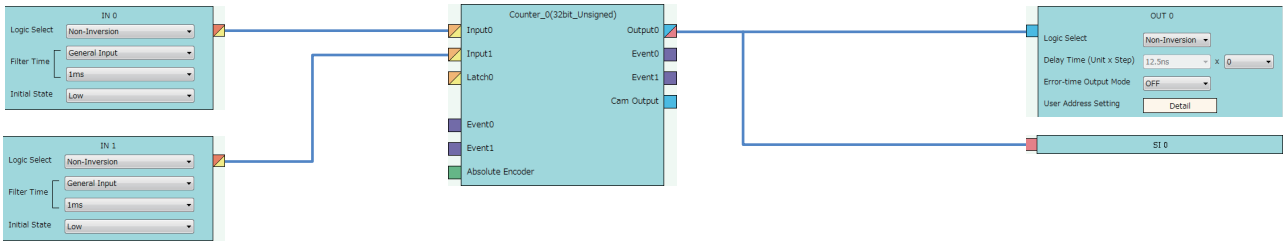
Creating a hardware logic

Create a hardware logic with the configuration tool.

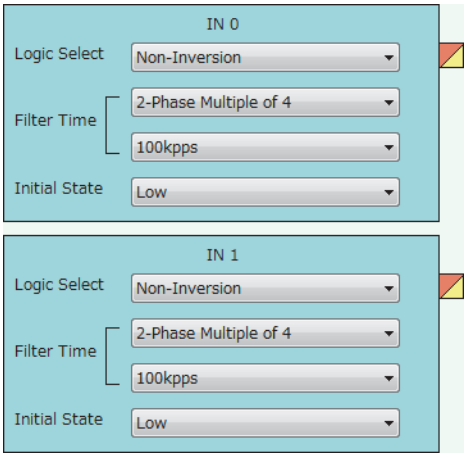
■Link and settings in the hardware logic outline window

1. Arrange a 32-bit unsigned multi function counter block in the hardware logic outline window, and link it to external input blocks.

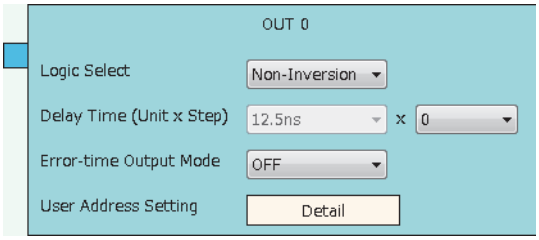
- To perform external outputs according to the counting result, link the multi function counter block to an external output block.
- To start an interrupt program according to the counting result, link the multi function counter block to an SI device terminal. (☞ Page 216 Interrupt program example)



2. Set the external input blocks according to the specifications of external input signals.

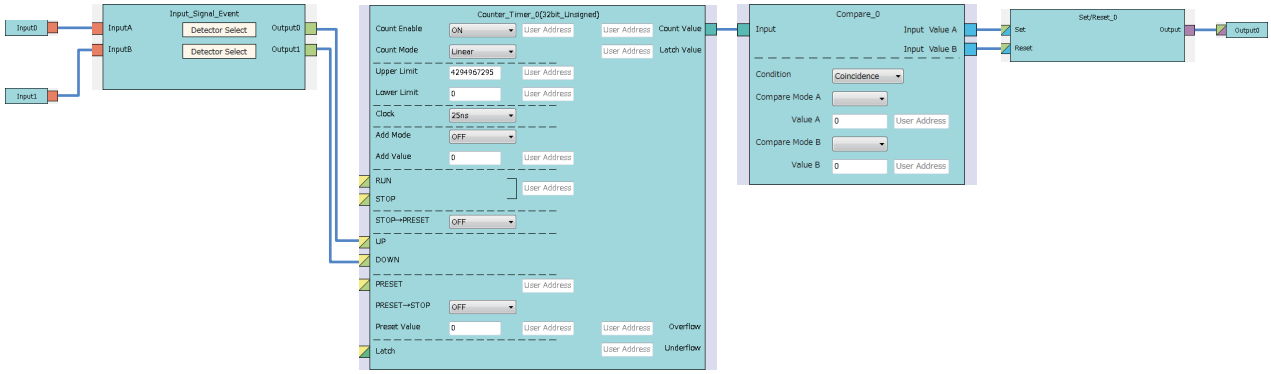


3. To use the external output block, set it according to the specifications of external output signals and desired output timings.

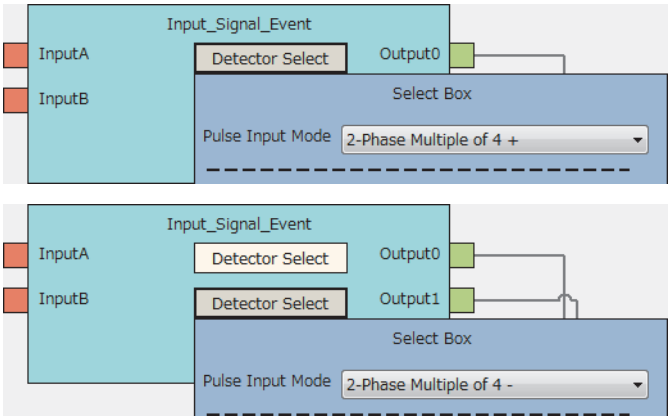


■Link and settings in the multi function counter block detail window

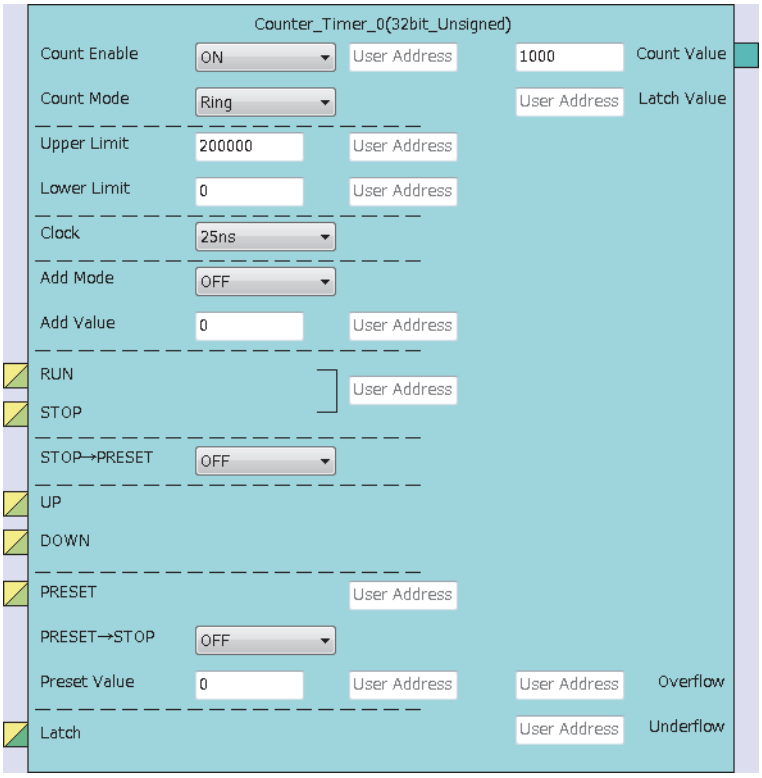
1. Link blocks in the multi function counter block detail window as shown below.



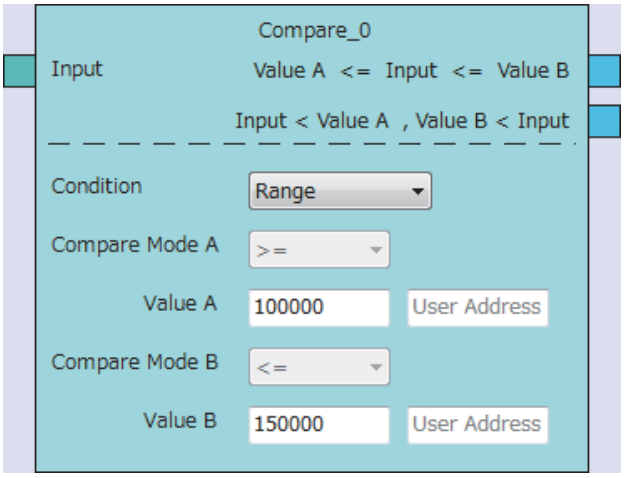
2. Set the setting values of the input signal event detection blocks as shown below.



3. Set the setting values of the counter timer block as shown below.



4. Set the setting values of the comparison block as shown below.



■Writing data to the module

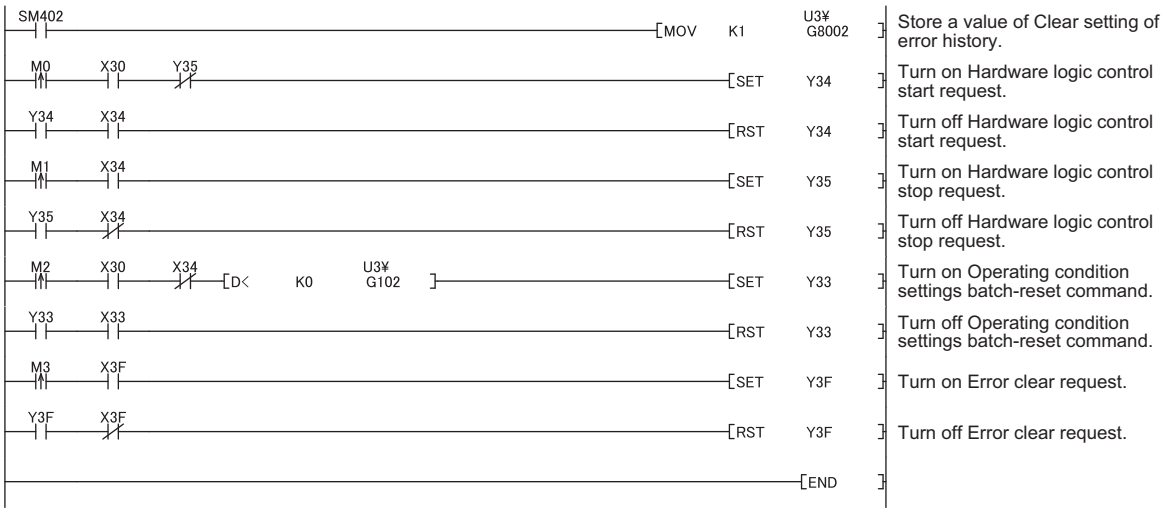
Write a project to the CPU module with GX Works2. Write the hardware logic to the flexible high-speed I/O control module with the configuration tool.

Program example

■User devices

Device	Description
M0	Hardware logic control start
M1	Hardware logic control stop
M2	Operating condition settings batch-reset
M3	Error reset command
X30	Module ready
X33	Operating condition settings batch-reset complete flag
X34	Hardware logic control flag
X3F	Error flag
Y33	Operating condition settings batch-reset command
Y34	Hardware logic control start request
Y35	Hardware logic control stop request
Y3F	Error clear request

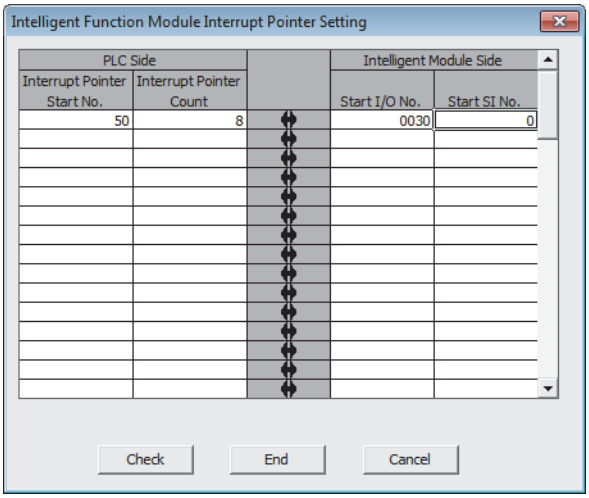
■Program example



Interrupt program example

■Interrupt pointer setting

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [PLC System] ⇨ "Intelligent Function Module Setting" ⇨ [Interrupt Pointer Setting] button

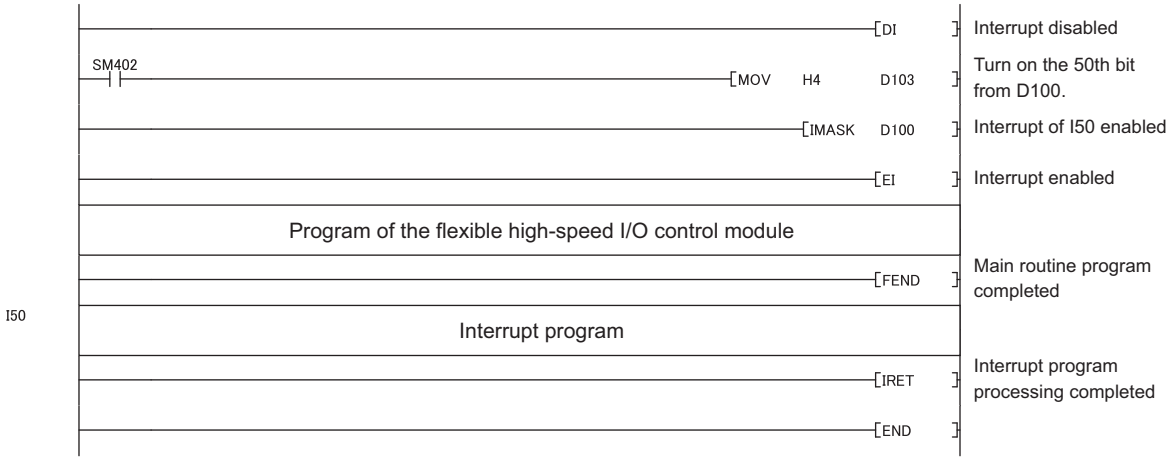


■User devices

Device	Description
D100 to D115	Interrupt enable flag storage for IMASK instruction

■Program example

Before using an interrupt pointer, enable an interrupt with the IMASK instruction.



Point

- When the program above is executed, the I50 interrupt program is enabled, and all other interrupt programs are disabled. To execute any interrupt program other than the I50 interrupt program, set the bit that corresponds to the target interrupt pointer to "1: enabled".
- For details on the IMASK instruction, refer to the following (MELSEC-Q/L Programming Manual (Common Instruction)).

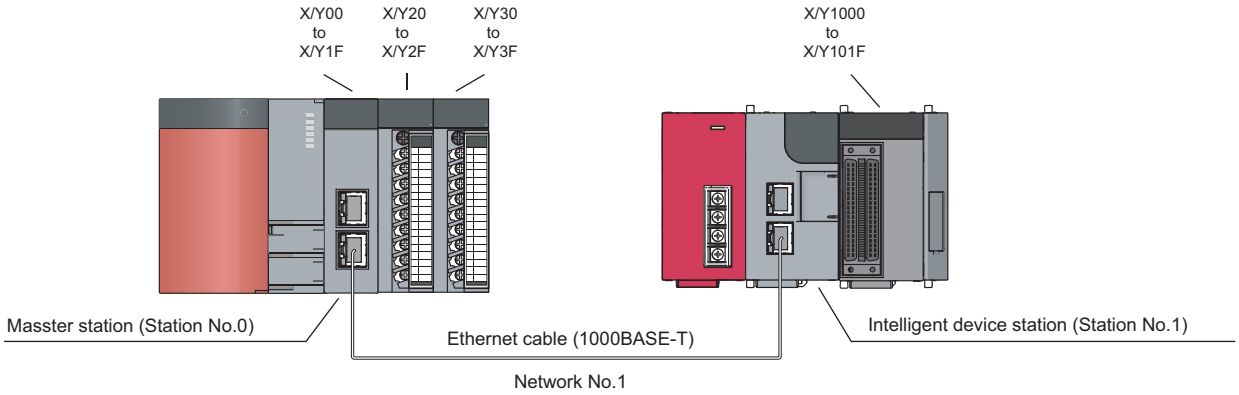
13.3 When the Module Is Connected to a Head Module

This section shows a program example with the following system configuration and conditions of the flexible high-speed I/O control module.

System configuration

Power supply module (Q62P)
CPU module (Q10UDHCPU)
Master/local module (QJ71GF11-T2)
Input module (QX10)
Output module (QY40P)

Power supply module (L61P)
Head module (LJ72GF15-T2)
Flexible high-speed I/O control module (LD40PD01)
END cover (L6EC)



Programming conditions

The program counts pulses (2-phase multiple of 4) input to the flexible high-speed I/O control module with the multi function counter block.

User devices

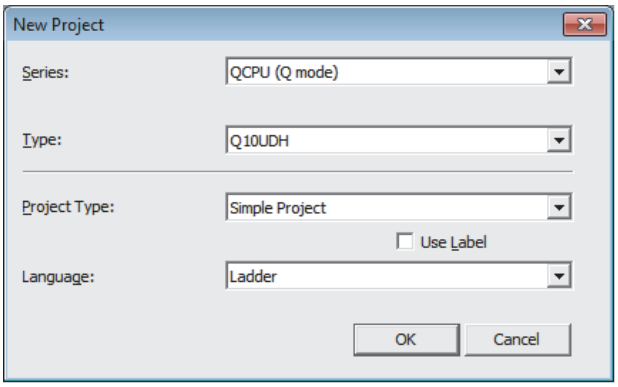
Device	Description
M100	Setting start command
M110	Hardware logic control start command
M111	Hardware logic control stop command
M112	Count value read command
M113	Operating condition batch-reset command
M114	Hardware logic control stop flag clear command at disconnection
M120	Error reset command
M200, M201	Write complete flag
M210, M211	Read complete flag 1
M220, M221	Read complete flag 2
M300	Count value reading flag
M310	Number of writes to a flash ROM reading flag
M1000	Communication ready flag (station number 1)
M1001	Setting request at a startup
M1002	Setting request signal
M1003	Setting complete flag at a startup
D100 (W1010)	Storing the latest error code
D200, D201	Storing the cumulative number of write accesses to a flash ROM
D1000	Storing the clear setting of error history
D1010, D1011	Count value
F200	Parameter write complete with an error
F210	Count value read complete with an error
F220	Number of writes to a flash ROM read complete with an error

Settings on the master station side

1. Create a project of GX Works2.

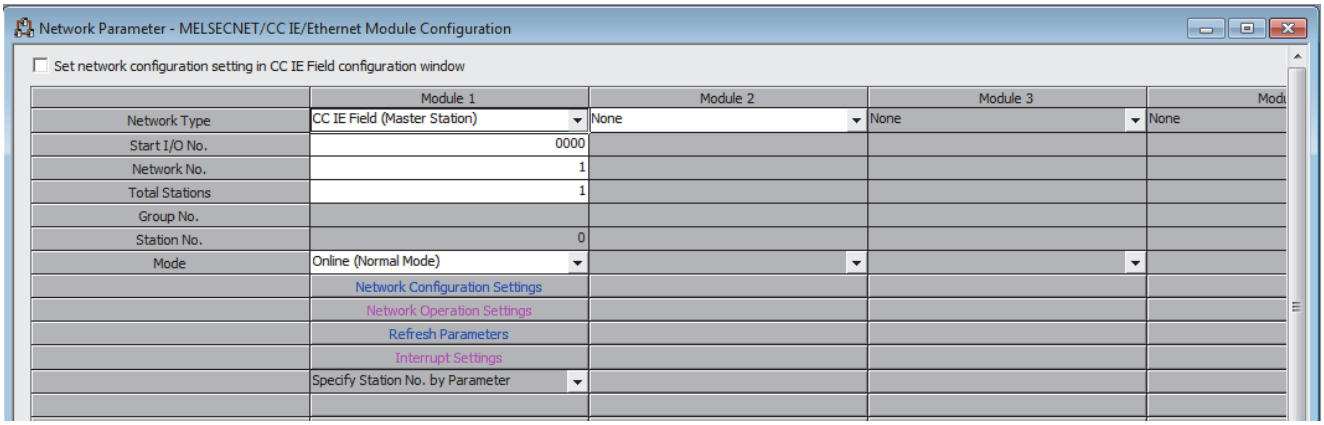
Select "QCPU (Q mode)" in "Series" and select "Q10UDH" in "Type".

[Project] ⇨ [New]



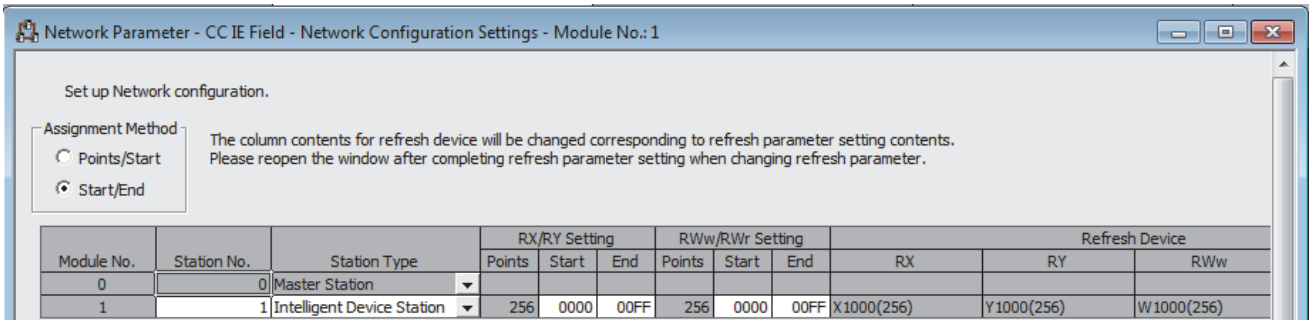
2. Display the setting window for the network parameters and set the values as follows.

[Project window] ⇨ [Parameter] ⇨ [Network Parameter] ⇨ [Ethernet / CC IE / MELSECNET]



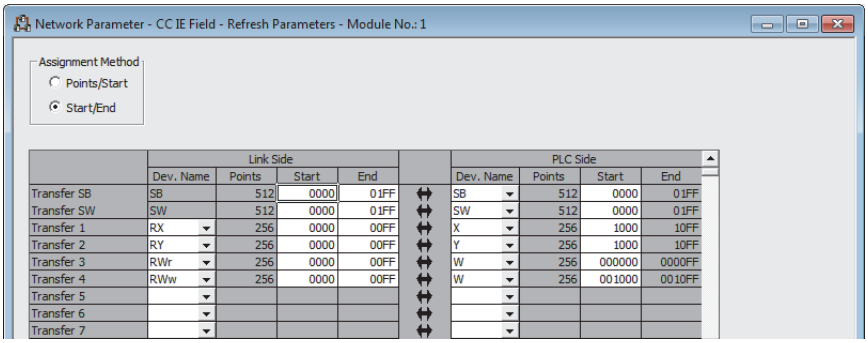
3. Display the setting window for the network configuration settings and set the values as follows.

[Project window] ⇨ [Parameter] ⇨ [Network Parameter] ⇨ [Ethernet / CC IE / MELSECNET] ⇨ Network Configuration Settings button



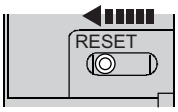
4. Display the setting window for the refresh parameters and set the values as follows.

[Project window] ⇨ [Parameter] ⇨ [Network Parameter] ⇨ [Ethernet / CC IE / MELSECNET] ⇨ Refresh Parameters button



5. Write the set parameters to the CPU module on the master station. Then reset the CPU module or power off and on the programmable controller.

[Online] ⇨ [Write to PLC]



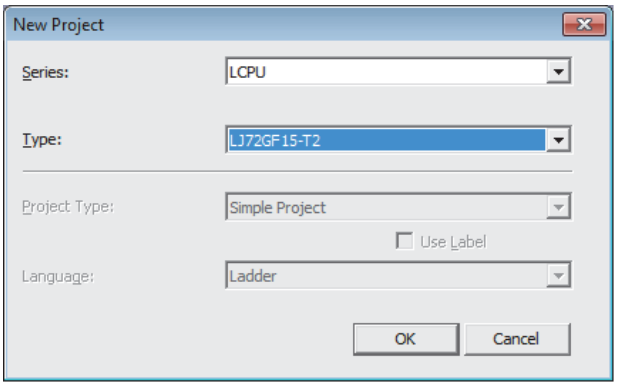
or Power OFF → ON

Setting on the intelligent device station side

1. Create a project of GX Works2.

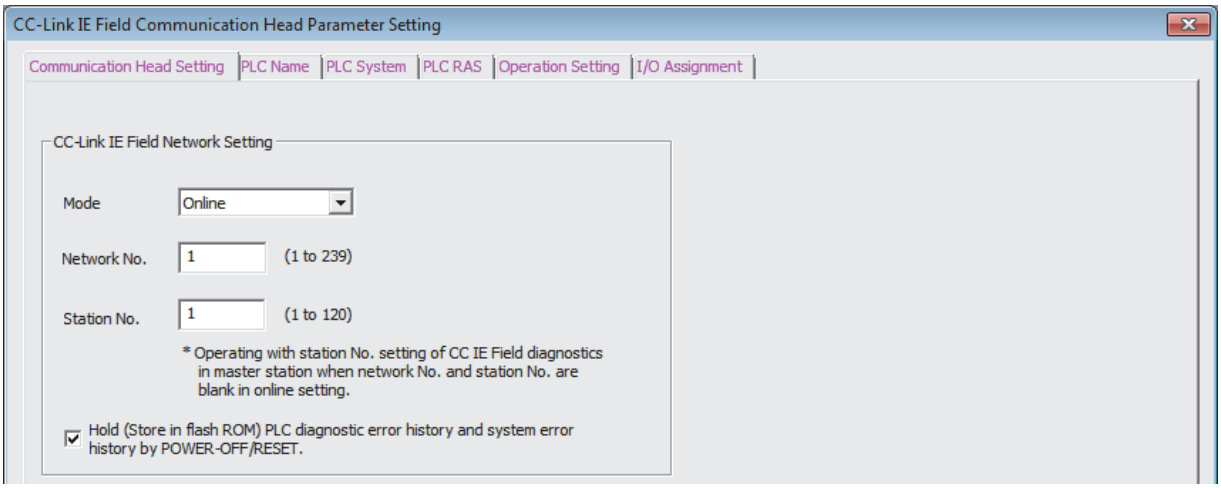
Select "LCPU" in "Series" and select "LJ72GF15-T2" in "Type".

[Project] ⇨ [New]



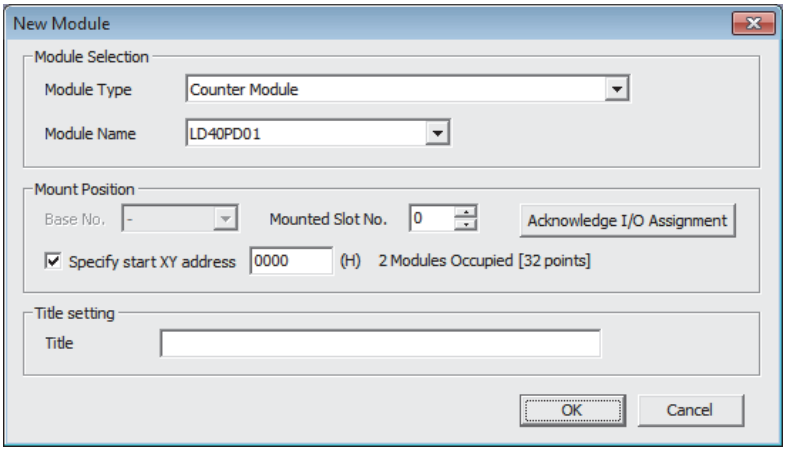
2. Display the setting window for the PLC parameters and set the values as follows.

[Project window] ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ "Communication Head Setting"



3. Add the flexible high-speed I/O control module (LD40PD01) to the project of GX Works2.

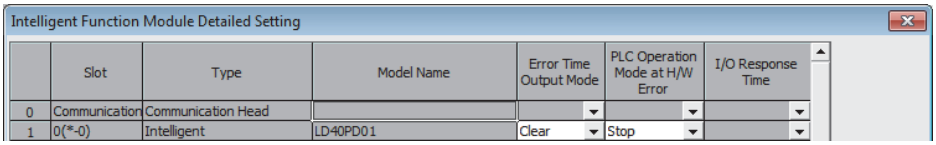
[Project window] ⇨ [Intelligent Function Module] ⇨ Right-click ⇨ [New Module]



13

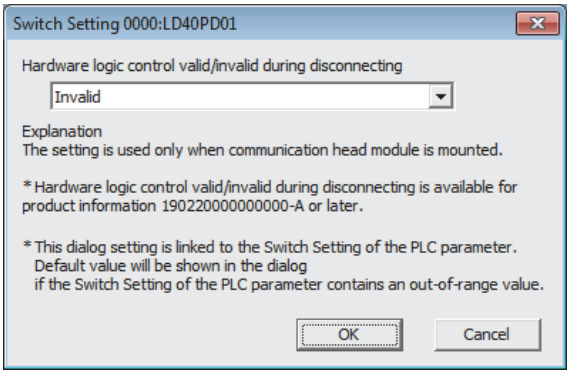
4. Display the setting window for the intelligent function module detailed setting of the flexible high-speed I/O control module (LD40PD01) and set the values as follows.

[Project window] ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [I/O Assignment] ⇨ Detailed Setting button



5. Display the setting window for the switch setting of the flexible high-speed I/O control module (LD40PD01) and set the value as follows.

[Project window] ⇨ [Intelligent Function Module] ⇨ Module model name ⇨ [Switch Setting]

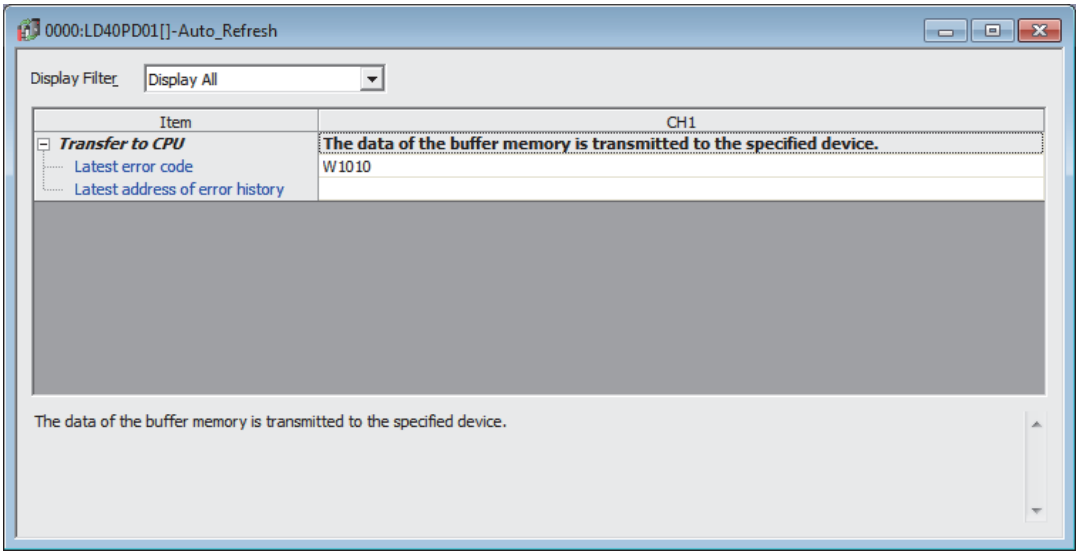


When the own station is disconnected, the operations of the flexible high-speed I/O control module differ depending on the setting of "Hardware logic control valid/invalid during disconnecting" in the switch setting or that of "Error Time Output Mode" in the intelligent function module detailed setting. For details, refer to the following.

☞ Page 229 Operations of the flexible high-speed I/O control module when the head module is connected

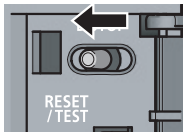
6. Display the setting window for the auto refresh setting of the flexible high-speed I/O control module (LD40PD01) and set the values as follows.

[Project window] ⇨ [Intelligent Function Module] ⇨ Module model name ⇨ [Auto Refresh]



7. Write the set parameters to the head module. Then reset the head module or power off and on the programmable controller.

[Online] ⇨ [Write to PLC]



or Power OFF → ON

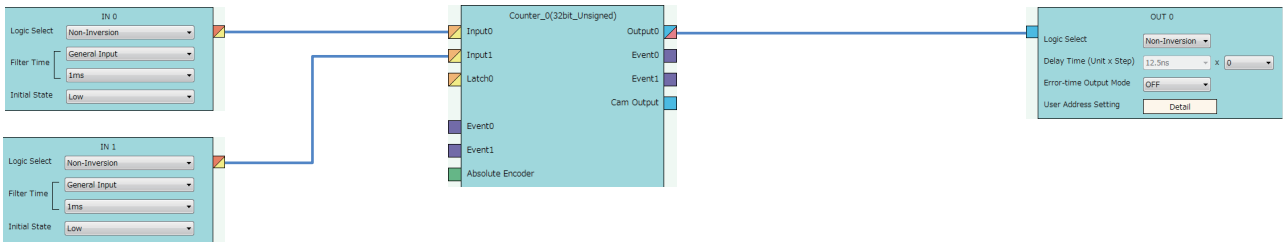
Creating a hardware logic

Create a hardware logic with the configuration tool.

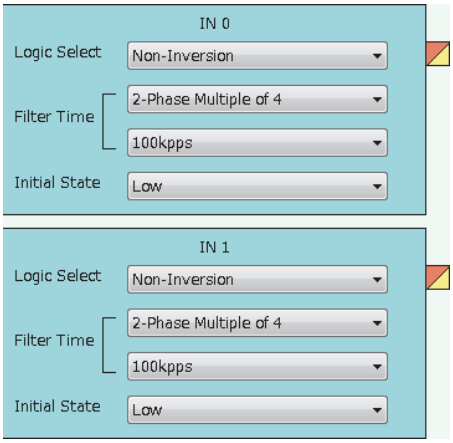
■Link and settings in the hardware logic outline window

1. Arrange a 32-bit unsigned multi function counter block in the hardware logic outline window, and link it to external input blocks.

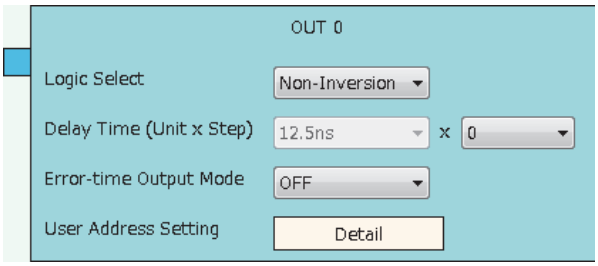
- To perform external outputs according to the counting result, link the multi function counter block to an external output block.



2. Set the external input blocks according to the specifications of external input signals.

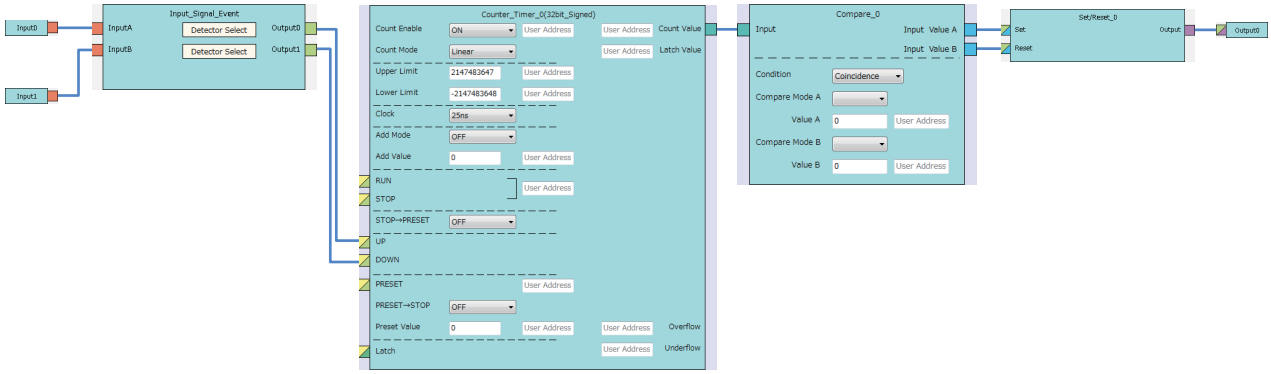


3. To use the external output block, set it according to the specifications of external output signals and desired output timings.

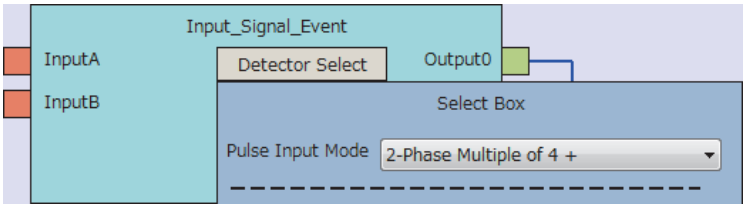


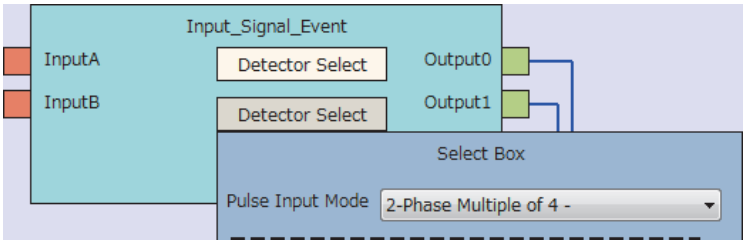
■Link and settings in the multi function counter block detail window

1. Link blocks in the multi function counter block detail window as shown below.

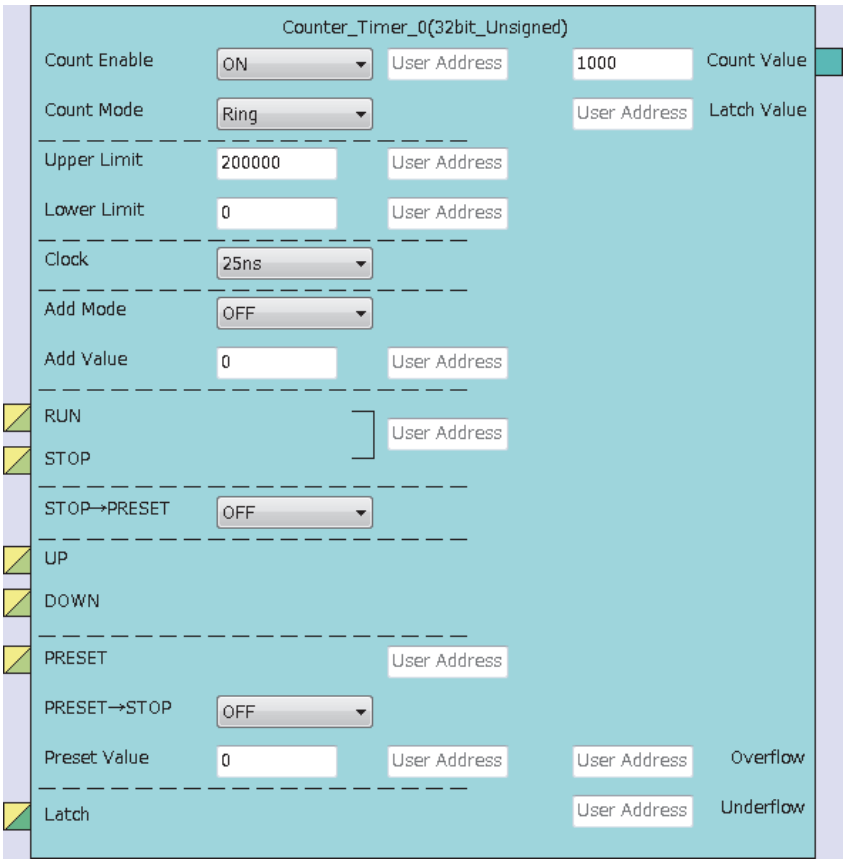


2. Set the setting values of the input signal event detection blocks as shown below.

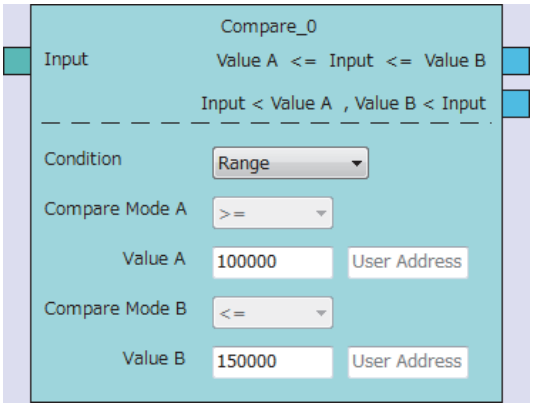




3. Set the setting values of the counter timer block as shown below.



4. Set the setting values of the comparison block as shown below.



■Writing data to the module

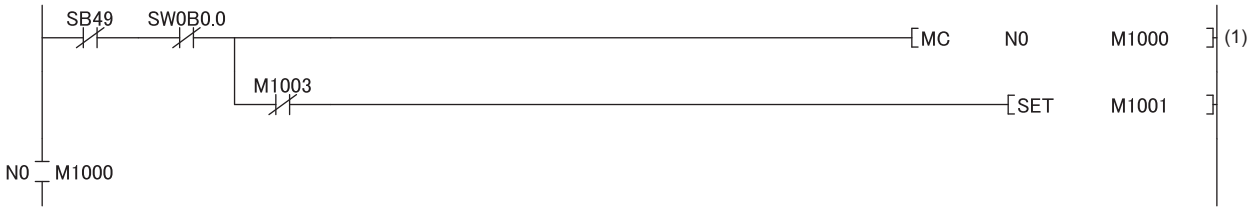
Write the hardware logic to the flexible high-speed I/O control module with the configuration tool.

Program example

The following provides program examples. Write the programs to the CPU module on the master station.

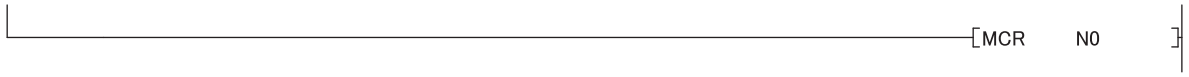
■Common program

A program example to check the data link status of the head module (station number 1)



(1) Check the data link status of the head module (station number 1).

Add the MCR instruction shown below to the last of the program.



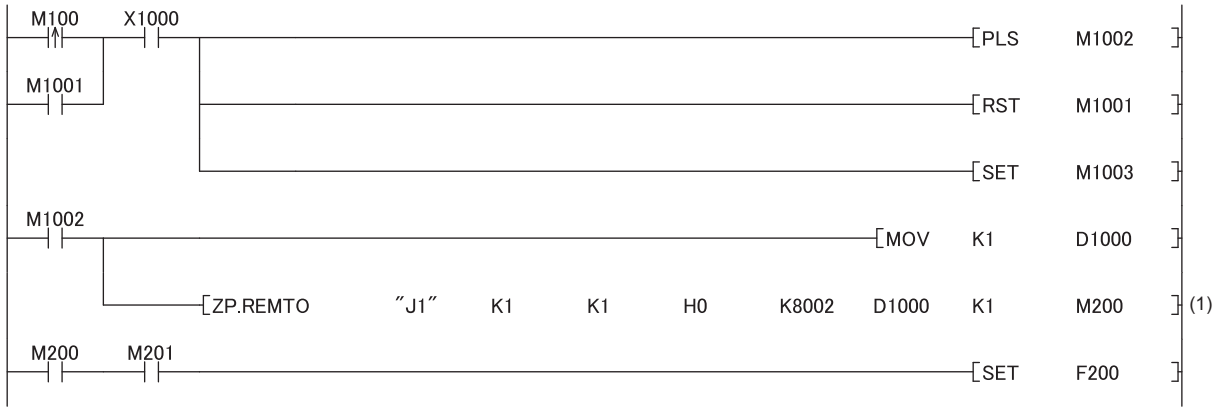
■Program example 1

A program example to turn on Hardware logic control stop signal at disconnection (Y1006)

(1) Turn on Hardware logic control stop signal at disconnection (Y1006).

■Program example 2

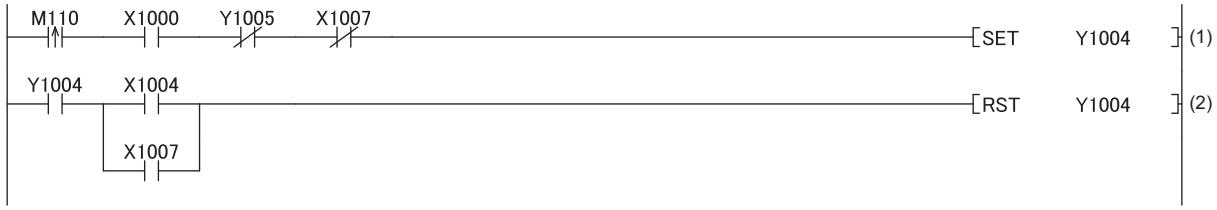
A program example to configure the clear setting of error history



(1) Store Clear the history. (1) in Clear setting of error history (Un\G8002).

■Program example 3

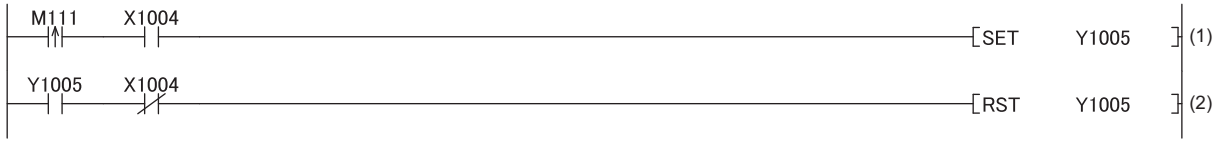
A program example to start the hardware logic control



(1) Turn on Hardware logic control start request (Y1004).
(2) Turn off Hardware logic control start request (Y1004).

■Program example 4

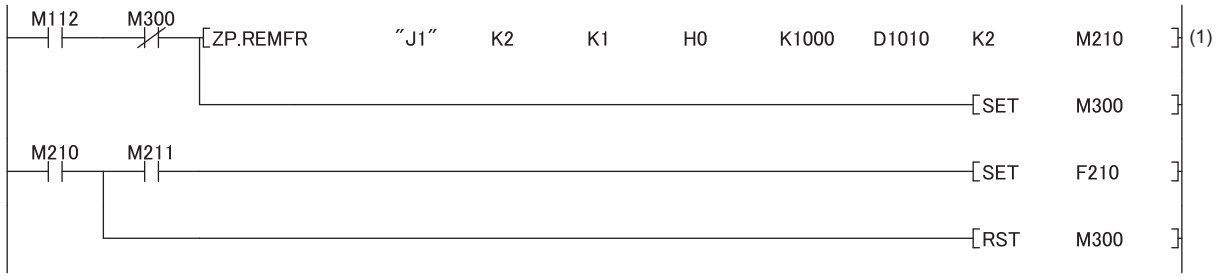
A program example to stop the hardware logic control



(1) Turn on Hardware logic control stop request (Y1005).
(2) Turn off Hardware logic control stop request (Y1005).

■Program example 5

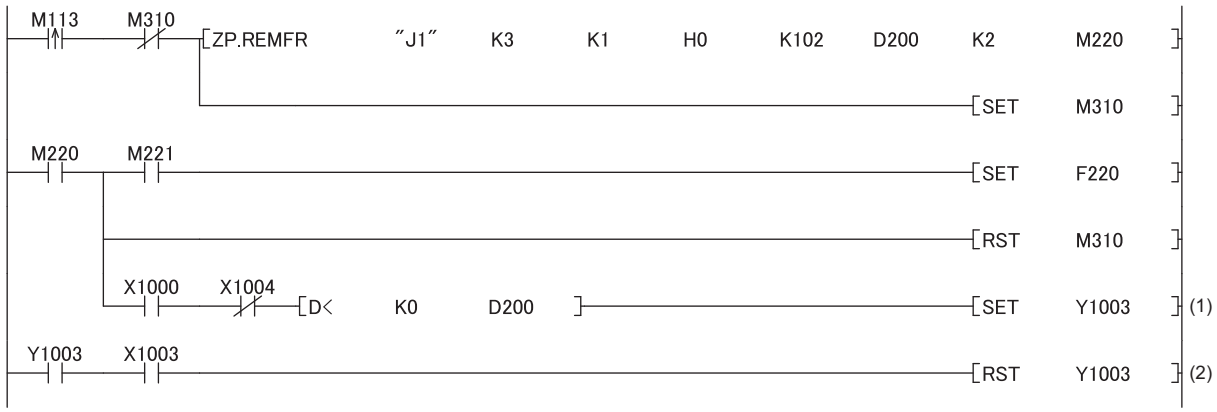
A program example to read the count value



(1) Read the count value.

■Program example 6

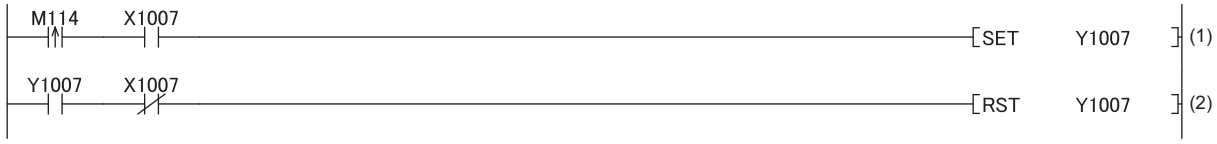
A program example to reset the operating condition settings in a batch



(1) Turn on Operating condition settings batch-reset command (Y1003).
(2) Turn off Operating condition settings batch-reset command (Y1003).

■Program example 7

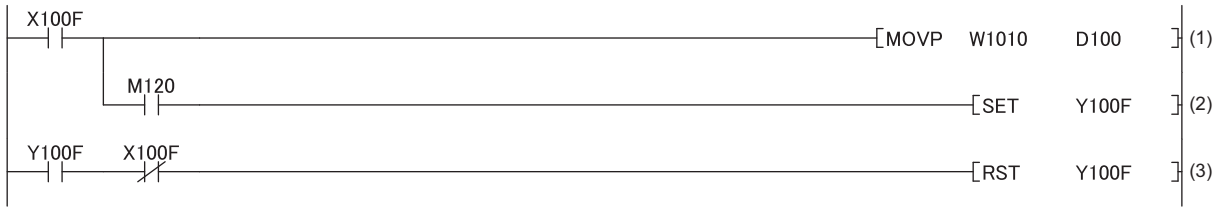
A program example to turn off Hardware logic control stop flag at disconnection (X1007).



(1) Turn on Hardware logic control stop flag clear request at disconnection (Y1007).
(2) Turn off Hardware logic control stop flag clear request at disconnection (Y1007).

■Program example 8

A program example to read the latest error code and reset the error



(1) Read Latest error code (Un\G100).
(2) Turn on Error clear request (Y100F).
(3) Turn off Error clear request (Y100F).

Operations of the flexible high-speed I/O control module when the head module is connected

The following describes the operations of the flexible high-speed I/O control module when the own station is disconnected. The operations differ depending on the combination of the setting of "Hardware logic control valid/invalid during disconnecting" in the switch setting and that of "Error Time Output Mode" in the intelligent function module detailed setting.

"Hardware logic control valid/invalid during disconnecting" is "Valid"

When Hardware logic control stop signal at disconnection (Y6) is off, the hardware logic control is not executed. When Hardware logic control stop signal at disconnection (Y6) is turned off during hardware logic control, the hardware logic control is stopped.

When "Valid" is set for "Hardware logic control valid/invalid during disconnecting", the operation differs depending on the setting of "Error Time Output Mode" as follows.

"Error Time Output Mode"	Operation
Clear	Hardware logic control stop signal at disconnection (Y6) is turned off at the head module disconnection, and thus the hardware logic control stops. The external output during a hardware logic control stop varies depending on "Error-time Output Mode" of the external output block.
Hold	Hardware logic control stop signal at disconnection (Y6) is not turned off at the disconnection, and thus the hardware logic control will continue.

After the head module is returned, turn on Hardware logic control start request (Y4) to restart the hardware logic control.

"Hardware logic control valid/invalid during disconnecting" is "Invalid"

When "Invalid" is set for "Hardware logic control valid/invalid during disconnecting", the operation differs depending on the setting of "Error Time Output Mode" as follows.

"Error Time Output Mode"	Operation
Clear	Even though the head module is disconnected, the hardware logic control continues. However, all the Y device terminals of the hardware logic will be turned to Low because the Y signal is turned off. Note that the operation changes when a created hardware logic includes Y device terminals.
Hold	Even though the head module is disconnected, the hardware logic control continues.

To continue the hardware logic control when the head module is disconnected, set "Invalid" for "Hardware logic control valid/invalid during disconnecting".

If "Hardware logic control valid/invalid during disconnecting" is set to "Invalid", a hardware logic control stop request cannot be issued from a program in the disconnection state.

Operation of the flexible high-speed I/O control module at disconnection

"Hardware logic control valid/invalid during disconnecting"	"Error Time Output Mode"	Operation of the flexible high-speed I/O control module		
		Y signal status	Hardware logic operation	External output status
Valid	Hold	Held	Continued	Output according to the operation result by the hardware logic control
	Clear	Turned off	Stop	Output set in "Error-time Output Mode" of the external output block
Invalid	Hold	Held	Continued	Output according to the operation result by the hardware logic control
	Clear	Turned off	Continued	

For details on the Y signal status of when a head module is connected, refer to the following.

MELSEC-L CC-Link IE Field Network Head Module User's Manual

14 TROUBLESHOOTING

This chapter describes errors that may occur while the flexible high-speed I/O control module is being used, and those troubleshooting.

Checking error codes

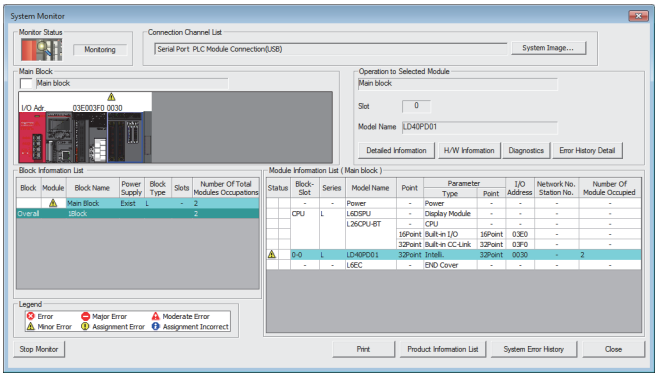
Check the error codes of the errors that occur in the flexible high-speed I/O control module with one of the following methods. Select a method depending on the application or purpose.

☞ Page 231 Checking Error Codes in the Module's Detailed Information Window of GX Works2
☞ Page 232 Checking Error Codes with Latest Error Code (Un\G100)
☞ Page 233 Checking Error Codes with the Module Error Collection Function of GX Works2
☞ Page 208 Checking and Clearing Errors

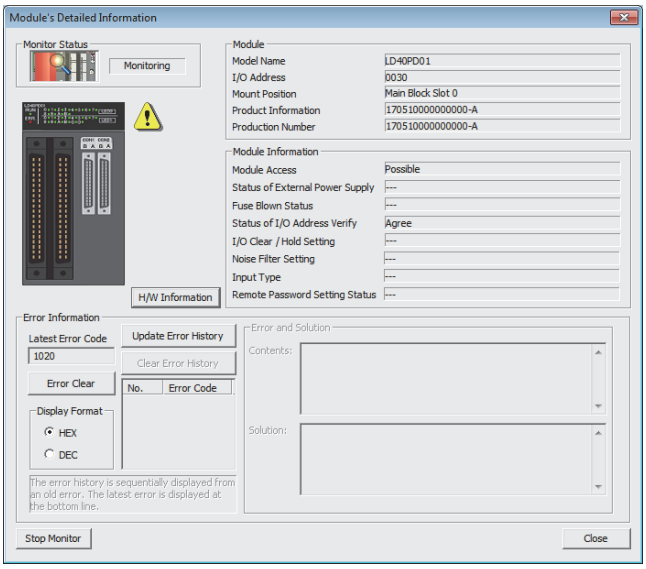
14.1 Checking Error Codes in the Module's Detailed Information Window of GX Works2

This section describes how to check errors in the Module's Detailed Information window of GX Works2.

[Diagnostics] ⇨ [System Monitor]



1. Select the flexible high-speed I/O control module in "Main block" and click the [Detailed Information] button.

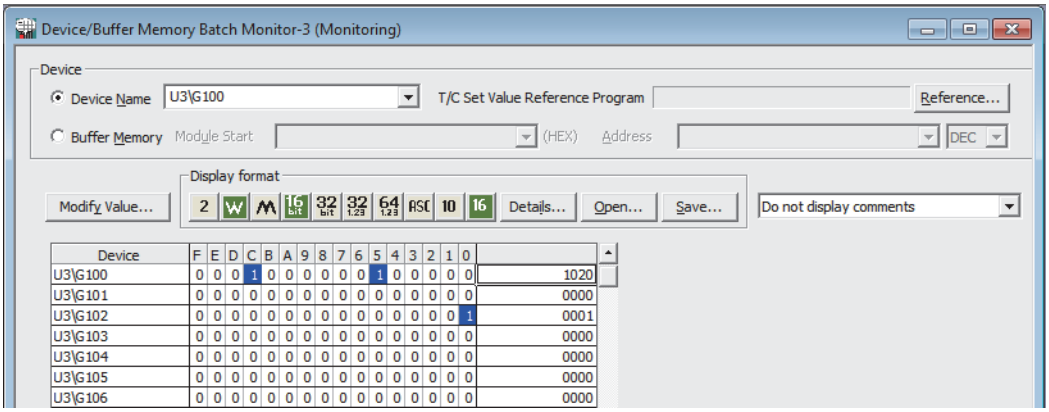


2. The "Module's Detailed Information" window of the flexible high-speed I/O control module is displayed.

14.2 Checking Error Codes with Latest Error Code (Un\G100)

This section describes how to check errors with Latest error code (Un\G100).

[Online] ⇨ [Monitor] ⇨ [Device/Buffer Memory Batch]



Point

If multiple errors have occurred, the latest error code is stored in Latest error code (Un\G100).

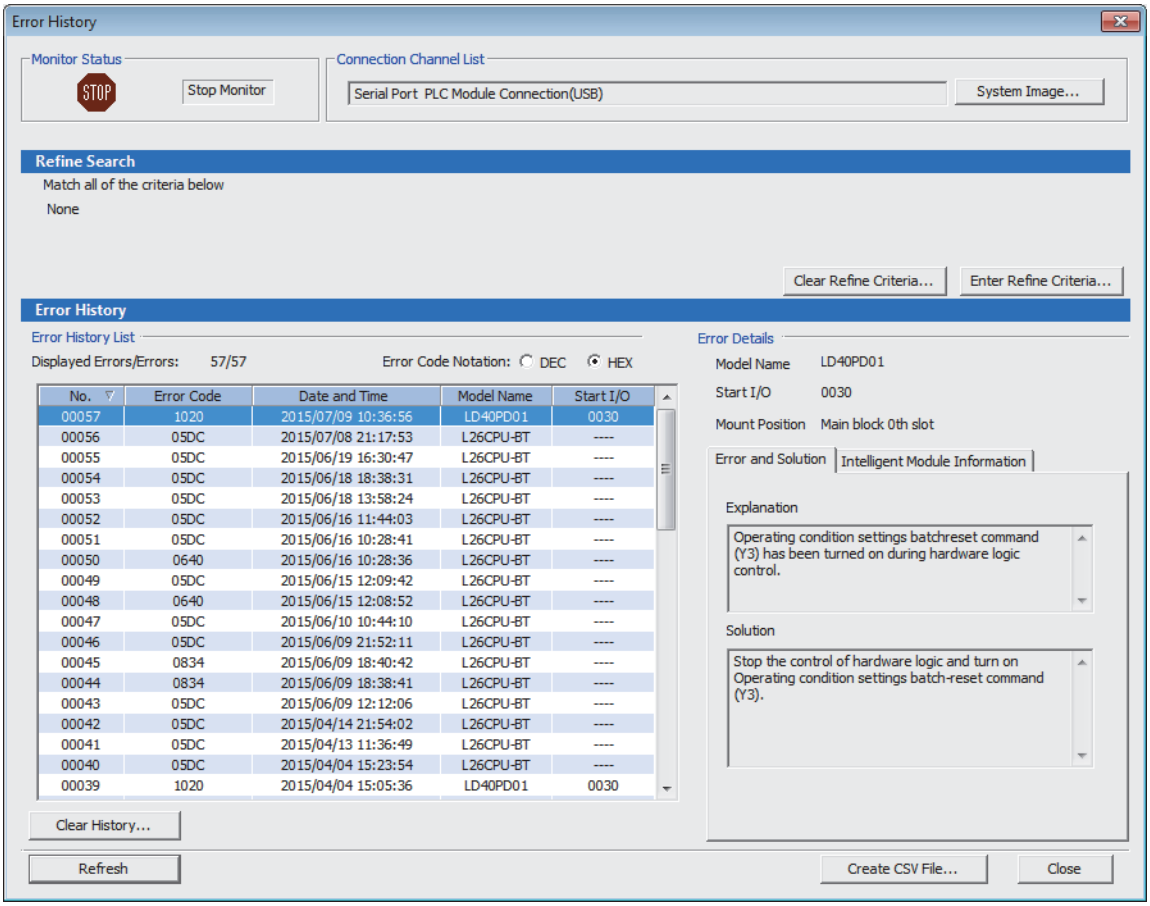
14.3 Checking Error Codes with the Module Error Collection Function of GX Works2

Error codes of the errors that have occurred in the flexible high-speed I/O control module can be saved into the CPU module with the module error collection function of GX Works2. Even after the power of the module is turned off or the CPU module is reset, the error codes are held.

Checking error codes with the module error collection function

Check the error history of the flexible high-speed I/O control module that the CPU module have collected in the "Error History" window.

[Diagnostics] ⇨ [System Monitor] ⇨ [Error History Detail] button



Errors to be collected

Errors described in the following section are notified to the CPU module.

☞ Page 238 List of Error Codes

14.4 Troubleshooting with LEDs

RUN LED is flashing or turns off

RUN LED is flashing

Check item	Action
Is the simulation being executed?	Check that the RUN LED turns on after the completion of the simulation.

RUN LED turns off

Check item	Action
Has the power been supplied?	Check if the voltage supplied to the power supply module is within the rated range.
Is the capacity of the power supply module sufficient?	Calculate the total current consumption of the connected modules including the CPU module, input/output modules, and intelligent function module to check if the power capacity is sufficient.
Has the module been properly connected?	Check if the module has been properly connected.
Other than the above	Reset the CPU module and check if the RUN LED turns on. If the RUN LED still does not turn on, the possible cause is a failure of the module. Please consult your local Mitsubishi representative.

ERR. LED turns on

Check item	Action
Is there an error?	Check Latest error code (Un\G100) and take actions described in the following section. ☞ Page 238 List of Error Codes

14.5 Troubleshooting by Symptom

Inputs from external devices are not performed

Check item	Action
Is the LED0 on?	Check the external wiring and make necessary corrections.
Is the control of the hardware logic working?	When Hardware logic control flag (X4) is off, turn on Hardware logic control start request (Y4) to start the hardware logic control.
Are the block layout and links between blocks in the hardware logic correct?	Check the block layout and links between blocks in the hardware logic and make necessary corrections.

Incorrect inputs from external devices are performed

Check item		Action
Measures to reduce noise	Is the filter time setting of external input blocks correct?	Set the filter time of the external input blocks longer.
	Have twisted pair shielded cables been used for the pulse input cables?	Use twisted pair shielded cables for the pulse input cables.
	Have measures to reduce noise been taken in the control panel or for adjacent devices?	Take measures to reduce noise such as attaching a CR surge suppressor to the magnet switch or other device.
	Is there a sufficient distance between the high voltage device and the pulse input cables?	Wire the pulse input cables alone when placing them in a duct, and keep a distance of 150mm or more from the power cables in the control panel.
	Is the module affected by noise through the grounding area?	Separate the grounding cable of the flexible high-speed I/O control module from the grounding area.
	Are the power cables and I/O cables bundled together?	Do not bundle the power cables and I/O cables together.
	Is the external wiring connected to unused terminals?	Do not connect the external wiring to unused terminals.

Outputs to external devices are not performed

Check item	Action
Is the LED1 on?	Check the block layout and links between blocks in the hardware logic and make necessary corrections.
Is the external wiring correct?	Check the external wiring and make necessary corrections.
Is the control of the hardware logic working?	When Hardware logic control flag (X4) is off, turn on Hardware logic control start request (Y4) to start the hardware logic control.
Are the block layout and links between blocks in the hardware logic correct?	Check the block layout and links between blocks in the hardware logic and make necessary corrections.

The hardware logic does not function

Check item	Action
Is the control of the hardware logic working?	When Hardware logic control flag (X4) is off, turn on Hardware logic control start request (Y4) to start the hardware logic control.
Are the block layout and links between blocks in the hardware logic correct?	Check the block layout and links between blocks in the hardware logic and make necessary corrections.
Is the CPU module indicating an error?	If the CPU module is in an error status, refer to the troubleshooting in the user's manual for the CPU module used and take corrective actions to restore normal operation of the CPU module.

A multi function counter does not start counting or does not count properly

The module does not start counting

Check item	Action
Has Count Enable been set to ON?	Set Count Enable to ON using a program or the configuration tool.
Is any LED of the CPU module indicating an error?	If the LED indicates an error, refer to the troubleshooting in the manual for the CPU module used and take corrective actions to restore normal operation of the CPU module.
Is the external wiring for ΦA and ΦB correct?	Check the external wiring and make necessary corrections.
Is the control of the hardware logic working?	When Hardware logic control flag (X4) is off, turn on Hardware logic control start request (Y4) to start the hardware logic control.
Are the block layout and links between blocks in the hardware logic correct?	Check the block layout and links between blocks in the hardware logic and make necessary corrections.

The module does not count properly

Check item	Action
Are the current value or other values read in increments of one word (16 bits) using a program when 32-bit counter timer blocks are used?	Read the values of two words (32 bits) in a batch.
Was the preset function performed within the count range of a counter?	Reset the preset value within the count range and perform the preset function again.
Is the filter time setting of external input blocks correct?	Check the filter time setting and make necessary corrections.
When the same pulse is input to the multi function counter blocks that have the same links, is the same value counted?	If the count values are different, the possible cause is a failure of the module. Please consult your local Mitsubishi representative.
Does the input pulse wave satisfy the performance specifications?	Observe and check the pulse wave with a synchroscope. If the input pulse does not satisfy the performance specifications, input pulses that satisfy the performance specifications.
Is the external wiring with the SSI encoder correct?	Check the external wiring. (☞ Page 55 Example of external wiring with the SSI encoder (serial communication))
Is the setting value of the SSI encoder block correct?	Check and correct the value according to the SSI encoder to be connected.
Is the cable length within the range of the maximum cable length?	Check the cable length and size. (☞ Page 55 Example of external wiring with the SSI encoder (serial communication)) Or slow the SSI transmission speed.
Are shielded twisted pair cables used?	Use shielded twisted pair cables.
Does noise affect anything?	Take measures to reduce noise such as attaching a surge suppressor to the magnet switch.
Is there a sufficient distance between the high voltage device and the signal wires?	Wire the signal wires alone and keep them 150mm or more away from power cables.

■Pulse shaping method

As one of measures against external noise or waveform distortion, the following describes the shaping method of a pulse waveform with dummy resistors.

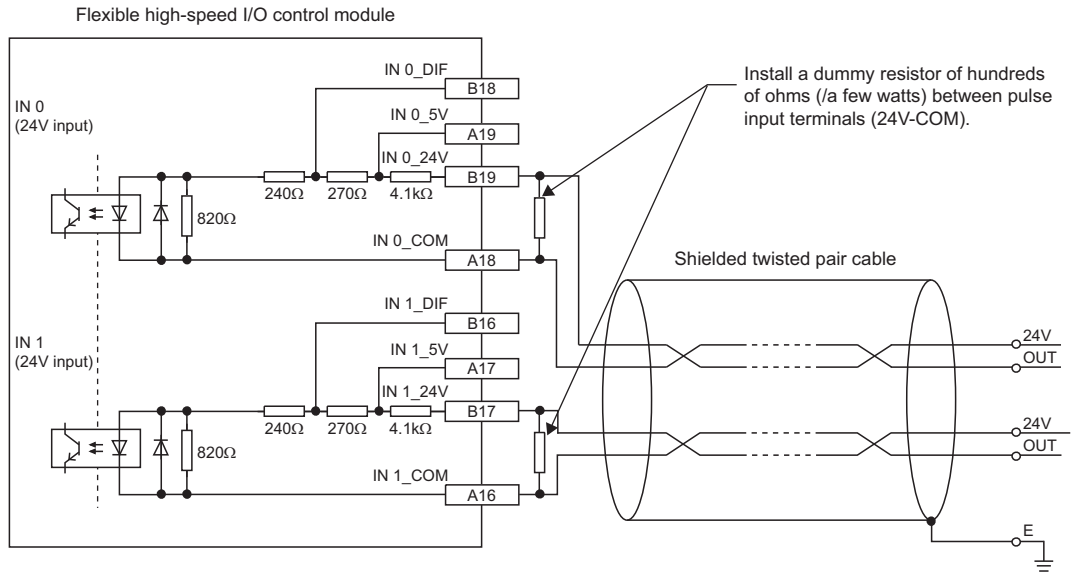
An effective method for pulse shaping is to apply dummy resistors of several hundreds ohms (/several watts) across pulse input terminals connected to an encoder to increase a load current through the cables. This method becomes more effective as the load current value increases.

With this shaping method, the following effects can be obtained.

- When the wiring distance between an encoder and the flexible high-speed I/O control module is long, this shaping method improves the waveform distortion and the pulse waveform becomes stable.
- When the pulse waveform is unstable due to noise such as external noise, this shaping method stabilizes the pulse waveform and the noise effects can be reduced.

Ex.

The following figure shows a connection example of dummy resistors at 24VDC.



The following example describes how to select a dummy resistor (how to calculate a resistance constant and rated power of a dummy resistor).

Target	Calculation method
Resistance constant of a dummy resistor (at 24VDC input)	Calculate a resistance constant (R) as follows. • R = V ÷ I = 24V ÷ 35mA = 680Ω
Rated power of a dummy resistor (at 24VDC input)	Calculate the power (P1) as follows. • P1 = V × I = 24V × 35mA = 0.84W (Approx. 1W) Calculate the power (P2) including margins from the power (P1). • P2 = P1 × 2 = 0.84 × 2 = 1.68W (Approx. 2W)

As a result of the above calculations, apply dummy resistors of 680Ω (/2W) across pulse input terminals in this case.

Interrupt requests are not properly sent to the CPU module

Check item	Action
Is a link to the SI device terminal in the hardware logic correct?	Check the block layout and links between blocks in the hardware logic and make necessary corrections.
Is the coincidence detection disabled because the addition mode has been applied?	To use the coincidence detection interrupt and addition mode together, preset the value used for the coincidence detection.
Is the intelligent function module interrupt pointer setting of the PLC parameter correct?	Review the intelligent function module interrupt pointer setting.

14.6 List of Error Codes

This section lists the codes of errors that may occur in the use of the I/O control module.

The error codes are stored in Latest error code (Un\G100) and also reported to the CPU module.

The ☐ in the error code indicates the number of the multi function counter block where an error has occurred.

Error code (hexadecimal)	Error name	Description and cause	Operation at the error	Action
3001H	Hardware error	A hardware error has occurred.	The control of hardware logic stops.	Turn off and on the power, or reset the CPU module. If the error occurs again, the possible cause is a failure of the module. Please consult your local Mitsubishi representative.
1060H	Flash ROM data error	The setting data in the flash ROM are faulty.	The control can be started with non-wired hardware logic.	Write the setting data again with a configuration tool. Take measures to reduce noise with a shielded cable for connection. If the error occurs again, the possible cause is a failure of the module. Please consult your local Mitsubishi representative.
1080H	Number of writes to a flash ROM over error	The number of writes to a flash ROM has exceeded 10000 times.	The control of hardware logic can be started.	Any further writes to a flash ROM may not be reflected correctly.
100☐H	Multi function counter block ☐ overflow error	A count value has exceeded the upper limit value when 32-bit multi function counter block is set to linear counter mode.	The count operation stops for the corresponding multi function counter block.	Perform the preset function to the corresponding multi function counter block.
101☐H	Multi function counter block ☐ underflow error	A count value has fallen below the lower limit value when 32-bit multi function counter block is set to linear counter mode.	The count operation stops for the corresponding multi function counter block.	Perform the preset function to the corresponding multi function counter block.
1020H	Reset error during hardware logic control	Operating condition settings batch-reset command (Y3) has been turned on during hardware logic control.	The control of hardware logic continues.	Stop the control of hardware logic and turn on Operating condition settings batch-reset command (Y3).
1040H	Reset error without any data writes to a flash ROM	Operating condition settings batch-reset command (Y3) has been turned on while any setting data has not been written to a flash ROM.	The operating condition settings batch-reset for hardware logic is not performed.	Set operating conditions in a flash ROM and turn on Operating condition settings batch-reset command (Y3).
109☐H	SSI encoder block ☐ DATA signal wire reverse error	The positive and negative of the DATA signal wire are reversely connected.	Position data from the encoder cannot be received properly.	Check the external wiring.
10A☐H	SSI encoder block ☐ DATA signal error	The DATA signal input state is Low at the start of data transmission, or is High just after the transmission is completed.		Check the cabling, shielding, SSI transmission speed, cable length, and SSI code length. In addition, consider the possibility of noise effects.
10B☐H	SSI encoder block ☐ parity error	A parity error has occurred.		Check the external wiring and settings of the SSI encoder block.

14.7 Checking the Status of the Flexible High-speed I/O Control Module with System Monitor

Select "H/W Information" of the flexible high-speed I/O control module in the system monitor of GX Works2 and check the LED status and the setting status of the switch setting.

H/W LED Information

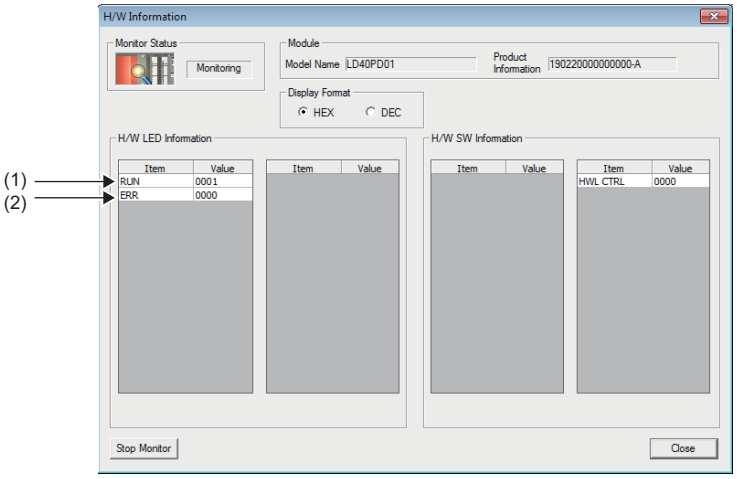
The LED on/off status is displayed.

No.	LED name	On/off status
(1)	RUN LED	0000H: The LED is off. 0001H: The LED is on. Alternately displayed 0000H and 0001H: The LED flashes. (As the state in communication is displayed, 0000H and 0001H are not always displayed for the same period of time.)
(2)	ERR. LED	

H/W SW Information

The setting status of the switch setting is displayed.

- When "Invalid" is set for "Hardware logic control valid/invalid during disconnecting", 0000 is displayed in "HWL CTRL".
- When "Valid" is set for "Hardware logic control valid/invalid during disconnecting", 0001 is displayed in "HWL CTRL".



APPENDICES

Appendix 1 Details of I/O Signals

This section describes the details on the I/O signals of the flexible high-speed I/O control module to the CPU module.
The I/O numbers (X/Y) in this section apply when the start I/O number of the flexible high-speed I/O control module is set to "0".

Input signal

Module READY (X0)

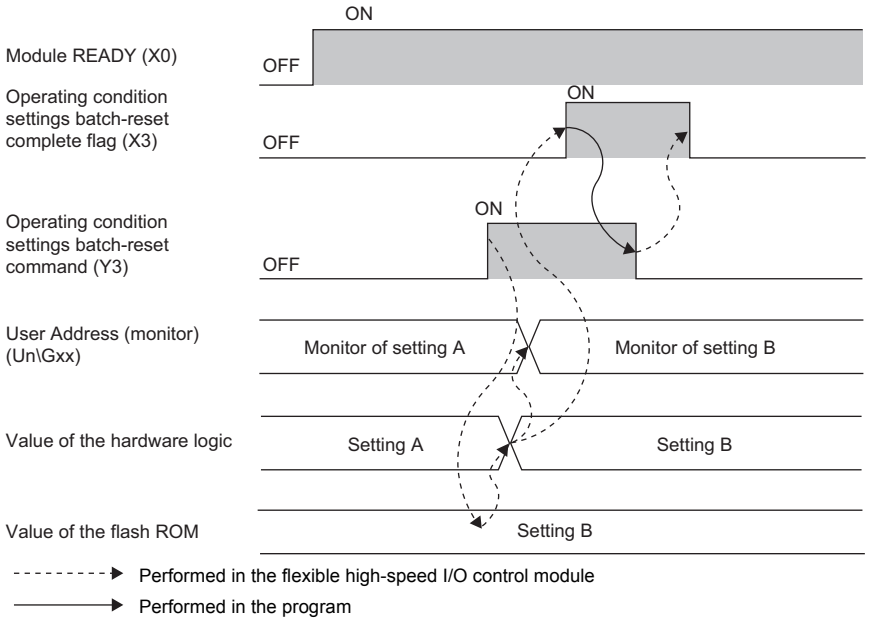
This signal turns on when the control is ready after the CPU module is powered on or is reset.
In the following case, Module READY (X0) turns off.

- When a watchdog timer error has occurred in the flexible high-speed I/O control module (The control is not performed.)

Operating condition settings batch-reset complete flag (X3)

When the setting of the execution memory is reset with the value stored in the flash ROM in the flexible high-speed I/O control module, this signal is used as an interlock to turn on or off Operating condition settings batch-reset command (Y3).

- When Operating condition settings batch-reset command (Y3) is turned on, this signal turns on. When the reset of the hardware logic setting is completed with an error, this signal also turns on.
- When Operating condition settings batch-reset command (Y3) is turned off, this signal turns off.



Hardware logic control flag (X4)

While the hardware logic operates, Hardware logic control flag (X4) is on.

■ON of Hardware logic control flag (X4)

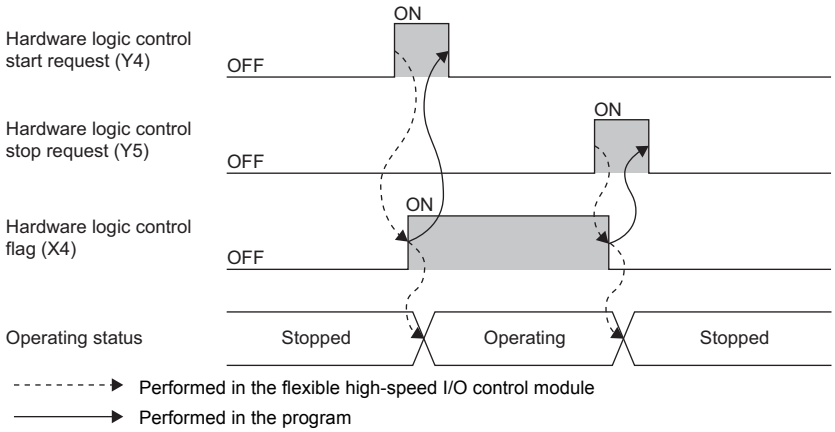
In the following status, this signal turns on.

- When Hardware logic control start request (Y4) is turned on
- When the hardware logic control start request is issued with the configuration tool

■OFF of Hardware logic control flag (X4)

In the following status, this signal turns off.

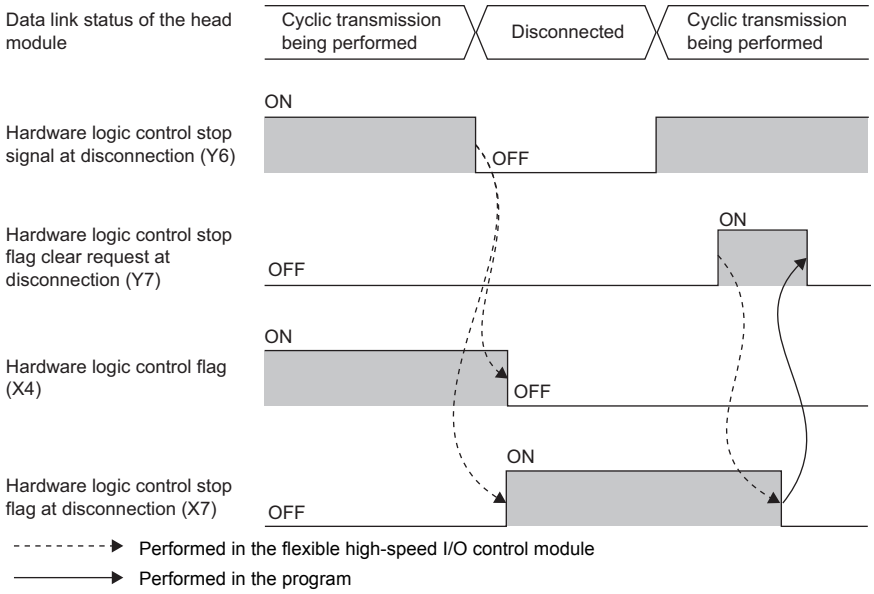
- When the power supply is turned on
- When the CPU module is reset
- When Hardware logic control stop request (Y5) is turned on (If Hardware logic control start request (Y4) and Hardware logic control stop request (Y5) are turned on at the same time, Hardware logic control stop request (Y5) takes priority and Hardware logic control flag (X4) does not turn on.)
- When the hardware logic control stop request is issued with the configuration tool
- From when the "Write to Module (execution memory)" or "Write to Module (execution + flash ROM)" is executed with the configuration tool until the hardware logic control restarts
- When the simulation is executed with the configuration tool
- When Hardware logic control stop flag at disconnection (X7) turns on
- When a stop error occurs in the CPU module



A

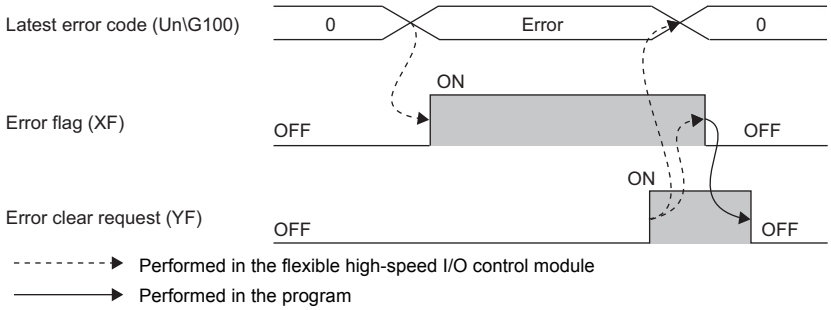
Hardware logic control stop flag at disconnection (X7)

- This signal is enabled when "Valid" is set for "Hardware logic control valid/invalid during disconnecting" in "Switch Setting".
- When Hardware logic control stop signal at disconnection (Y6) is turned off during hardware logic control, the hardware logic control is stopped and this signal turns on. When Hardware logic control stop signal at disconnection (Y6) is turned off while the hardware logic control is stopped, this signal does not turn on.
- When Hardware logic control stop flag clear request at disconnection (Y7) is turned on, this signal turns off.
- When Hardware logic control start request (Y4) is turned on while this signal is on, the request is ignored. Turn off this signal by turning on Hardware logic control stop flag clear request at disconnection (Y7). Then, turn on Hardware logic control start request (Y4).



Error flag (XF)

This signal turns on when an error occurs.



■OFF of Error flag (XF)

When the error cause has been eliminated and Error clear request (YF) is turned on and off, the following flag and error code are cleared.

- Error flag (XF)
- Latest error code (Un\G100)

When Clear setting of error history (Un\G8002) has been set to Clear the history. (1), Error history No. ☐ (Un\G8010 to Un\G8169) is also cleared.

IN 0 to IN B (X10 to X1B)

Set input values to external input blocks ("IN 0" to "IN B").

A

Output signal

Operating condition settings batch-reset command (Y3)

This signal is used to reset the setting of the execution memory with the value stored in the flash ROM in the flexible high-speed I/O control module. When this signal is turned on, the values in the execution memory and Hardware logic area (Un\G1000 to Un\G1099) are reset to the values stored in the flash ROM.

For the timing of turning on and off this signal, refer to the following.

☞ Page 240 Operating condition settings batch-reset complete flag (X3)

■Precautions

- Turn on this signal while the hardware logic stops. When this signal is turned on in the operation of the hardware logic, the reset error during hardware logic control (error code: 1020H) occurs. The setting of the hardware logic is not reset and the operation of the hardware logic continues.
- When no data has been written to the flash ROM and this signal is turned on, the reset error without any data writes to a flash ROM (error code: 1040H) occurs.

Hardware logic control start request (Y4)

This signal is used to start the operation of the hardware logic. Because the operation of the hardware logic is stopped when the power supply is turned on, this signal needs to be turned on to start the operation.

For the timing of turning on and off this signal, refer to the following.

☞ Page 241 Hardware logic control flag (X4)

Hardware logic control stop request (Y5)

This signal is used to stop the operation of the hardware logic. When the operation of the hardware logic is stopped by turning on this signal, the count value is reset. To stop only the count operation without resetting the count value, set "OFF" for "Count Enable" of the counter timer block.

For the timing of turning on and off this signal, refer to the following.

☞ Page 241 Hardware logic control flag (X4)

Hardware logic control stop signal at disconnection (Y6)

This signal is enabled when "Valid" is set for "Hardware logic control valid/invalid during disconnecting" in "Switch Setting". Do not set "Valid" for "Hardware logic control valid/invalid during disconnecting" in "Switch Setting" when a head module is not connected. If "Valid" is set, this signal needs to be on at a hardware logic control start.

■Starting the hardware logic control

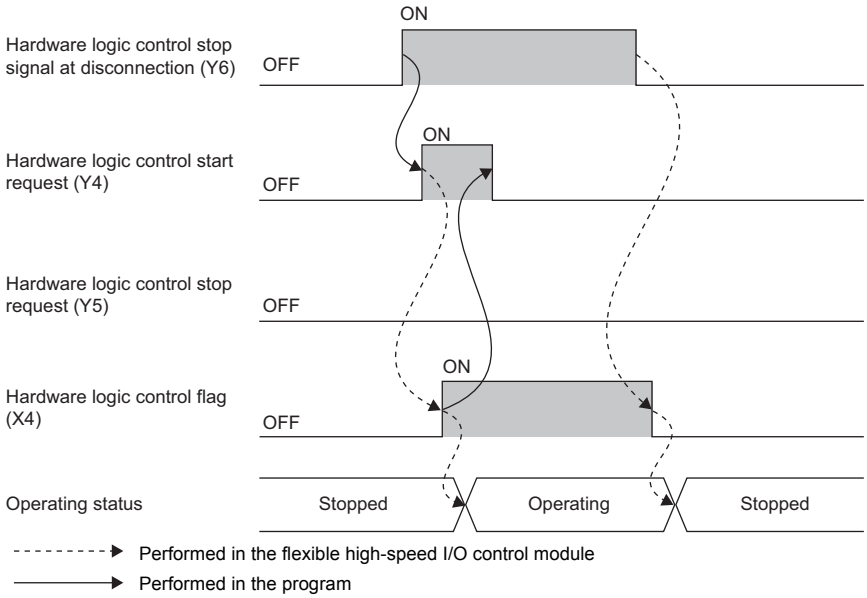
When "Hardware logic control stop enable/disable setting during disconnecting" is set to "Valid" and both of the following conditions are satisfied, the hardware logic control is started.

- When this signal is on
- When Hardware logic control start request (Y4) is turned on

■Stopping the hardware logic control

When any of the following conditions is satisfied, the hardware logic control is stopped.

- When this signal is turned off
- When Hardware logic control stop request (Y5) is turned off while this signal is on



Hardware logic control stop flag clear request at disconnection (Y7)

This signal is enabled when "Valid" is set for "Hardware logic control valid/invalid during disconnecting" in "Switch Setting". Turn on and off this signal to turn off Hardware logic control stop flag at disconnection (X7).

For the timing of turning on and off this signal, refer to the following.

☞ Page 242 Hardware logic control stop flag at disconnection (X7)

Error clear request (YF)

To clear Error flag (XF), Latest error code (Un\G100), and Error history No.☐ (Un\G8010 to Un\G8169), turn on and off this signal.

For the timing of turning on and off this signal, refer to the following.

☞ Page 243 Error flag (XF)

General command 0 to General command F (Y10 to Y1F)

Signals in the hardware logic can be controlled from a program.

Turning on or off General command 0 to General command F (Y10 to Y1F) outputs the internal signals of the hardware logic in High or Low state from Y device terminals.

For details on the Y device terminals, refer to the following.

☞ Page 109 Y device terminal

Appendix 2 Details of Buffer Memory Areas

This chapter describes the details on the buffer memory areas of the flexible high-speed I/O control module.

Latest error code (Un\G100)

This area stores the latest error code detected in the flexible high-speed I/O control module.

For details on the error codes, refer to the following.

☞ Page 238 List of Error Codes

■How to clear an error

Turn on and off Error clear request (YF).

Cumulative number of write accesses to a flash ROM (Un\G102, Un\G103)

This area stores the cumulative number of writes to a flash ROM. When a hardware logic is written to the flash ROM of the flexible high-speed I/O control module with the setting tool, the stored value is increased by one.

When the number of writes exceeds the allowable number of writes to the flash ROM (10000 times), the written hardware logic data cannot be assured. To decrease the number of writes to the flash ROM, write hardware logics to the execution memory for adjustment. After the adjustment is completed, write the hardware logic to the flash ROM.

SSI receive data monitor 0 (Un\G110, Un\G111)

Out of the data frames received from SSI encoder 0, the information for the number of bits specified with "Data Frame Length" is stored in this area at the communication cycle of the SSI encoder.

The parity bit is not reflected to this area.

When the data frame length is smaller than 32 bits, the least significant bit of the data frame is stored in the bit 0 of Un\G110.

For details, refer to the following.

☞ Page 114 SSI encoder block

SSI receive data monitor 1 (Un\G114, Un\G115)

Out of the data frames received from SSI encoder 1, the information for the number of bits specified with "Data Frame Length" is stored in this area at the communication cycle of the SSI encoder.

The data to be stored in this area is the same as the one of SSI receive data monitor 0 (Un\G110, Un\G111).

Hardware logic area (Un\G1000 to Un\G1099)

The monitor items and setting items of the hardware logic can be assigned to buffer memory addresses.

There are two types of areas for the buffer memory areas: High speed area and low speed area. For each area, the addresses are assigned as follows.

Area	Buffer memory address	Description
High speed area	Un\G1000 to Un\G1029	• The items of the input terminals and parameters that are assigned to these areas are written in a high-speed period (100μs). • The items of the monitors assigned to these areas are read in a high-speed period (100μs).
Low speed area	Un\G1030 to Un\G1099	• The items of the input terminals and parameters that are assigned to these areas are written in a low-speed period (1ms). • The items of the monitors assigned to these areas are read in a low-speed period (1ms).

These items are also read or written when an interrupt signal is sent to the CPU module.

■Assignable monitor items and setting items

The following items can be assigned to these areas.

Block	Type	Variable name	R/W*1	Setting value/ Stored value	Description
Counter timer block	Input terminal	RUN /STOP	R/W	0	Both the "RUN" and "STOP" terminals turn to Low.
				1	The "RUN" terminal turns to High and the "STOP" terminal turns to Low.
				2	The "RUN" terminal turns to Low and the "STOP" terminal turns to High.
				3	Both the "RUN" and "STOP" terminals turn to High.
		PRESET	R/W	0	The "PRESET" terminal turns to Low.
				1	The "PRESET" terminal turns to High.
	Parameter	Count Enable	R/W	0	Count Enable is off.
				1	Count Enable is on.
		Upper Limit*2	R/W	*3	Set the upper limit value.
		Lower Limit*2	R/W	*3	Set the lower limit value.
		Add Value*2	R/W	*3	Set the addition value.
		Preset Value*2	R/W	*3	Set the preset value.
	Monitor	Count Value*2	R	*3	A count value is stored.
		Latch Value*2	R	*3	A latch value is stored.
		Overflow*4	R	0	No overflow occurs.
				1	An overflow has been occurred.
		Underflow*4	R	0	No underflow occurs.
				1	An underflow has been occurred.
Cam switch block	Parameter	Step No.0 ⋮ Step No.15*2	R/W	*3	Step No. 0 ⋮ Step No. 15
Comparison block	Parameter	Compare Value	R/W	*3	Value compared with a count value of the counter timer
External output block	Parameter	Enable Forced Output	R/W	0	The forced output is disabled.
				1	The forced output is enabled.
	Parameter	Forced Output	R/W	0	The forced output status of the external terminal is off (0: OFF).
				1	The forced output status of the external terminal is on (1: ON).
	Monitor	External terminal monitor	R	0	The output status (0: OFF) of the external output terminal is stored.
				1	The output status (1: ON) of the external output terminal is stored.

*1 The output values of each block in the hardware logic are "R" and the input values of each block in the hardware logic are "R/W".

*2 Assign a parameter of two words (32 bits) to an even address.

*3 The setting and storage ranges are determined depending on the type of a counter timer block.

*4 The item cannot be assigned in a 16-bit counter timer block.

Latest address of error history (Un\G8000)

This area stores the buffer memory address which has the latest error code among the addresses of Error history No.☐ (Un\G8010 to Un\G8169).

Clear setting of error history (Un\G8002)

Set whether to clear an error history when Error clear request (YF) is turned on.

Clear setting of error history	Setting value
Do not clear the history.	0
Clear the history.	1

■Enabling the setting

The setting is enabled immediately after a value is set in the buffer memory area.

■Default value

The default value is Do not clear the history. (0).

Error history No.☐ (Un\G8010 to Un\G8169)

This area stores up to 16 errors that have occurred in the module.

For details on the error history function, refer to the following.

☞ Page 58 Error History Function

	b15 to b8	b7 to b0
Un\G8010	Error code	
Un\G8011	First two digits of the year	Last two digits of the year
Un\G8012	Month	Day
Un\G8013	Hour	Minute
Un\G8014	Second	Day of the week
Un\G8015 to Un\G8019	System area	

Item	Description	Storage example*1
First two digits of the year/last two digits of the year	Stored as a BCD code.	2015H
Month/day		0424H
Hour/minute		1035H
Second		40H
Day of the week	For each day of the week, one of the following values is stored as a BCD code. Sunday: 0H, Monday: 1H, Tuesday: 2H, Wednesday: 3H, Thursday: 4H, Friday: 5H, Saturday: 6H	5H

*1 Value for when an error occurred at 10:35:40 on Friday, April 24th, 2015

RUN LED status monitor (Un\G8170)

This area stores the current status of the RUN LED.

For details on the RUN LED, refer to the following.

☞ Page 21 PART NAMES

RUN LED status	Stored value	Description
Off	0	The RUN LED turns off.
On	1	The RUN LED turns on.
Flashing	2	The RUN LED is flashing.

ERR LED status monitor (Un\G8171)

This area stores the current status of the ERR. LED.

For details on the ERR. LED, refer to the following.

☞ Page 21 PART NAMES

ERR. LED status	Stored value	Description
Off	0	The ERR. LED turns off.
On	1	The ERR. LED turns on.

Appendix 3 How to Get the Configuration Tool

For the configuration tool, please consult your local Mitsubishi representative.

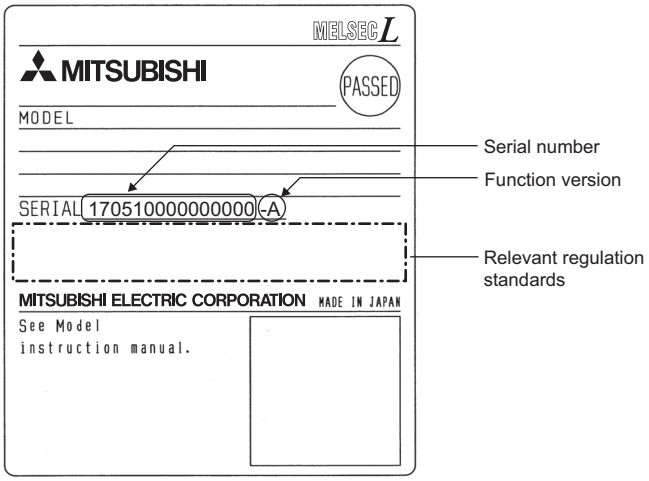
Appendix 4 Checking Serial Number and Function Version

The serial number and function version of the module can be checked with one of the following methods.

- Rating plate
- Front surface of the module
- System monitor of the programming tool

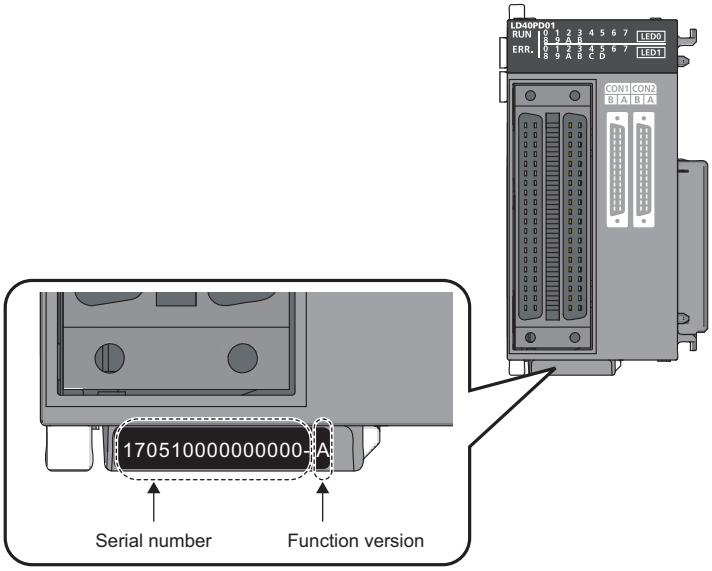
Checking on the rating plate

The rating plate is on the side surface of the module.



Checking on the front surface of the module

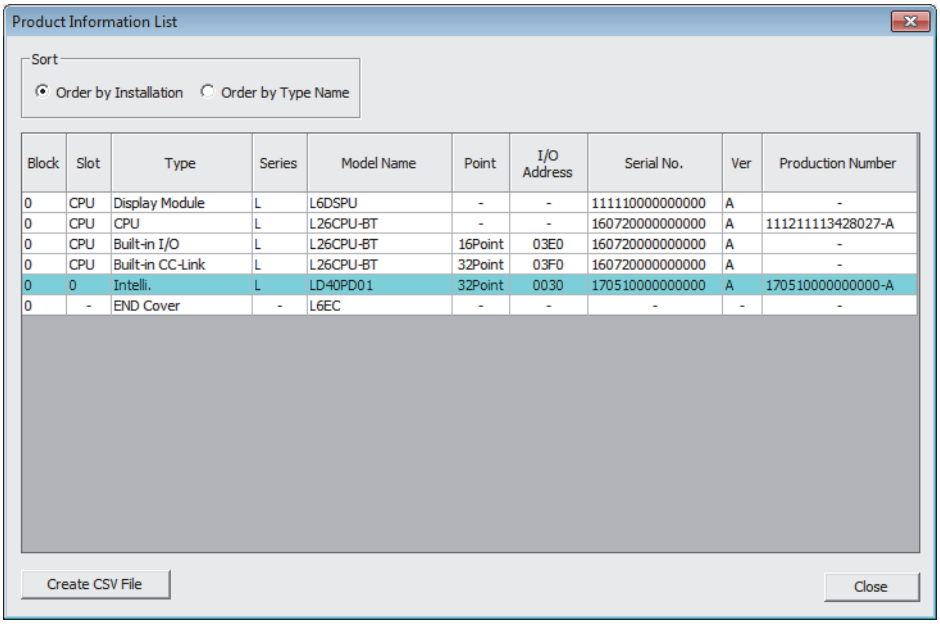
The following figure shows the serial number printed on the rating plate on the front surface (bottom part) of the module.



Checking with the system monitor

Check the serial number and function version in the "Product Information List" window.

[Diagnostics] ⇨ [System Monitor] ⇨ [Product Information List] button



■Product number display

"Production Number" shows the serial number (product number) printed on the rating plate.

By checking this item, users can check the serial number (product number) without visually checking the module.

Point

There are some cases in which the serial number printed on the rating plate and the front surface of the module and the one displayed in the "Product Information List" window of the programming tool are different.

- The serial number printed on the rating plate and the front surface of the module indicates the management information of the product.
- The serial number displayed in the "Product Information List" window of the programming tool indicates the function information of the product. The function information is updated when a function is added.

A

Appendix 5 Added and Changed Functions

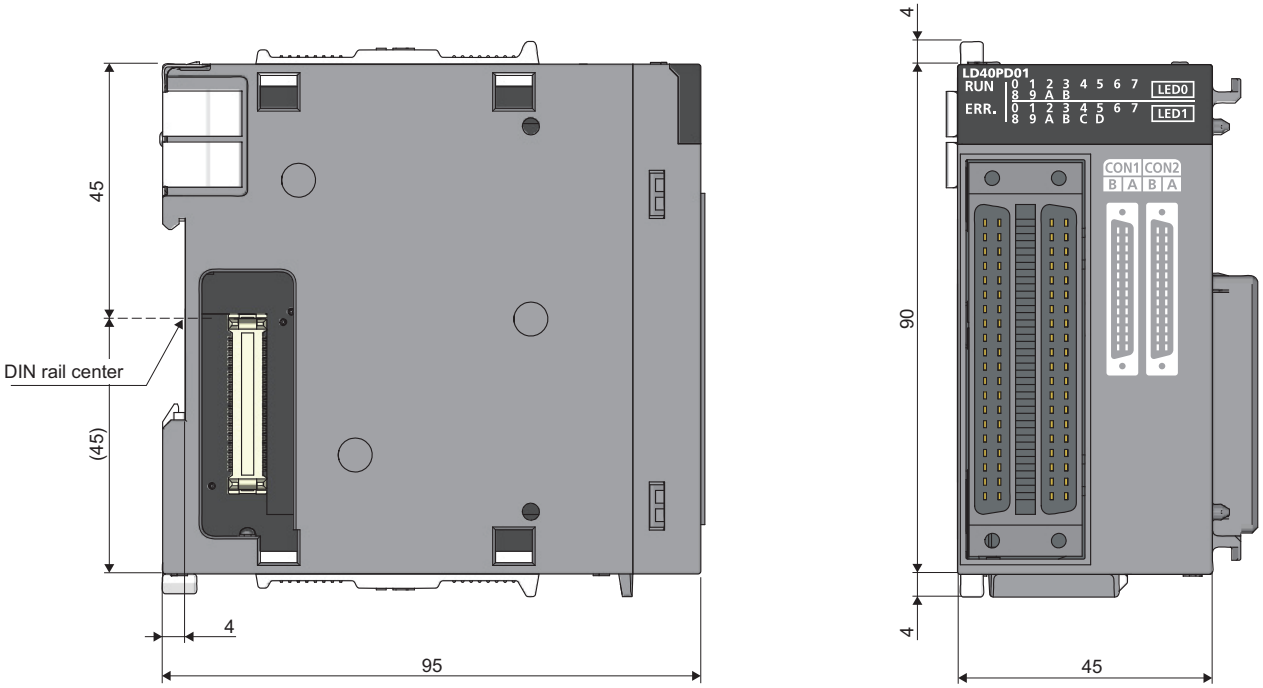
The following table lists the added or changed functions of the flexible high-speed I/O control module, the configuration tool, and GX Works2.

Addition/Change	Upper five digits of the applicable product information number of the flexible high-speed I/O control module	Applicable version of the configuration tool	Applicable version of GX Works2	Reference
Security	—	Version 1.001B	—	☞ Page 74 Security
Read from module (Flash ROM)				☞ Page 90 Reading data from the module
SSI encoder block	17102 or later	Version 1.002C		☞ Page 114 SSI encoder block
Changes of an external output block • Addition of Forced Output • Addition of External terminal monitor				☞ Page 123 External output block
Changes of a comparison block • Coincidence or Range can be selected for Condition. • Compare values can be changed.				☞ Page 158 Comparison block
An event input terminal can be linked with a Latch terminal of a counter timer block.				☞ Page 135 Event input terminal
Switching the language	—			☞ Page 66 Switching the Language
Copying a block				☞ Page 83 Copying a block
Pasting a block				☞ Page 84 Pasting a block
Library function				☞ Page 85 Library Function
Verifying with the module (Flash ROM)				☞ Page 91 Verifying with the module
Module operation				☞ Page 92 Module operation
Addition of monitorable terminals • External input terminal corresponding to an external input block • Output 0 terminal of a multi function counter block • External output terminal corresponding to an external output block	17102 or later			☞ Page 93 Monitor
Connecting to a head module	19022 or later	—	1.560J or later	☞ Page 34 SYSTEM CONFIGURATION
Adding a module, switch setting, auto refresh with GX Works2				☞ Page 204 SETTINGS

Appendix 6 External Dimensions

The following figures show the external dimensions of the flexible high-speed I/O control module.

LD40PD01



(Unit: mm)

A

INDEX

V

W

Y

I

REVISIONS

*The manual number is given on the bottom left of the back cover.

Revision date	*Manual number	Description
October 2015	SH(NA)-081532ENG-A	First edition
March 2017	SH(NA)-081532ENG-B	■Added or modified parts SAFETY PRECAUTIONS, INTRODUCTION, COMPLIANCE WITH EMC AND LOW VOLTAGE DIRECTIVES, RELEVANT MANUALS, MANUAL PAGE ORGANIZATION, TERMS, Chapter 2, Section 3.1 to 3.4, 5.1, 5.2, 6.1, 6.2, 6.5, 8.2, 8.9, 8.10, 9.1 to 9.3, Chapter 11, Section 13.1 to 13.3, 14.4, 14.5, 14.7, Appendix 1, 2, 5

Japanese manual number: SH-081531-D

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.

However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place. Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to:

(1) Damages caused by any cause found not to be the responsibility of Mitsubishi.

(2) Loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products.

(3) Special damages and secondary damages whether foreseeable or not, compensation for accidents, and compensation for damages to products other than Mitsubishi products.

(4) Replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

TRADEMARKS

The company names, system names and product names mentioned in this manual are either registered trademarks or trademarks of their respective companies.
In some cases, trademark symbols such as '™' or '®' are not specified in this manual.

SH(NA)-081532ENG-B(1703)MEE
MODEL: LD40PD01-U-E
MODEL CODE: 13JX37

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : TOKYO BUILDING, 2-7-3 MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN
NAGOYA WORKS : 1-14 , YADA-MINAMI 5-CHOME , HIGASHI-KU, NAGOYA , JAPAN