

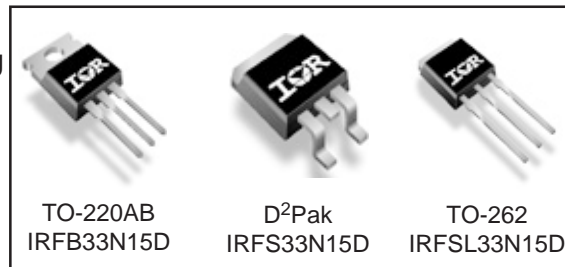
Applications

- High frequency DC-DC converters

V_{DSS}	$R_{DS(on) \max}$	I_D
150V	0.056Ω	33A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	33	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	24	
I_{DM}	Pulsed Drain Current ①	130	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ⑦	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	170	
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	4.4	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw ⑥	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input Active Clamp Forward Converter

Notes ① through ⑦ are on page 11

IRFB/IRFS/IRFSL33N15D

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

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	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.056	Ω	$V_{GS} = 10V, I_D = 20A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = 50V, I_D = 20A$
Q_g	Total Gate Charge	—	60	90	nC	$I_D = 20A$
Q_{gs}	Gate-to-Source Charge	—	17	26		$V_{DS} = 120V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	27	41		$V_{GS} = 10V, \text{④⑥}$
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 75V$
t_r	Rise Time	—	38	—		$I_D = 20A$
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		$R_G = 3.6\Omega$
t_f	Fall Time	—	21	—		$V_{GS} = 10V, \text{④}$
C_{iss}	Input Capacitance	—	2020	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	400	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	91	—		$f = 1.0\text{MHz}$ ⑥
C_{oss}	Output Capacitance	—	2440	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	180	—		$V_{GS} = 0V, V_{DS} = 120V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	320	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑤

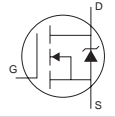
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②⑥	—	330	mJ
I_{AR}	Avalanche Current ①	—	20	A
E_{AR}	Repetitive Avalanche Energy ①	—	17	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.90	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	130		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	150	—	ns	$T_J = 25^\circ\text{C}, I_F = 20A$
Q_{rr}	Reverse Recovery Charge	—	920	—	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

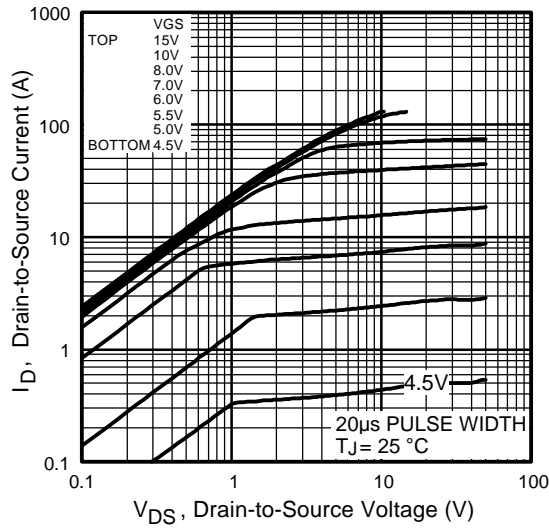


Fig 1. Typical Output Characteristics

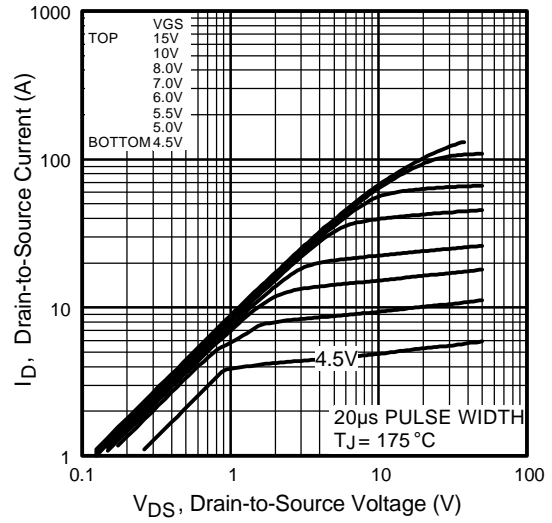


Fig 2. Typical Output Characteristics

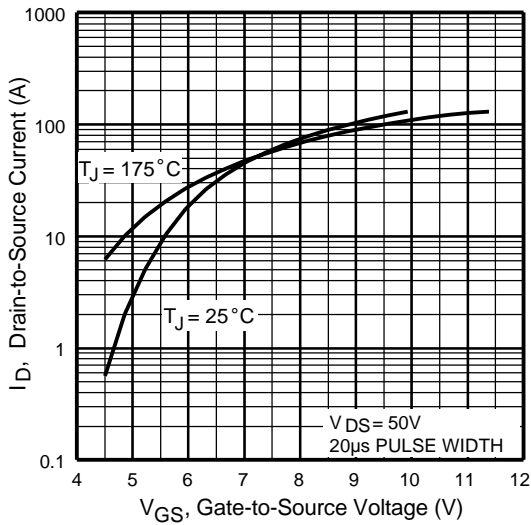


Fig 3. Typical Transfer Characteristics

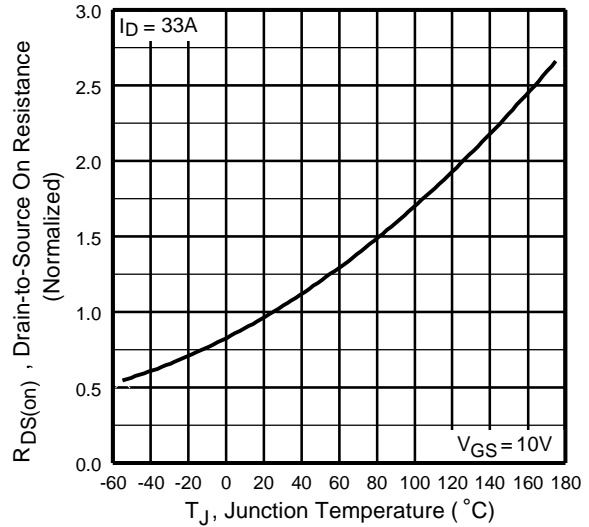


Fig 4. Normalized On-Resistance Vs. Temperature

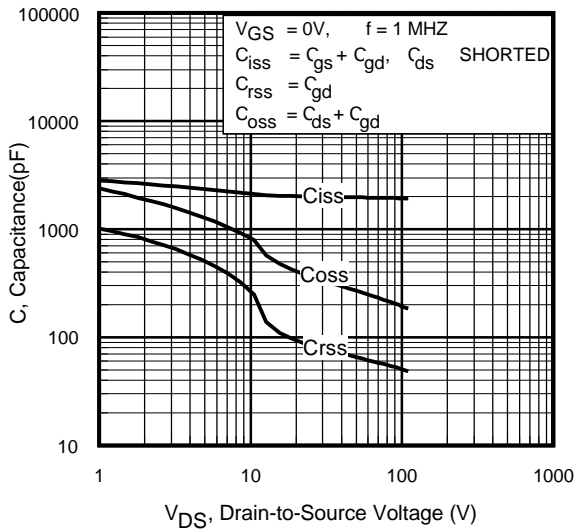


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

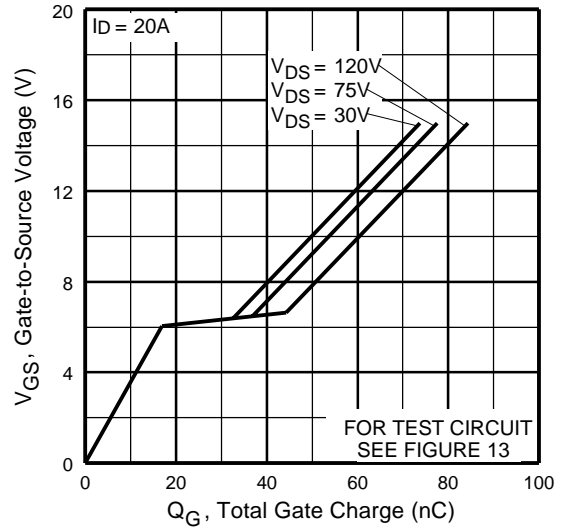


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

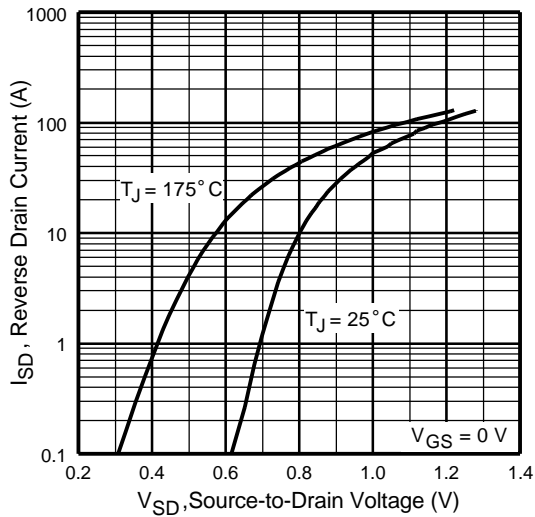


Fig 7. Typical Source-Drain Diode Forward Voltage

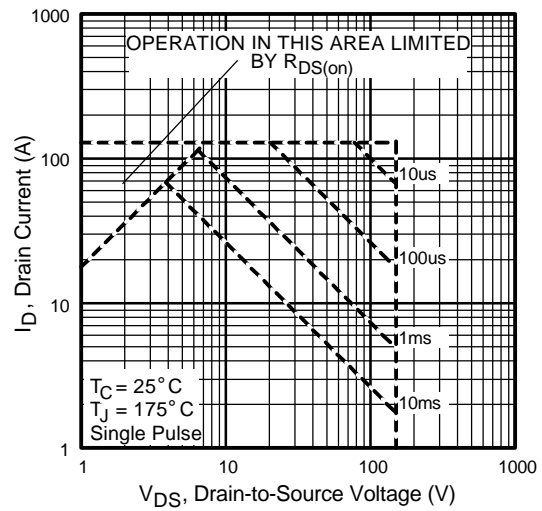


Fig 8. Maximum Safe Operating Area

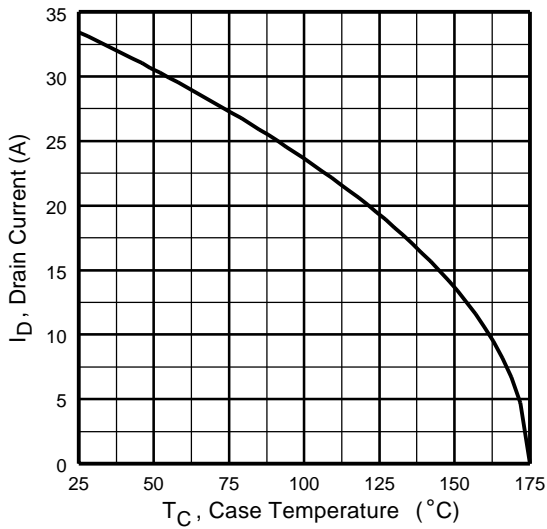


Fig 9. Maximum Drain Current Vs. Case Temperature

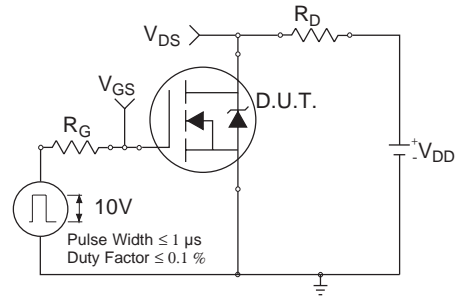


Fig 10a. Switching Time Test Circuit

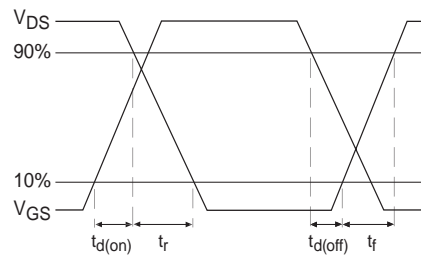


Fig 10b. Switching Time Waveforms

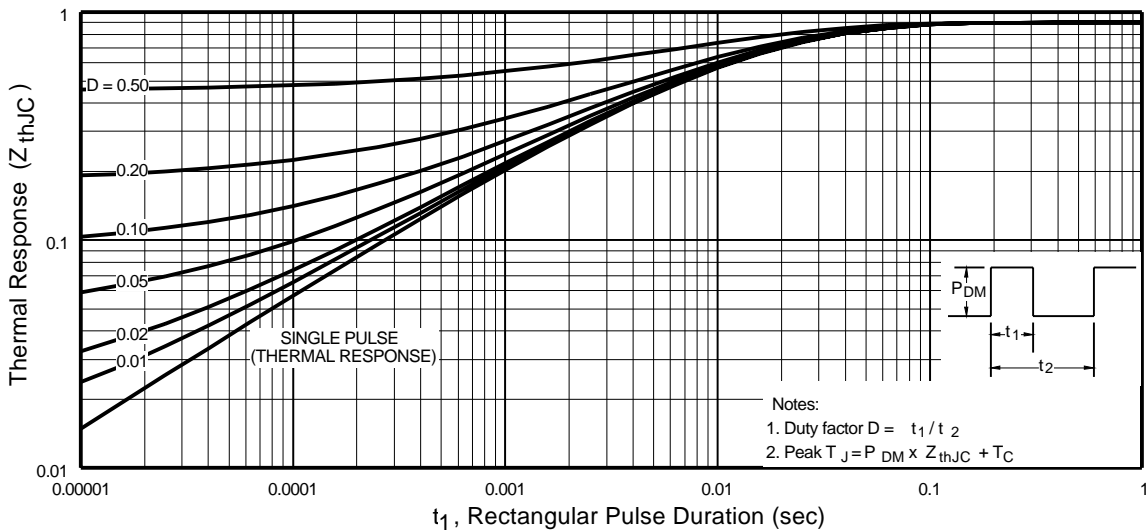


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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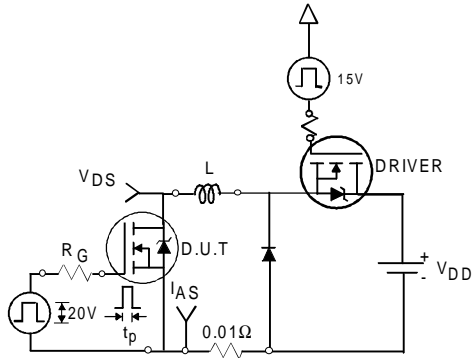


Fig 12a. Unclamped Inductive Test Circuit

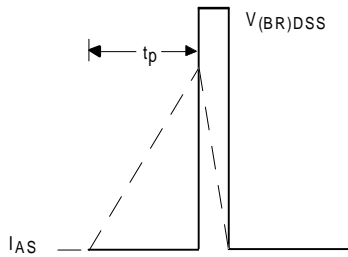


Fig 12b. Unclamped Inductive Waveforms

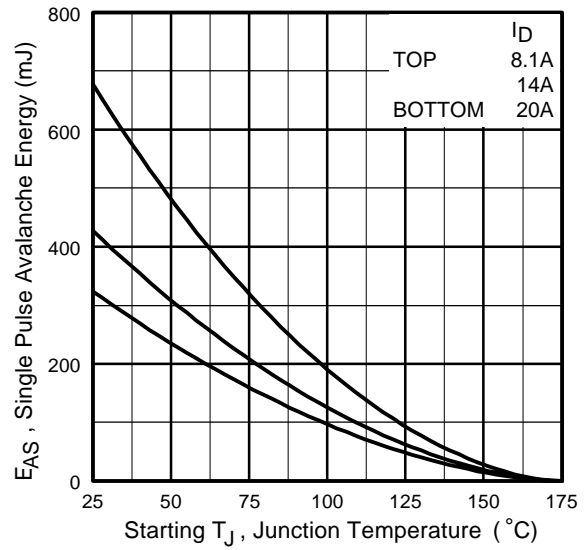


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

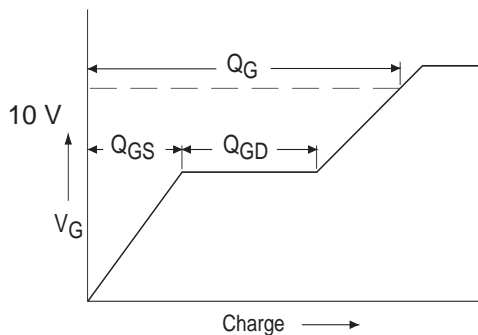


Fig 13a. Basic Gate Charge Waveform

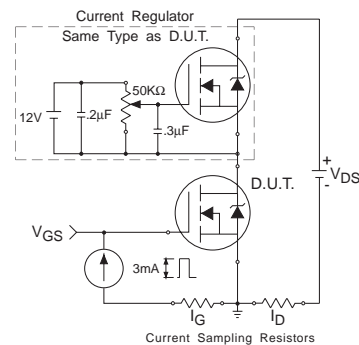
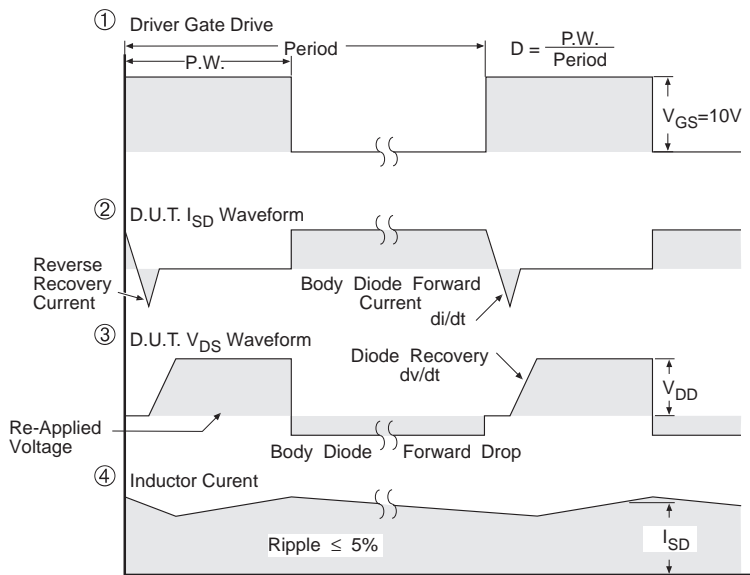


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

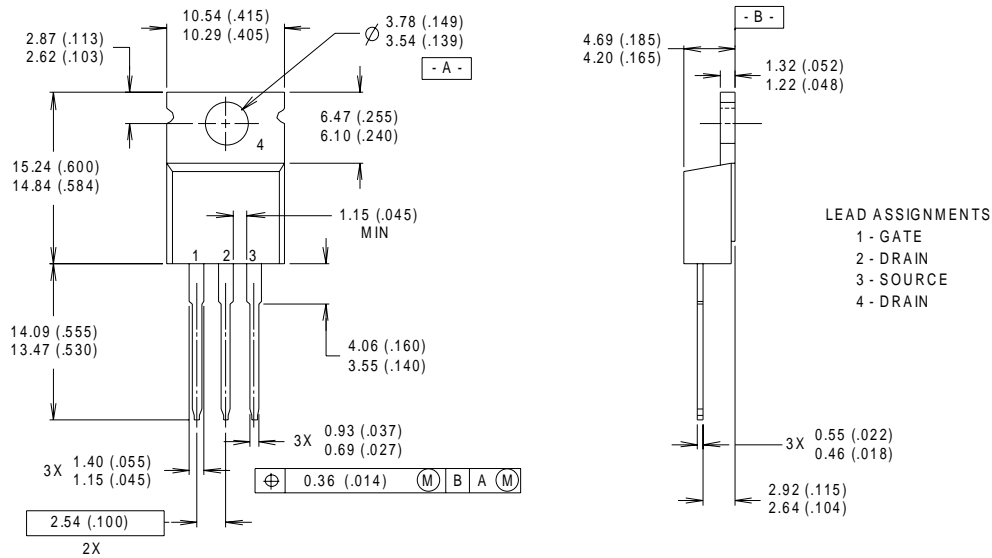
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



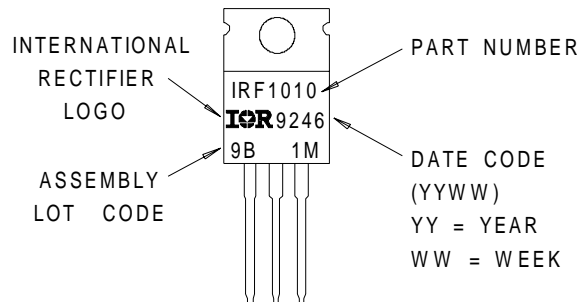
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

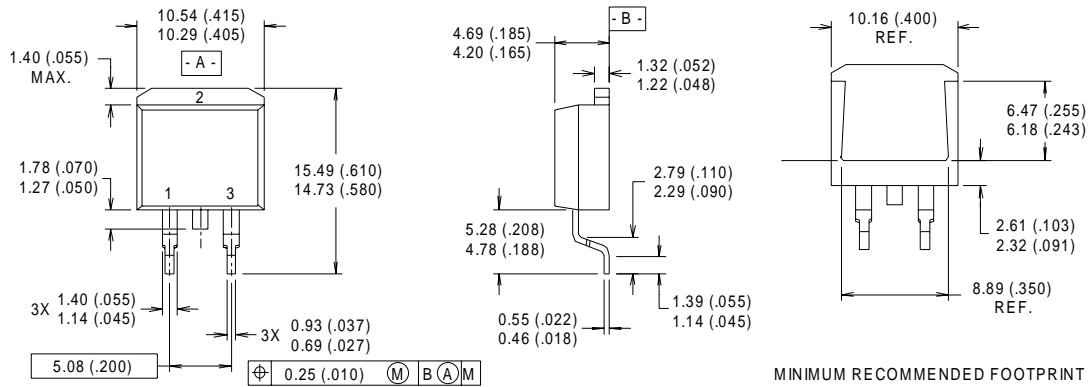
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



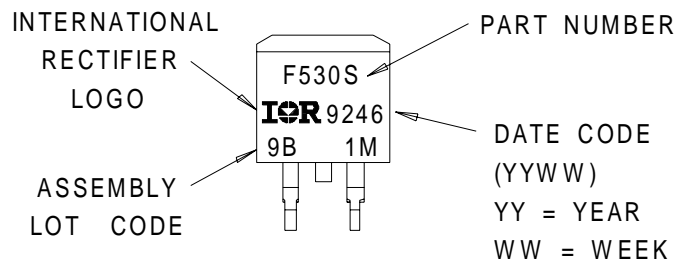
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

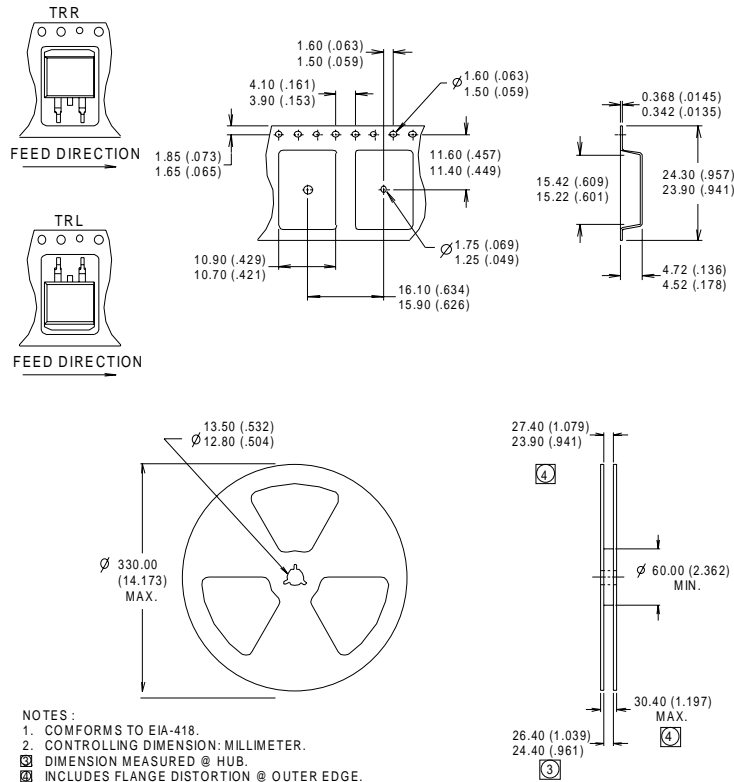
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

D²Pak Part Marking Information



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.7\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 20\text{A}$.
- ③ $I_{SD} \leq 20\text{A}$, $di/dt \leq 280\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>