SPECIFICATION

Device Name : IGBT - IPM

Type Name : 6MBP15RA120

Spec. No. : MS6M0741

Fuji Electric Co., Ltd.
Matsumoto Factory

	DATE	NAME	APPROVED
DRAWN	Aug -28-03	Y. Kusunoki	
CHECKED	Aug 29-03	T. Miyazaki K. Yamada	T. Fujihira

Fuji Electric Co.,Ltd.

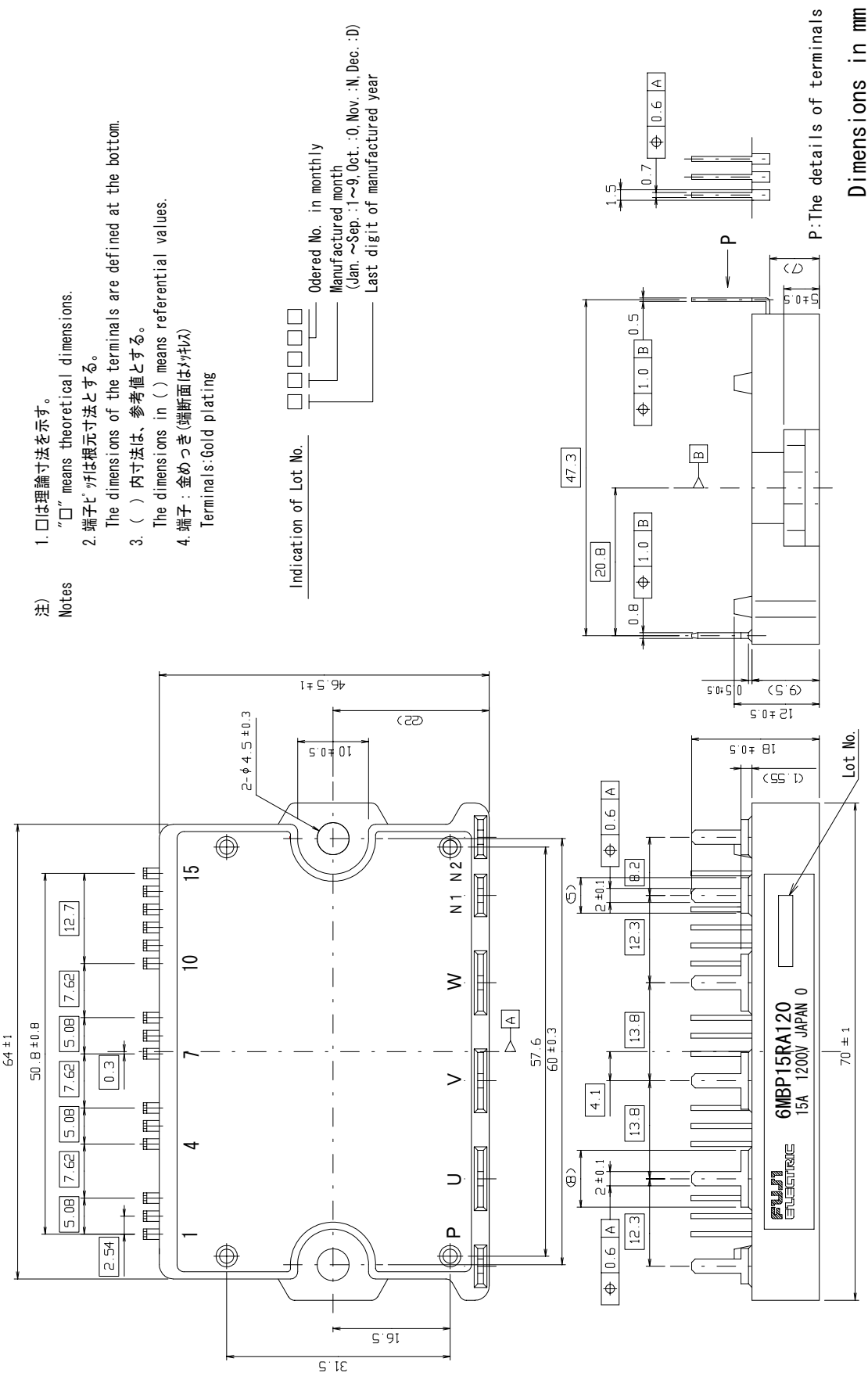
DWG.NO. MS6M0741 1/22

Revised Records

Date	Classi-fication	Ind.	Content	Applied date	Drawn	Checked	Approved
Aug 28 2003	enactment	—	———	Issued date	Y. Kuwaoki	T. Miyoshi K. Yamada	T. Fujishima

1. Package Outline Drawing 外形図

Package type : P619



2. Pin Descriptions

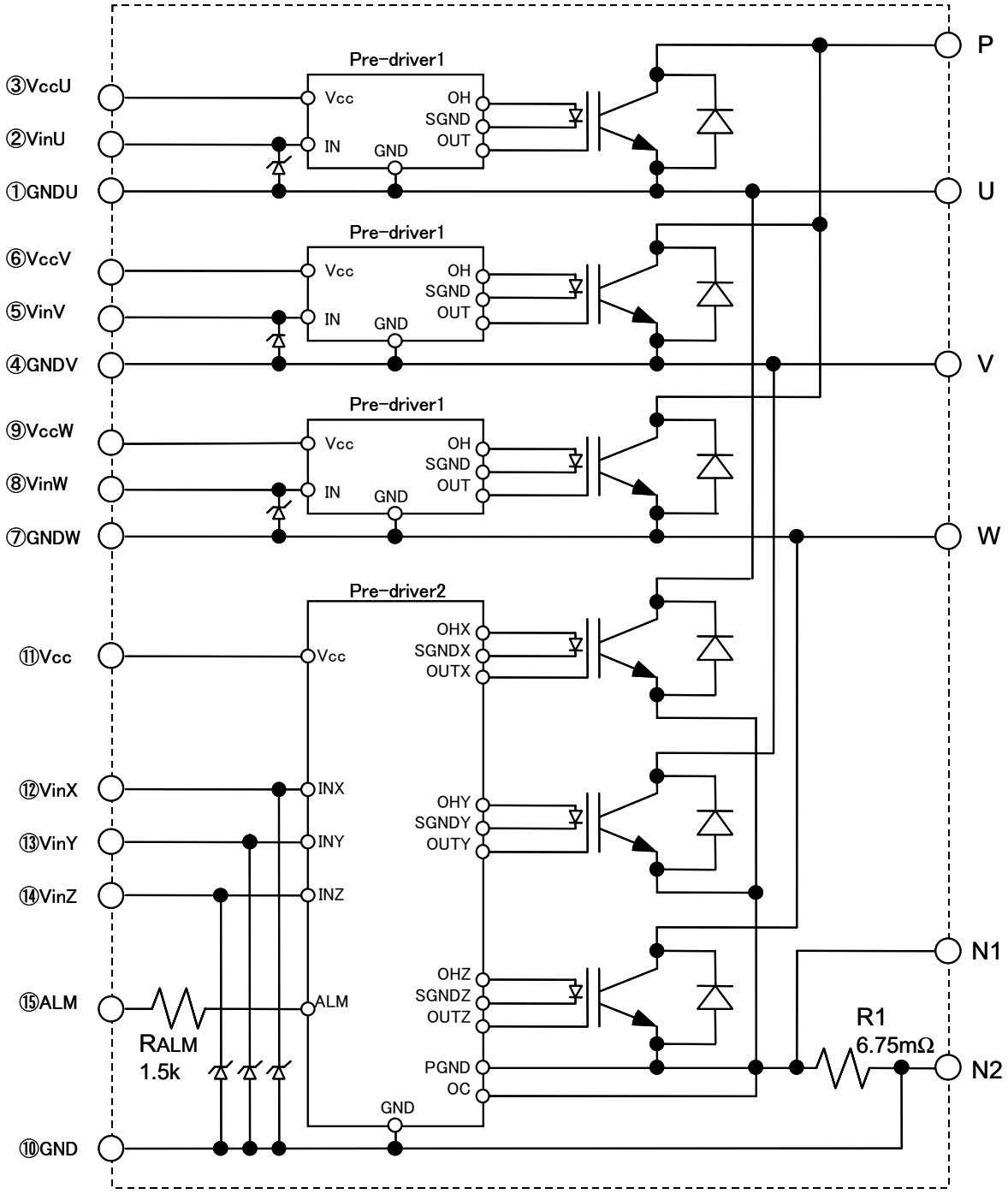
Main circuit

Symbol	Description
P	Positive input supply voltage.
U	Output (U).
V	Output (V).
W	Output (W).
N1	(For connection an external shunt-resistor)
N2	Negative input supply voltage.

Control circuit

No.	Symbol	Description
①	GNDU	High side ground (U).
②	VinU	Logic input for IGBT gate drive (U).
③	VccU	High side supply voltage (U).
④	GNDV	High side ground (V).
⑤	VinV	Logic input for IGBT gate drive (V).
⑥	VccV	High side supply voltage (V).
⑦	GNDW	High side ground (W).
⑧	VinW	Logic input for IGBT gate drive (W).
⑨	VccW	High side supply voltage (W).
⑩	GND	Low side ground.
⑪	Vcc	Low side supply voltage.
⑫	VinX	Logic input for IGBT gate drive (X).
⑬	VinY	Logic input for IGBT gate drive (Y).
⑭	VinZ	Logic input for IGBT gate drive (Z).
⑮	ALM	Low side alarm signal output.

3. Block Diagram



Pre-drover1 includes following functions.

(P-side)

1. Amplifier for driver
2. Under voltage lockout circuit
3. IGBT chip over heating protection

Pre-drover2 includes following functions.

(N-side)

1. Amplifier for driver
2. Under voltage lockout circuit
3. IGBT chip over heating protection
4. Over current protection
5. Alarm signal output

4. Absolute Maximum Ratings

Tc＝25℃ unless otherwise specified.

Items		Symbol	Min.	Max.	Units
Bus Voltage (between terminal P and N)	DC	V_{DC}	0	900	V
	Surge	$V_{DC(surge)}$	0	1000	V
	Short operating	Vsc	400	800	V
Collector-Emitter Voltage *1		Vces	0	1200	V
Collector Current	DC	Ic	-	15	A
	1ms	Icp	-	30	A
	Duty=78% *2	-Ic	-	15	A
Collector Power Dissipation	One transistor *3	Pc	-	92	W
Supply Voltage of Pre-Driver *4		Vcc	-0.5	20	V
Input Signal Voltage *5		Vin	-0.5	Vcc+0.5	V
Input Signal Current		Iin	-	1	mA
Alarm Signal Voltage *6		VALM	-0.5	Vcc	V
Alarm Signal Current *7		IALM	-	20	mA
Junction Temperature		Tj	-	150	℃
Operating Case Temperature		Topr	-20	100	℃
Storage Temperature		Tstg	-40	125	℃
Solder Temperature *8		Tsol	-	260	℃
Isolating Voltage (Terminal to base, 50/60Hz sine wave 1min.)		Viso	-	AC2500	V
Screw Torque	Mounting (M4)	-	-	2.0	Nm

Note

*1 : Vces shall be applied to the input voltage between terminal P and U or V or W ,N and U or V or W.

*2 : Duty=125℃/FWD Rth(j-c)/(Ic×VF MAX)=125/3.46/(15×3.1)×100=78%

*3 : Pc=125℃/IGBT Rth(j-c)=125/1.36=92W

*4 : VCC shall be applied to the input voltage between terminal No.3 and 1,6 and 4, 9 and 7, 11 and 10.

*5 : V_{in} shall be applied to the input voltage between terminal No.2 and 1, 5 and 4, 8 and 7, 12,13,14 and 10.

*6 : VALM shall be applied to the voltage between terminal No.15 and 10.

*7 : IALM shall be applied to the input current to terminal No.15.

*8 : Immersion time 10±1sec

5. Electrical Characteristics

Tj＝25℃, Vcc＝15V unless otherwise specified.

5.1 Main circuit

Item	Symbol	Conditions		Min.	Typ.	Max.	Units
Collector Current at off signal input	I_{CES}	V_{CE}＝1200V Vin terminal open.		-	-	1.0	mA
Collector-Emitter saturation voltage	$V_{CE(sat)}$	Ic＝15A	Terminal	-	-	2.8	V
			Chip	-	2.3	-	V
Forward voltage of FWD	VF	-Ic＝15A	Terminal	-	-	3.1	V
			Chip	-	2.3	-	V
Turn-on time	ton	V_{DC}＝600V、Tj=125℃		1.2	-	-	us
Turn-off time	toff	Ic＝15A Fig.1, Fig.6		-	-	3.6	
Reverse recovery time	trr	V_{DC}＝600V IF＝15A Fig.1, Fig.6		-	-	0.3	

5.2 Control circuit

Item	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply current of P-side pre-driver (one unit)	Iccp	Switching Frequency : 0～6kHz Tc=-20～100℃ Fig.7		0.5	-	9	mA
Supply current of N-side pre-driver	Iccn			0.8	-	28	mA
Input signal threshold voltage	Vin(th)	ON		1.0	1.35	1.7	V
		OFF		1.25	1.6	1.95	
Input Zener Voltage	Vz	Rin＝20kΩ		-	8.0	-	V
Alarm Signal Hold Time	tALM	Fig.2	Tc＝-20℃	1.1	-	-	ms
			Tc＝25℃	-	2.0	-	
			Tc＝125℃	-	-	4.0	
Current Limit Resistor	RALM	Alarm terminal		1425	1500	1575	Ω
Shunt-Resistor for over current sense	R1	Between terminal N1 and N2		-	6.75	-	mΩ

5.3 Protection Section （Vcc＝15V）

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Over Current Protection Level of Inverter circuit	Ioc	Tj=125℃	23	-	-	A
Over Current Protection Delay time	tdoc	Tj=125℃	-	5	-	us
IGBT Chips Over Heating Protection Temperature Level	TjOH	Surface of IGBT Chips	150	-	-	℃
Over Heating Protection Hysteresis	TjH		-	20	-	℃
Under Voltage Protection Level	VUV		11.1	11.7	12.4	V
Under Voltage Protection Hysteresis	VH		0.2	0.5	0.8	

6. Thermal Characteristics （Tc＝25℃）

Item		Symbol	Min.	Typ.	Max.	Units
Junction to Case	IGBT	Rth(j-c)	-	-	1.36	℃/W
Thermal Resistance *9	FWD	Rth(j-c)	-	-	3.46	
Case to Fin Thermal Resistance with Compound		Rth(c-f)	-	0.05	-	

*9:(For 1device, Case is under the device)

7. Noise Immunity （Vdc=600V、Vcc=15V、Test Circuit Fig 5.）

Item	Conditions	Min.	Typ.	Max.	Units
Common mode rectangular noise	Pulse width 1us,polarity ±,10 minutes Judge：no over-current, no miss operating	±2.0	-	-	kV
Common mode lightning surge	Rise time 1.2us,Fall time 50us Interval 20s,10 times Judge：no over-current, no miss operating	±5.0	-	-	kV

8. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
DC Bus Voltage	VDC	-	-	800	V
Power Supply Voltage of Pre-Driver	Vcc	13.5	15.0	16.5	V
Screw Torque (M4)	-	1.3	-	1.7	Nm

9. Weight

Item	Symbol	Min.	Typ.	Max.	Units
Weight	Wt	-	85	-	g

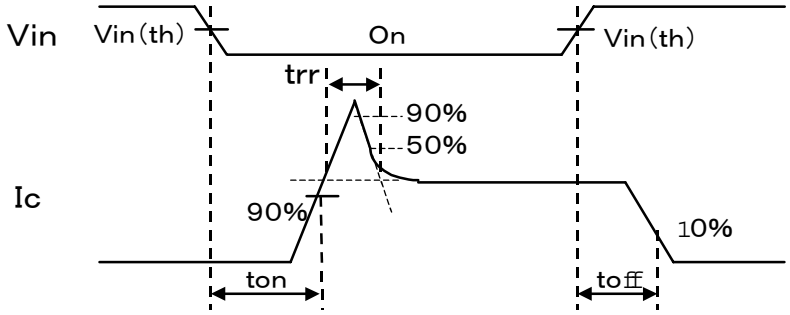


Figure 1. Switching Time Waveform Definitions

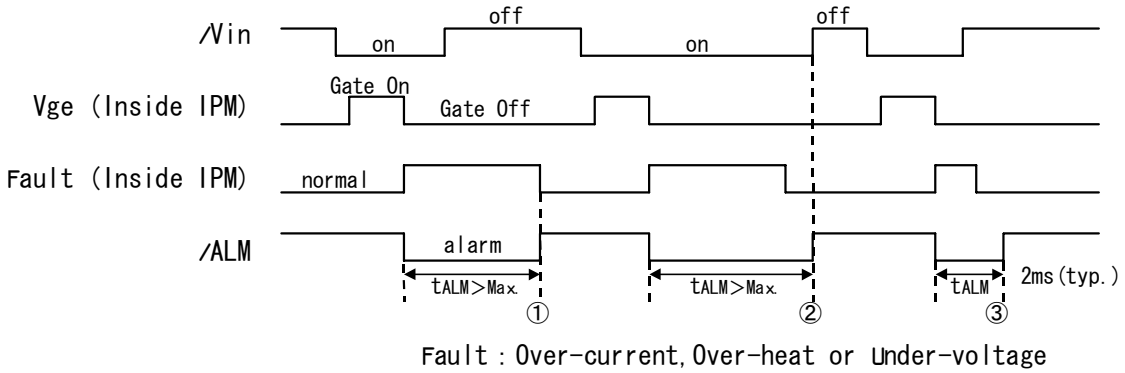


Figure 2. Input/Output Timing Diagram

Necessary conditions for alarm reset (refer to ① to ③ in figure2.)

① This represents the case when a failure-causing Fault lasts for a period more than tALM. The alarm resets when the input Vin is OFF and the Fault has disappeared.

② This represents the case when the ON condition of the input Vin lasts for a period more than tALM. The alarm resets when the Vin turns OFF under no Fault conditions.

③ This represents the case when the Fault disappears and the Vin turns OFF within tALM. The alarm resets after lasting for a period of the specified time tALM.

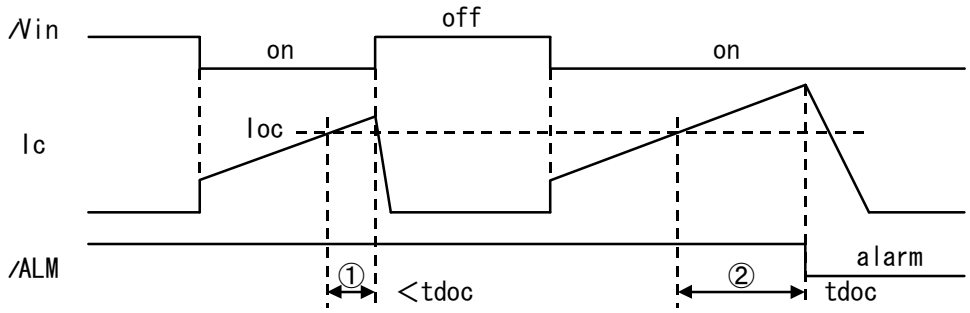


Figure 3. Over-current Protection Timing Diagram

Period ①: When a collector current over the OC level flows and the OFF command is input within a period less than the trip delay time tdoc, the current is hard-interrupted and no alarm is output.

Period ②: When a collector current over the OC level flows for a period more than the trip delay time tdoc, the current is soft-interrupted. If this is detected at the lower arm IGBTs, an alarm is output.

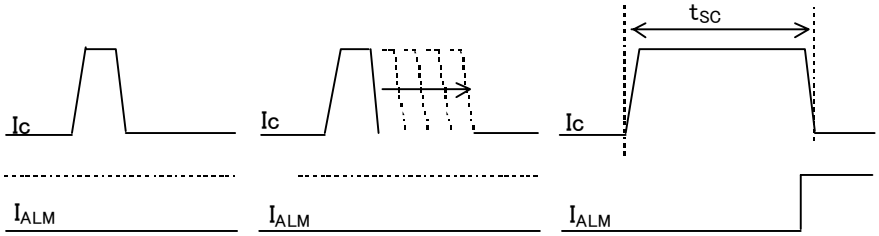


Figure.4 Definition of tsc

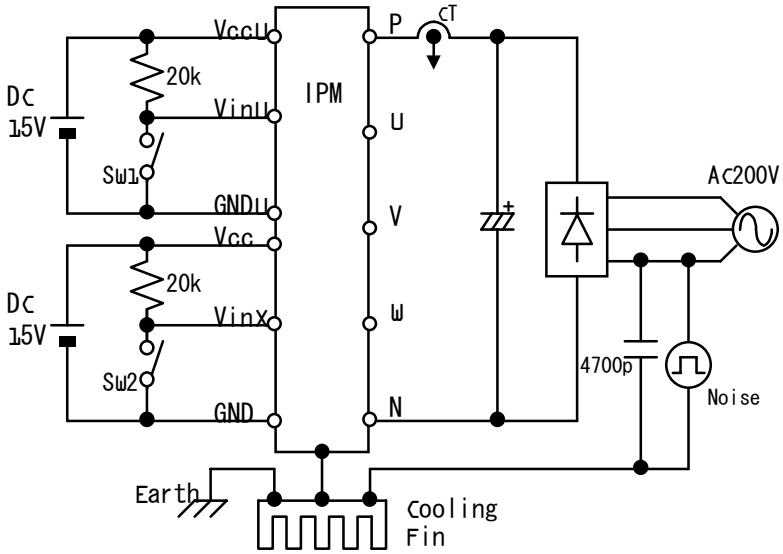


Figure 5. Noise Test Circuit

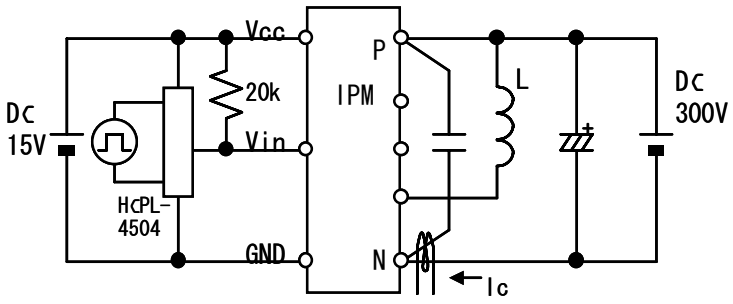


Figure 6. Switching Characteristics Test Circuit

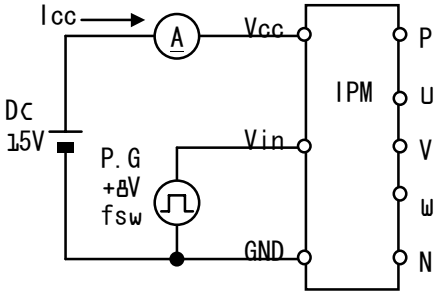


Figure 7. Icc Test Circuit

10. Truth table

10.1 IGBT Control

The following table shows the IGBT ON/OFF status with respect to the input signal Vin.

The IGBT turn-on when Vin is at “Low” level under no alarm condition.

Input (Vin)	Alarm	Output (IGBT)
Low	High	ON
Low	Low	OFF
High	–	OFF

10.2 Fault Detection

(1) When a fault is detected at the high side, only the detected arm stops its output.
At that time the IPM dosen’t any alarm.

(2) When a fault is detected at the low side, all the lower arms stop their outputs and the IPM outputs an alarm of the low side.

	Cause of Fault	IGBT				Alarm Output
		High side (U-phase)	High side (V-phase)	High side (W-phase)	Low side	ALM
High side (U-phase)	UV	OFF	*	*	*	High
	TjOH	OFF	*	*	*	High
High side (V-phase)	UV	*	OFF	*	*	High
	TjOH	*	OFF	*	*	High
High side (W-phase)	UV	*	*	OFF	*	High
	TjOH	*	*	OFF	*	High
Low side	OC	*	*	*	OFF	Low
	UV	*	*	*	OFF	Low
	TjOH	*	*	*	OFF	Low

*: Depend on input logic.

11. Cautions for design and application

1. Trace routing layout should be designed with particular attention to least stray capacity between the primary and secondary sides of optical isolators by minimizing the wiring length between the optical isolators and the IPM input terminals as possible.
フォトカプラとIPMの入力端子間の配線は極力短くし、フォトカプラの一次側と二次側の浮遊容量を小さくしたパターンレイアウトにして下さい。

2. Mount a capacitor between Vcc and GND of each high-speed optical isolator as close to as possible.
高速フォトカプラのVcc-GND間に、コンデンサを出来るだけ近接して取り付けて下さい。

3. For the high-speed optical isolator, use high-CMR type one with tpHL, tpLH ≦ 0.8μs.
高速フォトカプラは、tpHL,tpLH≦0.8us、高CMRタイプをご使用ください。

4. For the alarm output circuit, use low-speed type optical isolators with CTR ≧ 100%.
アラーム出力回路は、低速フォトカプラCTR≧100%のタイプをご使用ください。

5. For the control power Vcc, use four power supplies isolated each. And they should be designed to reduce the voltage variations.
制御電源Vccは、絶縁された4電源を使用してください。また、電圧変動を抑えた設計として下さい。

6. Suppress surge voltages as possible by reducing the inductance between the DC bus P and N, and connecting some capacitors between the P and N terminals.
P-N間の直流母線は出来るだけ低インダクタンス化し、P-N端子間にコンデンサを接続するなどしてサージ電圧を低減して下さい。

7. To prevent noise intrusion from the AC lines, connect a capacitor of some 4700pF between the three-phase lines each and the ground.
ACラインからのノイズ侵入を防ぐために、3相各線ーアース間に4700pF程のコンデンサを接続して下さい。

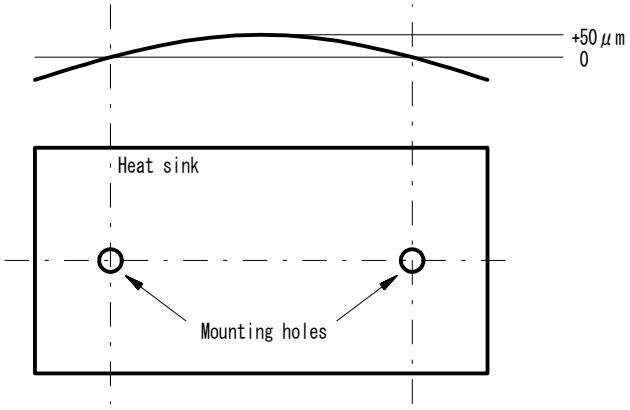
8. At the external circuit, never connect the control terminal GNDU to the main terminal U-phase, GNDV to V-phase, GNDW to W-phase, and GND to N-phase. Otherwise, malfunctions may be caused.
制御端子GNDUと主端子U相、制御端子GNDVと主端子V相、制御端子GNDWと主端子W相、制御端子GNDと主端子Nを外部回路で接続しないで下さい。誤動作の原因になります。

9. Take note that an optical isolator's response to the primary input signal becomes slow if a capacitor is connected between the input terminal and GND.
入力端子-GND間にコンデンサを接続すると、フォトカプラー次側入力信号に対する応答時間が長くなりますのでご注意ください。

10. Taking the used isolator's CTR into account, design with a sufficient allowance to decide the primary forward current of the optical isolator.
フォトカプラの一次側電流は、お使いのフォトカプラのCTRを考慮し、十分に余裕をもった設計にして下さい。

11. Apply thermal compound to the surfaces between the IPM and its heat sink to reduce the thermal contact resistance.
接触熱抵抗を小さくするために、IPMとヒートシンクの間にサーマルコンパウンドを塗布して下さい。

12. Finish the heat sink surface within roughness of 10μm and flatness (camber) between screw positions of 0 to +50μm. If the flatness is minus, the heat radiation becomes worse due to a gap between the heat sink and the IPM. And, if the flatness is over +50μm, there is a danger that the IPM copper base may be deformed and this may cause a dielectric breakdown.
ヒートシンク表面の仕上げは、粗さ10um以下、ネジ位置間での平坦度（反り）は、0～+50umとして下さい。平坦度がマイナスの場合、ヒートシンクとIPMの間に隙間ができ放熱が悪化します。また、平坦度が＋50um以上の場合IPMの銅ﾍﾞｰｽが変形し絶縁破壊を起こす危険性があります。

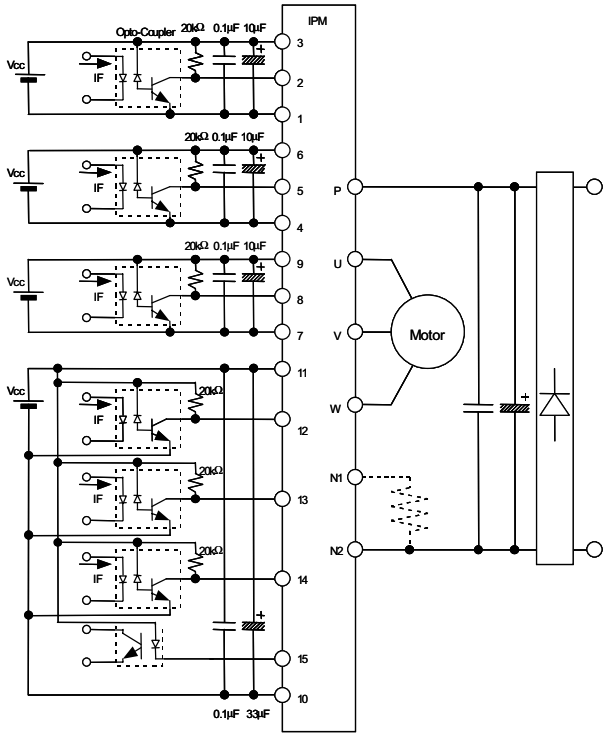


13. This product is designed on the assumption that it applies to an inverter use. Sufficient examination is required when applying to a converter use. Please contact Fuji Electric Co.,Ltd if you would like to applying to converter use.
本製品は、インバータ用途への適用を前提に設計されております。コンバータ用途へ適用される場合は、十分な検討が必要です。もし、コンバータへ適用される場合は御連絡ください。

14. There is thermal interference between nearby power devices,because the P619 PKG is a compact package. Therefore you measure the case temperature just under the IGBT chips that showed in report MT6M04858, and estimate the chip temperature.
パッケージを小型化しているため、パワー素子の熱干渉が考えられます。その為、チップ温度推定は必ずMT6M04858に示すチップ直下のケース温度を測定して行って下さい。

15. Please see the 『Fuji IGBT-IPM R SERIES APPLICATION MANUAL RH983』 and 『Fuji IGBT MODULES N SERIES APPLICATION MANUAL RH982』.
『富士IGBT-IPM Rシリーズ アプリケーションマニュアル RH983』及び『IGBTﾓｼﾞｭｰﾙ Nシリーズ アプリケーションマニュアル RH982』を御参照ください。

12. Example of applied circuit 応用回路例



13. Package and Marking 梱包仕様

Please see the MT6M4140 that is packing specification.

梱包仕様書 MT6M4140を御参照ください。

14. Cautions for storage and transportation 保管、運搬上の注意

- Store the modules at the normal temperature and humidity (5 to 35°C, 45 to 75%).
  常温常湿(5～35℃、45～75%)で保存して下さい。
- Avoid a sudden change in ambient temperature to prevent condensation on the module surfaces.
  モジュールの表面が結露しないよう、急激な温度変化を避けて下さい。
- Avoid places where corrosive gas generates or much dust exists.
  腐食性ガスの発生場所、粉塵の多い場所は避けて下さい。
- Store the module terminals under unprocessed conditions
  モジュールの端子は未加工の状態で保管すること。.
- Avoid physical shock or falls during the transportation.
  運搬時に衝撃を与えたり落下させないで下さい。

15. Scope of application 適用範囲

This specification is applied to the IGBT-IPM (type: 6MBP15RA120).

本仕様書は、IGBT-IPM (型式:6MBP15RA120)に適用する。

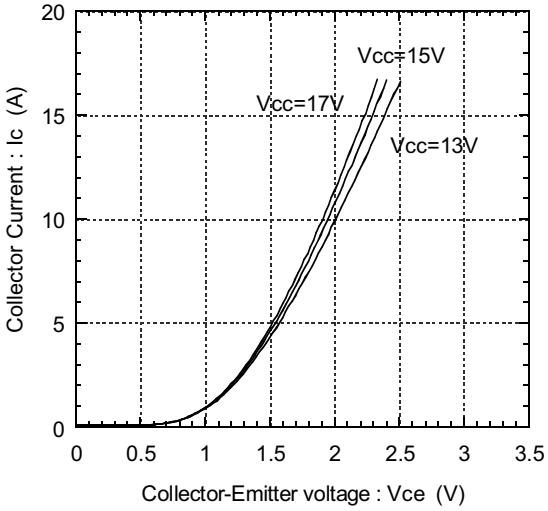
16. Based safety standards 準拠安全規格

UL1557

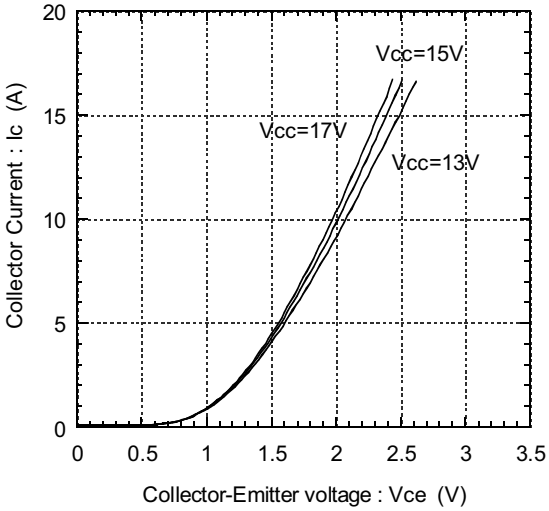
17.Characteristics
特性カーブ

17-1. Inverter
インバータ部

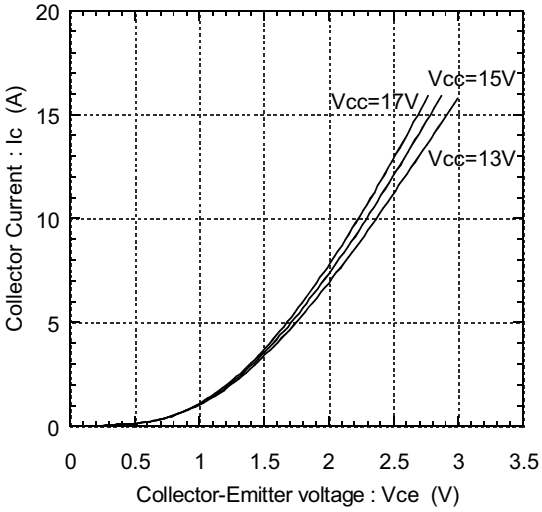
Collector current vs. Collector-Emitter voltage (typ.)
Tj=25°C / Chip



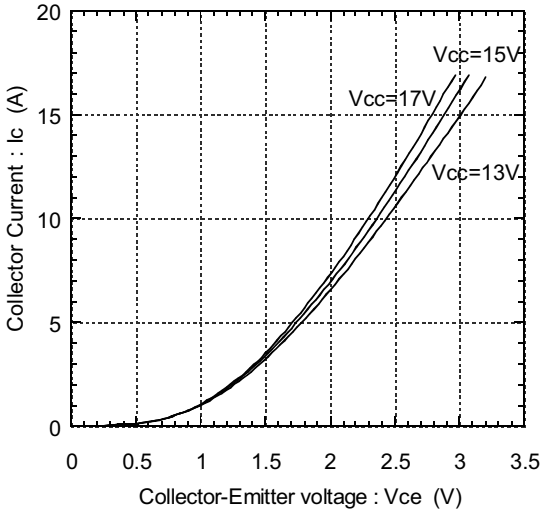
Collector current vs. Collector-Emitter voltage (typ.)
Tj=25°C / Terminal



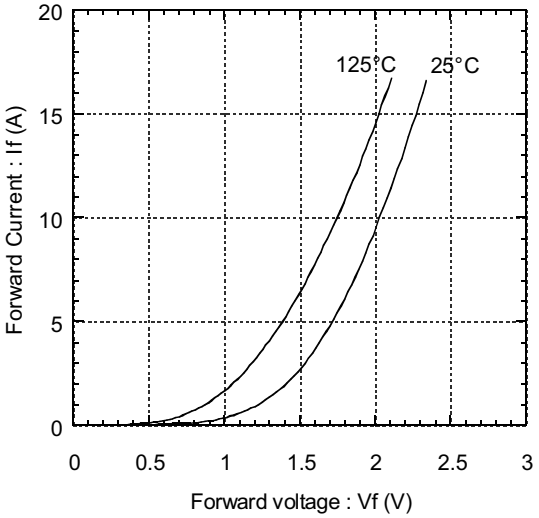
Collector current vs. Collector-Emitter voltage (typ.)
Tj=125°C / Chip



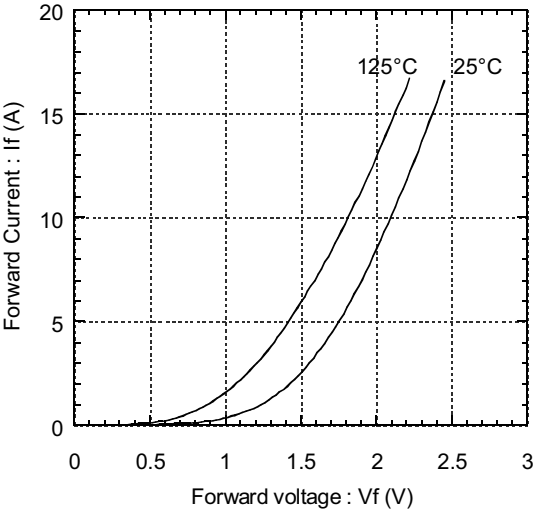
Collector current vs. Collector-Emitter voltage (typ.)
Tj=125°C / Terminal



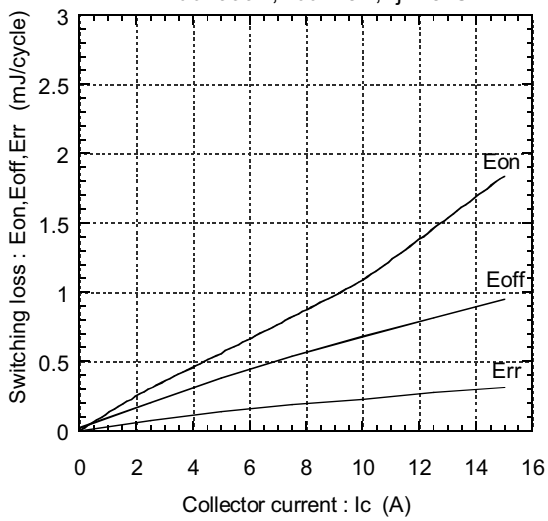
Forward current vs. Forward voltage (typ.)
Chip



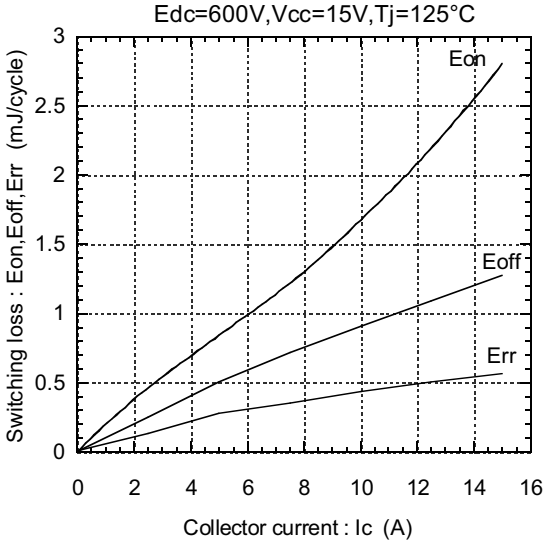
Forward current vs. Forward voltage (typ.)
Terminal



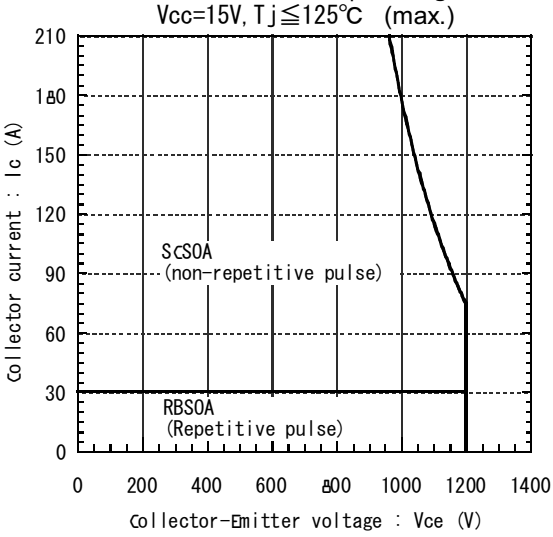
Switching Loss vs. Collector Current (typ.)
Edc=600V,Vcc=15V,Tj=25°C



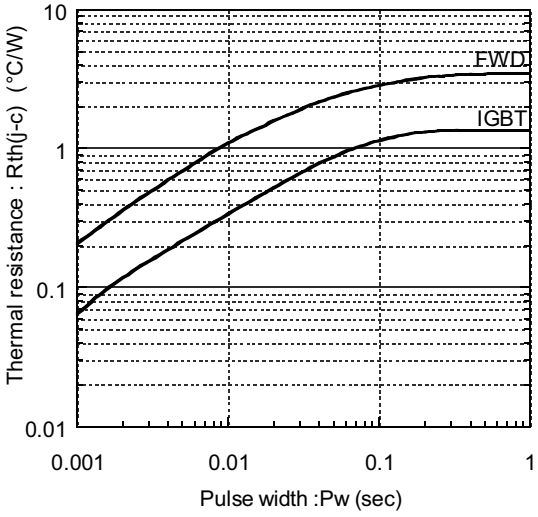
Switching Loss vs. Collector Current (typ.)
Edc=600V,Vcc=15V,Tj=125°C



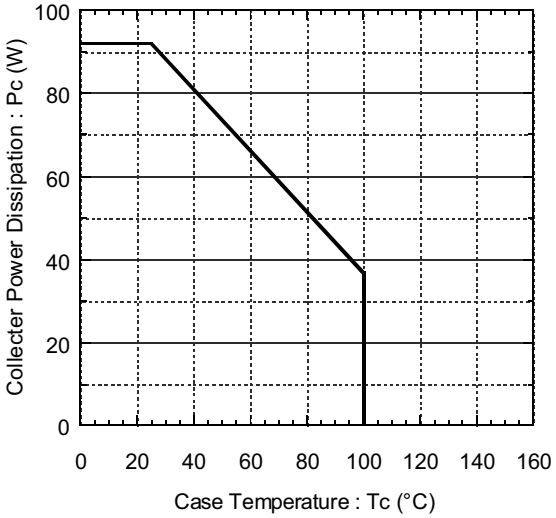
Reversed biased safe operating area
Vcc=15V, Tj≦125℃ (max.)



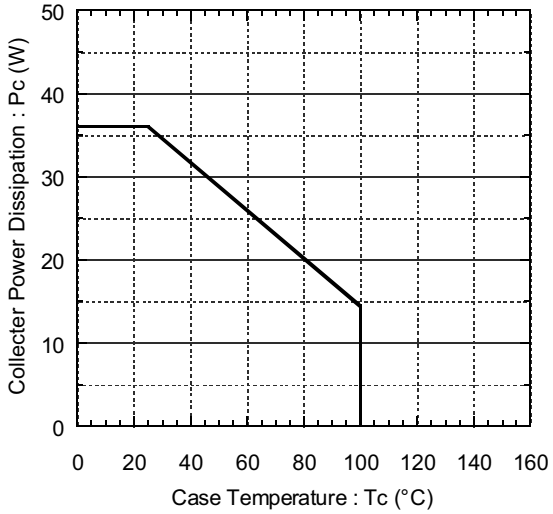
Transient thermal resistance
(max.)

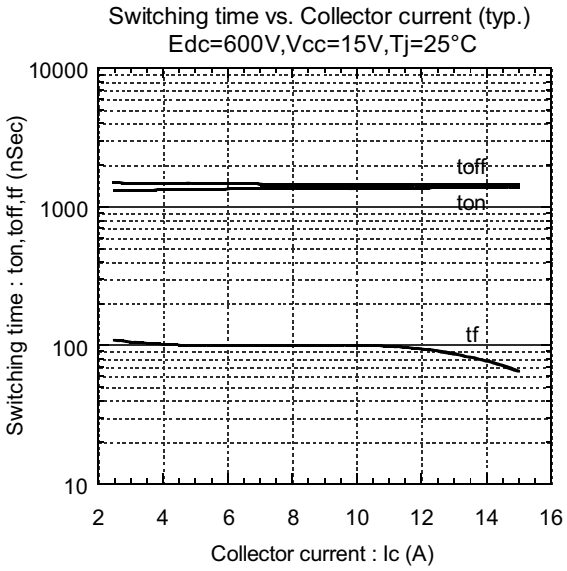


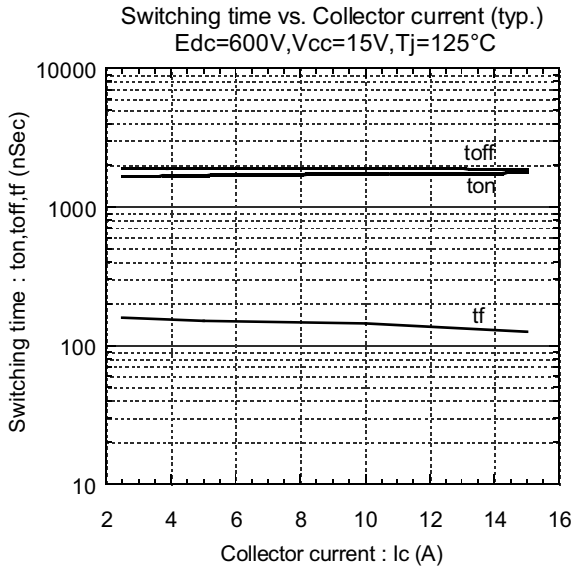
Power derating for IGBT (per device)
(max.)



Power derating for FWD (per device)
(max.)

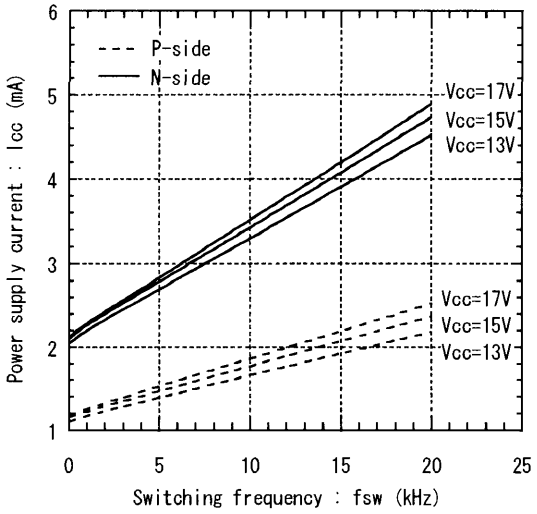




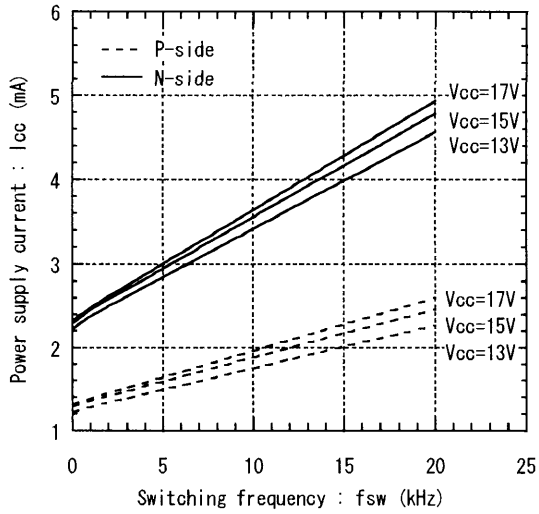


17-2. Control Circuit
制御部

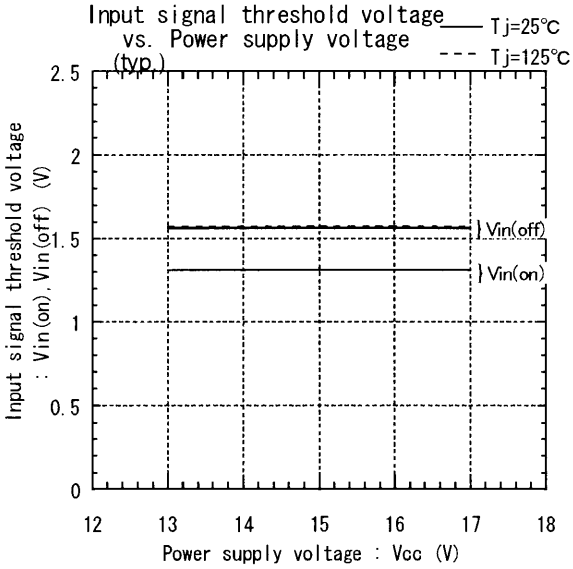
Power supply current vs. Switching frequency
Tc=100°C (typ.)



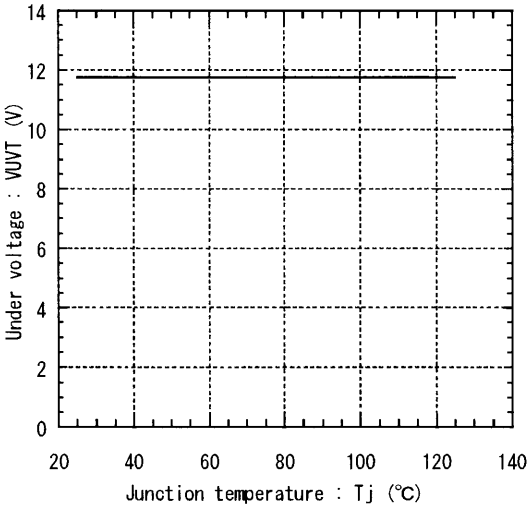
Power supply current vs. Switching frequency
Tc=25°C (typ.)



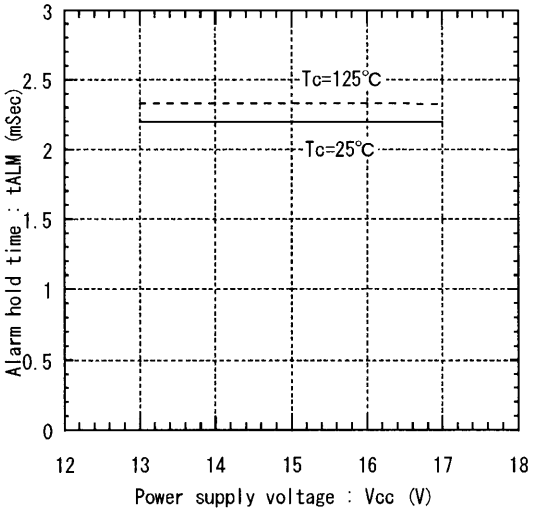
Input signal threshold voltage
vs. Power supply voltage
(typ.)



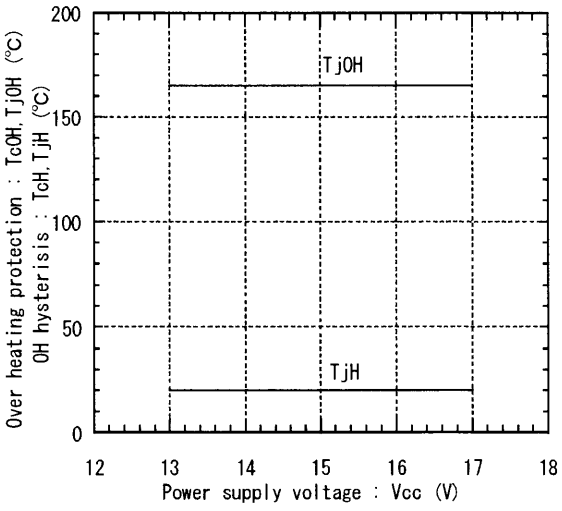
Under voltage vs. Junction temperature (typ.)



Alarm hold time vs. Power supply voltage (typ.)



Over heating characteristics
TjOH, TjH vs. Vcc (typ.)



18. Reliability Test Items

Test categories		Test items	Test methods and conditions	Reference norms EIAJ ED-4701	Number of sample	Acceptance number
Mechanical Tests	1	Terminal strength 端子強度 (Pull test)	Pull force : 40 N (main terminal) 10 N (control terminal) Test time : 10 ±1 sec.	Test Method 401 Method Ⅰ	5	(0 : 1)
	2	Mounting Strength 締付け強度	Screw torque : 1.3 ~ 1.7 N·m (M4) Test time : 10 ±1 sec.	Test Method 402 method Ⅱ	5	(0 : 1)
	3	Vibration 振動	Range of frequency : 10～500 Hz Sweeping time : 15 min. Acceleration : 100 m/s^2 Sweeping direction : Each X,Y,Z axis Test time : 6 hr. (2hr./direction)	Test Method 403 Condition code B	5	(0 : 1)
	4	Shock 衝撃	Maximum acceleratio : 5000 m/s^2 Pulse width 1.0 ms Direction : Each X,Y,Z axis Test time : 3 times/direction	Test Method 404 Condition code B	5	(0 : 1)
	5	Solderabitlity はんだ付け性	Solder temp. : 235 ±5 ℃ Immersion duration : 5.0 ±0.5 sec. Test time : 1 time Each terminal should be Immersed in solder within 1~1.5mm from the body.	Test Method 303 Condition code A	5	(0 : 1)
	6	Resistance to soldering heat はんだ耐熱性	Solder temp. : 260 ±5 ℃ Immersion time : 10 ±1sec. Test time : 1 time Each terminal should be Immersed in solder within 1~1.5mm from the body.	Test Method 302 Condition code A	5	(0 : 1)
Environment Tests	1	High temperature storage 高温保存	Storage temp. : 125 ±5 ℃ Test duration : 1000 hr.	Test Method 201	5	(0 : 1)
	2	Low temperature storage 低温保存	Storage temp. : -40 ±5 ℃ Test duration : 1000 hr.	Test Method 202	5	(0 : 1)
	3	Temperature humidity storage 高温高湿保存	Storage temp. : 85 ±2 ℃ Relative humidity : 85 ±5% Test duration : 1000hr.	Test Method 103 Test code C	5	(0 : 1)
	4	Unsaturated pressure cooker プレッシャークッカー	Test temp. : 120 ±2 ℃ Atmospheric pressure : 1.7x10^5 Pa Test humidity : 85 ±5% Test duration : 96 hr.	Test Method 103 Test code E	5	(0 : 1)
	5	Temperature cycle 温度サイクル	Test temp. : Minimum storage temp. -40 ±5℃ Maximum storage temp. 125 ±5℃ Normal temp. 5 ~ 35℃ Dwell time : Tmin ~ T_N ~ Tmax ~ T_N 1hr. 0.5hr. 1hr. 0.5hr. Number of cycles : 100 cycles	Test Method 105	5	(0 : 1)
	6	Thermal shock 熱衝撃	Test temp. : High temp. side 100 $^{+0}_{-5}$ ℃ Low temp. side 0 $^{+5}_{-0}$ ℃ Fluid used : Pure water (running water) Dipping time : 5 min. par each temp. Transfer time : 10 sec. Number of cycles : 10 cycles	Test Method 307 method Ⅰ Condition code A	5	(0 : 1)

Test categories		Test items	Test methods and conditions		Reference norms EIAJ ED-4701	Number of sample	Acceptance number
Endurance Tests	1	High temperature reverse bias 高温逆ﾊﾞｲｱｽ	Test temp. Bias Voltage Bias Method Test duration	: Ta = 125 ±5℃ (Tj ≦ 150 ℃) : VC = 0.8×VCES : Applied DC voltage to C-E Vcc = 15V : 1000 hr.	Test Method 101	5	(1 : 0)
	2	Intermitted operating life (Power cycle) 断続動作	ON time OFF time Test temp. Number of cycles	: 2 sec. : 18 sec. : ∆ Tj=100 ±5deg Tj ≦ 150 ℃, Ta=25 ±5℃ : 15000 cycles	Test Method 106	5	(1 : 0)

19. Failure Criteria

Item	Characteristic		Symbol	Failure criteria		Unit	Note
				Lower limit	Upper limit		
Electrical characteristic	Leakage current		ICES	-	USL×2	mA	
	Saturation voltage		VCE(sat)	-	USL×1.2	V	
	Forward voltage		VF	-	USL×1.2	V	
	Thermal resistance	IGBT	Rth(j-c)	-	USL×1.2	℃/W	
		FWD	Rth(j-c)	-	USL×1.2	℃/W	
	Over Current Protection		Ioc	LSL×0.8	USL×1.2	A	
	Alarm signal hold time		tALM	LSL×0.8	USL×1.2	ms	
	Over heating Protection		TcOH	LSL×0.8	USL×1.2	℃	
	Isolation voltage		Viso	Broken insulation		-	
Visual inspection	Visual inspection ┌Peeling Plating └and the others		-	The visual sample		-	

LSL : Lower specified limit.

USL : Upper specified limit.

Note : Each parameter measurement read-outs shall be made after stabilizing the components at room ambient for 2 hours minimum, 24 hours maximum after removal from the tests. And in case of the wetting tests, for example, moisture resistance tests, each component shall be made wipe or dry completely before the measurement.

Warnings

1. This product shall be used within its absolute maximum rating (voltage, current, and temperature). This product may be broken in case of using beyond the ratings.
   製品の絶対最大定格（電圧，電流，温度等）の範囲内で御使用下さい。絶対最大定格を超えて使用すると、素子が破壊する場合があります。

2. Connect adequate fuse or protector of circuit between three-phase line and this product to prevent the equipment from causing secondary destruction.
   万一の不慮の事故で素子が破壊した場合を考慮し、商用電源と本製品の間に適切な容量のヒューズ又はブレーカーを必ず付けて2次破壊を防いでください。

3. When studying the device at a normal turn-off action, make sure that working paths of the turn-off voltage and current are within the RBSOA specification. And ,when studying the device duty at a short-circuit current non-repetitive interruption, make sure that the paths are also within the SCSOA specification. In case of use of IGBT-IPM over these specifications,it might be possible to be broken.
   通常のターンオフ動作における素子責務の検討の際には、ターンオフ電圧・電流の動作軌跡がRBSOA仕様内にあることを確認して下さい。また、非繰返しの短絡電流遮断における素子責務の検討に際しては、SCSOA仕様内である事を確認して下さい。これらの仕様を越えて使用すると、素子が破壊する場合があります。

4. Use this product after realizing enough working on environment and considering of product's reliability life. This product may be broken before target life of the system in case of using beyond the product's reliability life.
   製品の使用環境を十分に把握し、製品の信頼性寿命が満足できるか検討の上、本製品を適用して下さい。製品の信頼性寿命を超えて使用した場合、装置の目標寿命より前に素子が破壊する場合があります。

5. If the product had been used in the environment with acid, organic matter, and corrosive gas (For example : hydrogen sulfide, sulfurous acid gas), the product's performance and appearance can not be ensured easily.
   酸・有機物・腐食性ガス（硫化水素，亜硫酸ガス等）を含む環境下で使用された場合、製品機能・外観などの保証は致しかねます。

6. The thermal stress generated from rise and fall of Tj restricts the product lifetime.
   You should estimate the ΔTj from power losses and thermal resistance, and design the inverter lifetime within the number of cycles provided from the power cycle curve. (Technical Rep. No.: MT6M4057)
   製品の寿命は、接合温度の上昇と下降によって起こる熱ストレスで決まります。損失と熱抵抗からΔTjを推定し、パワーサイクル寿命カーブで決まるサイクル数以下で、インバータの寿命を設計して下さい(技術資料№:MT6M4057)。

7. Never add mechanical stress to deform the main or control terminal.
   The deformed terminal may cause poor contact problem.
   主端子及び制御端子に応力を与えて変形させないで下さい。 端子の変形により、接触不良などを引き起こす場合があります。

8. If excessive static electricity is applied to the control terminals, the devices can be broken.
   Implement some countermeasures against static electricity.
   制御端子に過大な静電気が印加された場合、素子が破壊する場合があります。取り扱い時は静電気対策を実施して下さい。

Caution

1. Fuji Electric is constantly making every endeavor to improve the product quality and reliability. However, semiconductor products may rarely happen to fail or malfunction. To prevent accidents causing injury or death, damage to property like by fire, and other social damage resulted from a failure or malfunction of the Fuji Electric semiconductor products, take some measures to keep safety such as redundant design, spread-fire-preventive design, and malfunction-protective design.
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